

# 20 MHz Bandwidth Envelope Tracking Power Supply Using eGaN<sup>®</sup> FETs

*This article, we will present an ET power supply using EPC8004 high frequency eGaN FETs for 4G LTE wireless base station infrastructure. The ET power supply is based on a multi-phase, zero-voltage switching (ZVS) synchronous buck converter. It offers 20 MHz large signal bandwidth, delivering over 60 W average load power sourced from 30 V. 92% average total efficiency is achieved when tracking a 20 MHz LTE envelope with 7 dB peak-to-average power ratio (PAPR).*

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## Multi-Phase Topology with Soft-Switching

A four-phase synchronous buck pulse-width modulated (PWM) topology is selected, as shown in figure 1. The power switches are EPC8004 eGaN FETs. The PWM control signals for adjacent phases are phase-shifted by 90 degrees. Switching at 25 MHz in each phase gives the full converter an effective output switching frequency of 100 MHz. A resistive load is used to represent the radio-frequency power amplifier (RFPA), and a fourth-order filter with 20 MHz bandwidth that supports zero-voltage switching is designed, allowing high efficiency operation and automatic phase current balancing [2]. The printed circuit board (PCB) layout is optimized according to the design practices in [3].

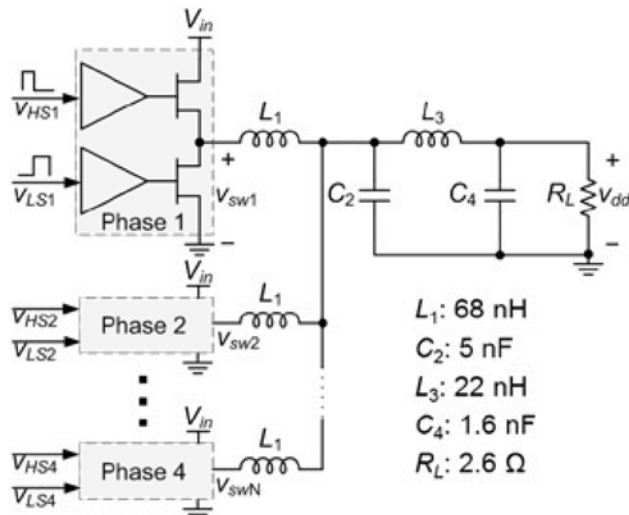


Figure 1: Diagram of a four-phase synchronous Buck converter with fourth-order output filter

## Low loss High Speed Gate Driver

Design of the gate driver that supports switching at high frequency is very challenging, particularly for the high-side FET in the half-bridge configuration. Traditional bootstrap half-bridge gate drivers (LM5113 [4], for instance), designed for higher current, lower frequency appli-

cations, generally have high loss due to the reverse recovery charge of the bootstrap diode. As a result, the maximum switching frequency is limited. In order to achieve 25 MHz switching frequency while maintaining high efficiency, a synchronous FET bootstrap supply [5] is used.

In [5], a way to use LM5113 at high frequency is introduced, with proper circuitry to disable its internal bootstrap diode. In this application, however, a different approach is implemented. As shown in figure 2, digital isolators ISO721MD [6] and ultra-high speed logic gates SN74LVC2G14 [7] are used instead of the LM5113. The EPC2038, with the smallest electrical and physical footprint is selected as the synchronous bootstrap FET ( $Q_{BST}$ ) for minimal parasitics and associated losses. The low side FET driver consists of the same component as the high side for matched propagation delay.

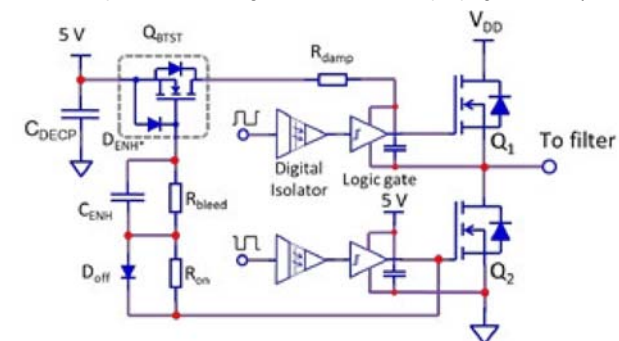


Figure 2: Schematic diagram of the gate drive circuit with synchronous FET bootstrap supply, for one phase of the system converter

## Static Efficiency Measurement

The ET supply is evaluated at steady-state operating points. Figure 3 shows the measured power-stage efficiency, and total efficiency that includes the losses in the gate driver, for a range of duty cycles (output voltages). The peak efficiencies are greater than 94% and 93% for power-stage and total, respectively, at around  $D = 0.5$ , or 15 V output. The static measurement was not performed for output voltages higher than 17 V due to thermal limit as no heat sink is mounted on the eGaN FETs.

The probability distribution function (PDF) of a 20 MHz 7 dB PAPR LTE envelope signal is also shown in figure 3. Even though the output voltage range is from 5 V to 28 V, voltages around 9 V to 15 V occur with significantly higher probability. Nevertheless, the power stage efficiency is greater than 90% over the whole range.

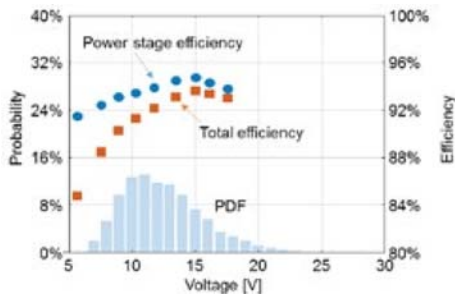


Figure 3: Measured steady-state power-stage efficiency and total efficiency; and probability distribution function (PDF) of the 20 MHz LTE envelope signal

#### Dynamic ET Measurement

The 20 MHz LTE envelope signal is converted into eight PWM signals, for controlling the high side and low side FETs in four phases. Appropriate dead times to achieve ZVS operation are also implemented at this stage. The PWM signals are stored in the memories of an Altera® Arria® V FPGA [8] and transmitted to the gate drivers. The resolution of the pulse width is around 0.2 ns, allowing fine adjustment of duty cycles and dead times for high fidelity ET performance. The block diagram of the LTE signal generator system is shown in figure 4.



Figure 4: Simplified diagram of ET signal generation

The output of the ET supply is measured with a 1 GHz differential probe (TDP1000). A sample of the measured output voltage is compared to the reference in figure 5. The average output power is 67 W and the peak value is 346 W, corresponding to 7 dB PAPR. Average power-stage efficiency and total efficiency are 93% and 92%, respectively. Accurate

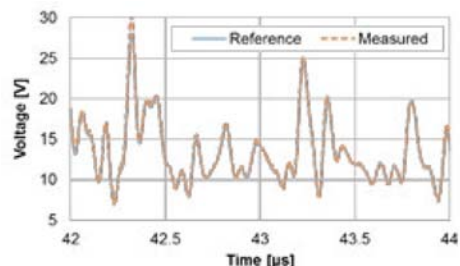


Figure 5: Reference and measured LTE envelope signal

tracking is achieved with the normalized root-mean-square error (NRMSE) of only 1.2%. The measured maximum current slew rate is 180 A/µs.

#### Summary

eGaN FETs and integrated circuits are helping to achieve very high switching frequency in switched-mode power supplies, leading to breakthroughs in a large number of applications where bandwidth, slew rate and efficiency are critical. ET is one of them.

Due to lower input and output capacitances ( $C_{ISS}$  and  $C_{OSS}$ ) and lower gate charge ( $Q_G$ ) [9], GaN based switching converters are able to operate at tens of megahertz switching frequency with high efficiency. With topologies such as multi-phase and multi-level, GaN switching converters can achieve high bandwidth that meets the requirement of modern wireless communication standards, such as 4G LTE.

An ET power supply with four-phase soft-switching buck converter using EPC8004 is able to accurately track a 20 MHz 7 dB PAPR LTE envelope signal with greater than 92% total efficiency, delivering 60 W average power. The design is also scalable to satisfy different power levels by choosing different EPC parts.

eGaN® FET is a registered trademark of Efficient Power Conversion Corporation.

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