

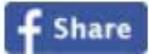
Article appeared on EDN Asia Online, March 2011

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## Shrink System Size with a 19 V – 1.2 V Buck Converter Using eGaNTM FETs

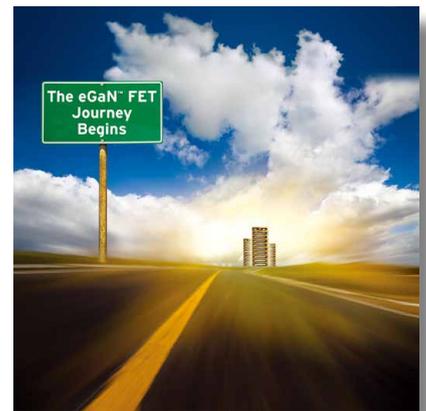
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### Introduction

Efficient Power Conversion Corporation (EPC) last year introduced a family of enhancement mode gallium nitride (eGaN) FETs. These devices were designed as replacements for the venerable – but aged – power MOSFET. One of the primary benefits of this new technology is that these FETs are capable of much higher switching speed with lower power losses. Pushing frequency higher to reduce the size and cost of energy storage and transmission elements such as capacitors, inductors and transformers has been discussed for many years. Unfortunately, with traditional silicon power devices, the tradeoff between frequency and efficiency has been too painful to implement commercially. eGaN FETs now make it possible for designers to reduce the space occupied by their DC-DC converters in 4 cell and industrial systems by increasing frequency while still exceeding efficiencies of converters based on conventional silicon power MOSFETs.



### Background

eGaN FETs begin with roughly a 10 times superior conduction mechanism than silicon. Electrons needed to conduct current in an eGaN FET, instead of jumping from lattice point to lattice point, form a 2 dimensional electron gas (2DEG) where they are free to move about virtually unimpeded. This 2DEG is created when a strain field is induced by depositing Aluminum Gallium Nitride (AlGaN) on a layer of GaN as shown in the cross section of figure 1. This class of device is known as a High Electron Mobility Transistor (HEMT).

In addition to the order of magnitude greater conductivity, GaN has a 10 times higher critical electric field. This allows terminals to be an order of magnitude closer together compared against silicon based devices, giving GaN a theoretical conduction advantage of more than two orders of magnitude.

To drive frequency higher in a Buck Converter, especially with a high input voltage, the power devices must have very low dynamic losses. The dominant component to the dynamic losses is the classic hard switching event where current commutates to output current before the voltage collapses. This event is shown in figure 2, and is reversed during turn off. The energy of each switching period is approximated by  $E_{SW} = V_{IN} \times I_{OUT} \times t$  where  $t$  is determined by the various components of the devices gate charge ( $Q_G$ ), device series gate resistance ( $R_G$ ), driver impedance, drive voltage, and device transfer characteristics. Due to eGaN FETs requiring much less die area and having a lateral structure, they have ultra-low gate charge. This, combined with a gate electrode designed to have low  $R_G$ , switching times for these devices are very short, and energy dissipated due to classical hard switching is very low.

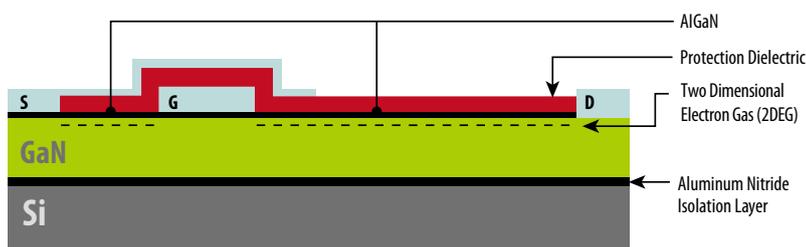


Figure 1: EPC's GaN Power Transistor Structure

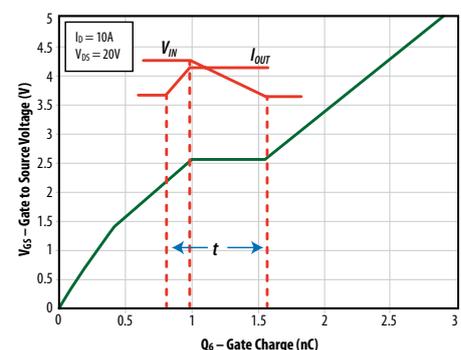


Figure 2: Classical Hard Switching Waveform

Other components that contribute significantly to dynamic losses are reverse recovery charge ( $Q_{RR}$ ), Output charge ( $Q_{OSS}$ ), gate charge ( $Q_G$ ), and reverse conduction voltage ( $V_{SD}$ ). The energy loss corresponding to each of these components can be expressed as:

$$E_{RR} = Q_{RR} \times V_{IN}$$

$$E_{OSS} = \frac{1}{2} Q_{OSS} \times V_{IN}$$

$$E_G = Q_G \times V_{GS}$$

$$E_{SD} = V_{SD} \times I_{OUT} \times t_R \quad (t_R \text{ is the total reverse conduction time})$$

Dynamic power dissipation is the sum of the dynamic energy losses multiplied by frequency:

$$P_{DYN} = f \times (E_{SW} + E_{RR} + E_{OSS} + E_G + E_{SD})$$

Because eGaN FETs are purely majority carrier devices, there are no minority carriers to be stored in a junction, and therefore, there is no  $Q_{RR}$ . Since the devices are so small for their  $R_{DS(ON)}$ ,  $Q_{OSS}$  is small as well. For eGaN FETs, both  $V_{GS}$  and  $Q_G$  are low, so  $E_G$  is negligible. Because of the reverse current conduction mechanism, eGaN FETs have a high  $V_{SD}$  when compared with the body diode forward voltage of a MOSFET. Care must therefore be taken to minimize the time that the rectifier switch is acting like a diode.

### Experimental Setup

As most components of dynamic losses are related to  $V_{IN}$ , higher input voltage increases the merit of switching to eGaN FETs. Netbook computers frequently use a 4 cell system with a 19 V charge voltage. This voltage is converted down to the required processor voltage, memory or other power-bus voltage using a single stage buck converter. For comparison, a typical output voltage of 1.2 V was chosen as representative of this application. Today's most prevalent solution, MOSFETs at 300 kHz, was tested as a baseline. Testing was then done for both eGaN FETs and MOSFETs at 300 kHz, 500 kHz and 800 kHz. The basic circuit is shown in figure 3.

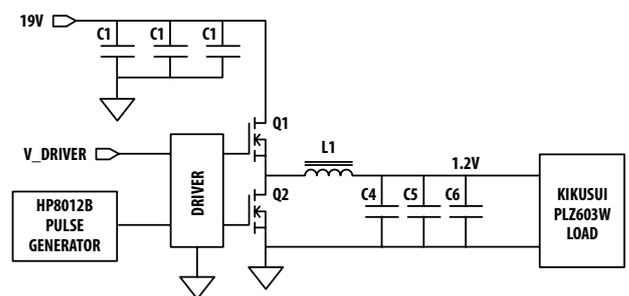


Figure 3: Schematic Diagram

The devices compared were EPC eGaN FETs with the EPC1014 (40 V, 16 mΩ) on the high side and EPC1015 (40 V, 4 mΩ) on the low side, and Infineon MOSFETs BSZ130M03MS (30 V, 15 mΩ) on the high side and BSZ035N03M (30 V, 4.3 mΩ) on the low side. In all cases, a single device was used for each socket. The MOSFETs were chosen as they are state of the art and similar  $R_{DS(ON)}$ . 40 V eGaN FETs were compared with 30 V MOSFETs because higher overshoot can be expected with the much higher switching speeds of the eGaN FETs. Table 1 shows important characteristics of the switching devices.

	$V_{DS}$ (V)	Q1		Q2				$V_{SD}$ (typ) 10A, 25°C	Total Package Area (nom)
		$R_{DS(ON)}$ (max) High Side	$Q_G$ (typ) High Side	$R_{DS(ON)}$ (max) Low Side	$Q_G$ (typ) Low Side	$Q_{OSS}$ (typ) Low Side	$Q_{RR}$ (max) Low Side		
eGaN FET	40	16 mΩ	0.55 nC	4 mΩ	11.6 nC	18.5 nC	0 nC	2.15 V	8.5 mm <sup>2</sup>
MOSFET	30	15 mΩ	1.5 nC	4.3 mΩ	27 nC	32 nC	20 nC	0.76 V	21.8 mm <sup>2</sup>

Table 1 - Switching Components

Gate drive voltages for all experiments were +5  $V_{GS}$  for the ON state, and 0  $V_{GS}$  for the OFF state. The converters were run open-loop with the duty cycle adjusted for the appropriate output voltage. The output filter was kept small to take advantage of the space savings enabled by high frequency conversion (See Table 2). For 800 kHz testing, only one output filter capacitor was used and for 300 kHz testing, a 470 μF PosCap was added. Tests were performed from zero load to 10 A. A baseline was obtained using the same MOSFETs at 300 kHz, a typical switching frequency for this application.

Component	Reference Designator	Part Number	Characteristics
Input Filter Capacitor	C1, C2, C3	Taiyo Yuden, UMK-325BJ475M	4.7 μF, 50 V, 1210, Ceramic
Output Filter Inductor	L1 <sup>1</sup>	Wurth, 7443340068	0.68 μH, 19 A, 1.72 mΩ, 8 mm x 8 mm
		or Vishay, IHLP2525CZ-R47-01	0.47 μH, 17.5A, 4 mΩ, 6 mm x 6 mm
Output Filter Capacitor	C4, C5 <sup>2</sup> C6 <sup>3</sup>	TDK, C3216XSR0J476M	47 μF, 6.3 V, XSR, 1206, Ceramic
		Sanyo, 2R5TPE470M7	PosCap, 470 μF, 2.5 V, 7 mΩ

Note 1: For 800 kHz testing, the smaller Vishay inductor was used.  
 Note 2: For 800 kHz testing, only a single output capacitor was used – C4.  
 Note 3: C6 was only used for 300 kHz testing

Table 2 - Input and Output Filter Components

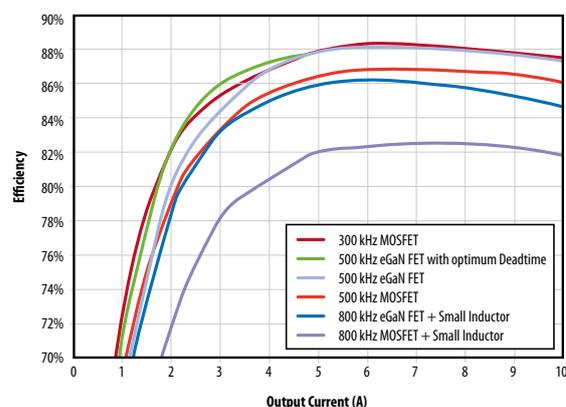


Figure 4: Efficiency Results

## Experimental Results

The tests show that the circuit with eGaN FETs running at 500 kHz was comparable to the baseline of MOSFETs at 300 kHz, while the MOSFET circuit saw an efficiency decrease of roughly 1.5% through most of the current range at 500 kHz.

At low current, the efficiency decreases for the eGaN FET solution because the fixed dead-time was minimized for optimal high current operation. This resulted in the loss of the zero-voltage switching advantage at light loads. However, when the dead-time was increased, as an adaptive type driver would do, the 500 kHz efficiency of the eGaN FET system became comparable to that of the 300 kHz MOSFET system under all load conditions.

Between the size reduction of the power switches and the elimination of the PosCap, the increased frequency capability of the eGaN FET system realized a saving of 36 mm<sup>2</sup> of board space (about 20%) with no efficiency penalty. Efficiency results can be seen in Figure 4.

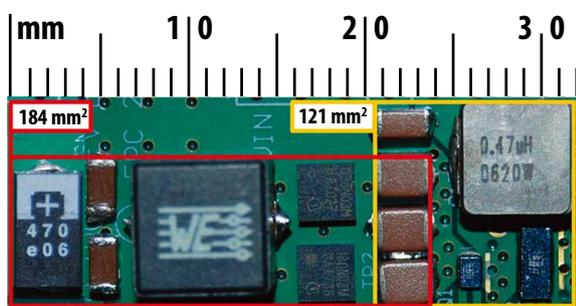


Figure 5: Size comparison between 300 kHz MOSFET buck (Red) and 800 kHz eGaN FET buck (Orange)

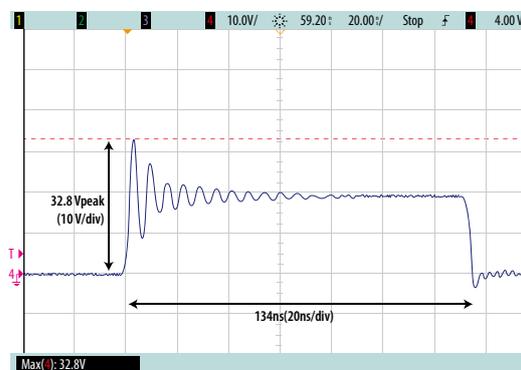


Figure 6: Switch-node Wave Form Showing Q1 On-Time at 500 kHz, 10A

The frequency was then increased to 800 kHz on the eGaN system, and output filter reduced to maximize board space savings. Even with the higher switching speeds, overshoot was limited to 33 V, and ringing was mostly damped in only a few cycles as shown in Figure 6.

The result was impressive. Efficiency over most of the current range stayed within 1% of the 500 kHz MOSFET system. The peak efficiency was over 86%, and the board space saved was 30 mm<sup>2</sup> (an additional 20%). Board space requirements are compared in Figure 5. This space savings can be translated into a reduced size and price of the multi-layer printed circuit board, or in increased performance by using that space for processing power and memory.

Modern DC-DC converters have limits on the voltage variation both in term of transients and ripple. Increasing frequency allows the output filter to be reduced while still maintaining a low ripple. The output filter components in these experiments were reduced to keep voltage ripple reasonably constant at about 12 mV peak-to-peak (1% of DC voltage). Figure 7 shows the output voltage ripple waveforms for 300 kHz, 500 kHz, and 800 kHz operation.

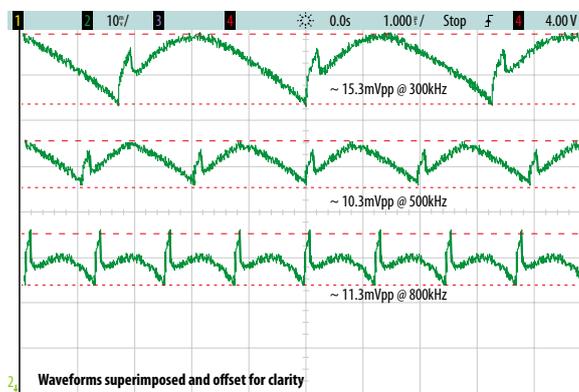


Figure 7: Output Voltage Ripple Waveforms

## Conclusions

We have demonstrated significant system size reductions without loss of efficiency, as well as extreme space savings by driving frequency from the traditional 300 kHz all the way up to 800 kHz. eGaN FETs bring a new spectrum of opportunities to designers wanting to shrink system size, reduce cost, or enhance system efficiency.

## About the Author



Johan Strydom is Vice President, Applications at EPC Corporation. He received his PhD from the Rand Afrikaans University, South Africa in 2001. From 1999 to 2002 he was working as a GRA and post-doctoral researcher at the Center for Power Electronics (CPES), Virginia Tech. Prior to joining EPC, he held various Application Engineering positions at International Rectifier Corporation (IRF) and more recently Linear Technology Corporation (LLTC), working on a wide range of consumer and industrial applications including motor drives, class-D audio, hybrid power modules and DC-DC converters for VRM and POL.