eGaN® FET-Based Synchronous Rectification

As GaN-on-Si becomes more common in DC-DC converter designs, questions often arise from experienced designers about the impact of the unique characteristics of GaN transistors when used as synchronous rectifiers (SRs). In particular, the third quadrant off-state characteristics, better known as "body diode" conduction in Si MOSFETs, which is activated during converter dead-time, is of interest. For this article, the focus will be on the similarities and differences of Si MOSFETs and eGaN FETs when operated as a "body diode" and outline their relative advantages and disadvantages.

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Typical data sheet reverse conduction characteristics of eGaN FETs and Si MOSFETs are shown in figure 1. For the eGaN FETs, the source-drain forward voltage is three to four times larger than that of a Si MOSFET, but there is no reverse recovery charge, Qrr. For Si MOSFETs, Qrr is significant, although it decreases as voltage rating is reduced. For source-drain forward voltage, the values have little dependence on voltage rating.

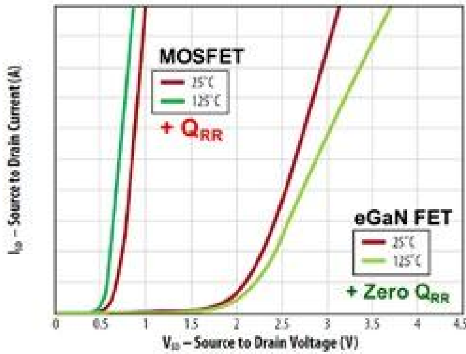


Figure 1: Typical source-to-drain forward drop vs. source-to-drain current and temperature for eGaN FETs and Si MOSFETs

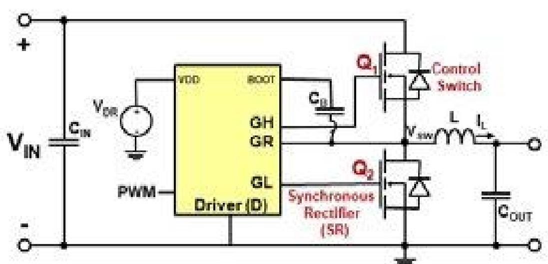


Figure 2: Buck converter schematic with synchronous rectifier

The major effects of reverse recovery can be discussed in the context of the typical buck converter, shown in figure 2. While SR reverse voltage drop V_{SD2} remains relatively consistent versus dead-time, $t_{d,on}$, which is the interval between switching transitions when both Q_1 and Q_2 are commanded to be off, the reverse recovery charge, Q_{RR}, is strongly affected by dead-time [1], [2].

Dead-time is necessary in practical converters to prevent cross-conduction of Q_1 and Q_2 due to the non-zero switching time, since cross-conduction results in shoot-through currents and corresponding high losses. However, dead-time also results in losses and the design of a high-efficiency converter will be improved by understanding the underlying mechanisms, of which two are dominant; reverse voltage drop and reverse recovery.

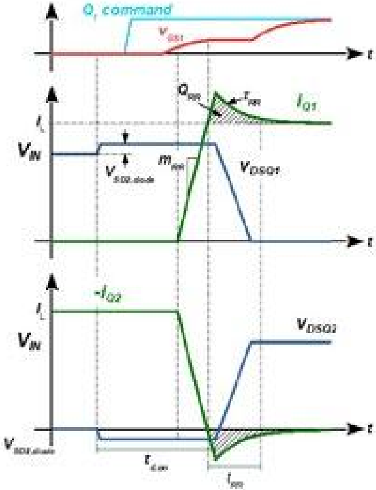


Figure 3: Idealized buck converter deivce Q1 turn-on waveforms, including reverse recovery of a Si MOSFET body diode

Reverse Voltage Drop And Dead-Time Losses

There are two dead-times to consider. The turn-on dead-time, $t_{d,on}$, is the interval between the time Q_2 responds to its turn-off command and the time its current i_{Q2} decreases to zero. The turn-off dead-time, $t_{d,off}$, is the interval beginning when Q_1 responds to its turn-off command and the time when Q_2 responds to its turn-on command. Figure 3 shows the key turn-on dead-time waveforms, and the turn-off dead-time is similar. During $t_{d,on}$ and $t_{d,off}$ the channel of Q_2 is off, and inductor current I_L flows through the body diode for a MOSFET and body diode like mechanism [3] for a GaN transistor.

In silicon MOSFETs this body diode is comprised of the PN junction formed between the drain epitaxial layer and the source wells. This diode has a forward voltage drop V_{SD2} of 0.6 - 0.8 V. The effective body diode in an eGaN FET arises when the gate and source are tied together with $V_{SD2} \approx 2.5\text{-}3$ V at nominal currents. The body diode conduction loss is easily computed by equation (1):

$$P_{SR,VSD}=I_L \cdot V_{SD2} \cdot f_{sw} \cdot (t_{d,on}+td_{,off}) \quad (1)$$

The higher V_{SD2} for eGaN FETs means that dead-time conduction losses are larger than those for silicon MOSFETs. This can be mitigated via an external Schottky diode or by good dead-time management [4], [5]. The faster switching of eGaN FETs compared to Si MOSFETs means that smaller dead-times are practical with GaN.

Reverse Recovery and Indirect Dead-Time Losses

Reverse recovery is a major source of switching loss, sometimes dominating all other switching loss mechanisms. However, it is frequently underestimated or even ignored, due to the lack of good data and challenging analysis, particularly for lower voltage FETs. As power density and efficiency demands continue to increase, reverse recovery losses merit closer inspection. Dead-time has a strong effect on reverse recovery [2]. This can result in much higher losses than body diode conduction in silicon MOSFETs, and these losses can far exceed the body diode conduction losses of eGaN FETs [1].

Reverse recovery is a phenomenon of PN junction diodes. When such a diode conducts a current $i_D = I_L$ in the forward direction, a population of minority carriers is injected into the junction depletion region. The final size of this carrier population corresponds to the magnitude of I_L. A portion of this population lags changes in i_D, with a time constant dependent on diffusion time, mobility, and recombination time of the minority carriers [6]. This portion of the carrier population is often referred to as stored junction charge. It is often confused with the capacitive depletion charge, but differs in that it is primarily a function of the diode current waveform, not the voltage waveform. As long as the stored charge remains in the junction, the diode can be considered to be in the conducting state regardless of the current value or direction. For the eGaN FET, reverse conductionis based on majority carrier devices with no PN junction, hence they do not exhibit reverse recovery.

Reverse recovery occurs when reverse voltage is applied to a PN diode that is conducting in the forward direction. It thus occurs during turn-on of Q_1. Figure 3 shows typical turn-on waveforms. At the beginning of the turn-on dead-time interval, the channel of Q_2 is turned off, forcing inductor current – I_L through the body diode. Then Q1 is turned on and begins to carry an increasing portion of I_L. When the control FET current reaches I_L, $i_{Q2} = 0$, an ideal diode would stop conducting. However, in a real PN junction diode, the stored charge in the junction region lags the current. Thus, the diode remains on, and since Q_1 is also on, the voltage V_{BUS} forces the current to continue to increase. This additional current flows strictly through the power loop, and is known as the reverse recovery current, where it acts as a shoot-through current and significantly increases losses. The stored charge begins to decay when the current reverses, and eventually reaches the point that it is just enough to support I_{RRM}, the peak negative i_{Q2} current, after which the current magnitude decreases exponentially with time constant t_{RR} until the $i_{Q2} = 0$, $i_{Q1} = I_L$, and the diode is off. The extra current that flows results in an extra charge termed reverse recovery charge (Q_{RR}) flowing through the power loop, and the resultant losses are given by:

$$P_{SR,VSD}=Q_{RR} \cdot V_{BUS} \cdot f_{sw} \quad (2)$$

Unfortunately, an accurate Q_{RR} value is difficult to obtain. Silicon MOSFET data sheets normally supply numbers for body diode Q_{RR} and t_{RR} under unrealistic conditions. Q_{RR} values may or may not include Q_{oss}, and this is rarely specified. Measurement of reverse recovery parameters under realistic conditions is challenging and error-prone, and accurate modeling of reverse recovery in typical device models is rare. This leads to poor estimates of reverse recovery losses.

Comparison of eGaN FETs and Si MOSFETs in V_{IN}=48 V Synchronous Rectification

Now let's look at the impact of the dead-time period on in-circuit performance for eGaN FET and Si MOSFET based SR designs. We will look at a V_{IN} = 48 V to V_{OUT} = 12 V synchronous buck converter operating in the frequency range of f_{sw} = 300 kHz to f_{sw} = 1 MHz. The experimental evaluation boards are shown in figures 4 (a) and (b) for the eGaN FET (EPC2045) and Si MOSFET equivalent, respectively. Each board is designed with a similar layout based on [7], use four-layer two by two inch two-ounce copper PCBs, and use gate drivers designed for their respective technologies.

To evaluate the impact of dead-time on performance for the two systems, the dead-time was tuned for each of the measurement points using no-load timing for consistency. Since the impact of Q_{RR} is seen during device Q_1 turn-on, only the rising edge dead-time, t_{Dead_Rise}, was varied, with the falling dead-times minimized to 10 ns and 15 ns, for the GaN transistor and Si MOSFET, respectively.

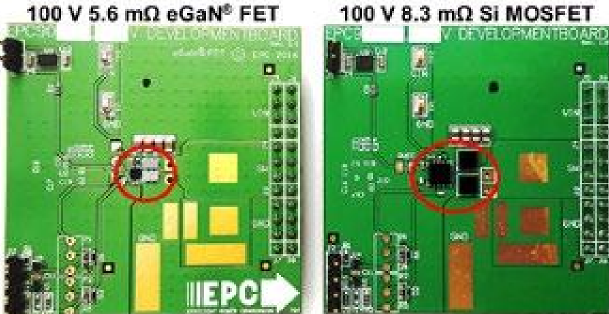


Figure 4: V_{IN} = 48 V demonstration systems (a) eGaN FET based design EPC9078 with EPC2045 eGaN FETs and LMG5113 GaN FET 5 V gate driver and (b) Si MOSFET based design with BSZ097N10NS5 Si MOSFETs and ISL2111 MOSFET 10 V gate driver

The minimum dead-time case is used as a baseline and subtracted from all other loss measurements. This enables quantification of the losses due to dead-time effects. For the faster eGaN FET, a minimum dead-time of 5 ns was selected, for the slower Si MOSFET, a minimum dead-time of 10 ns was selected. Figure 5 shows the impact of the duration of the "body-diode" conduction during dead-time on performance for output currents of 6 A, 10 A, and 14 A for switching frequencies of 500 kHz (figure 5(a)) and 1 MHz (figure (5b)). As dead-time is increased, Si MOSFETs show a large initial increase in loss due to Q_{RR}, which then approaches an asymptote of constant slope due to $V_{SD2,diode}$, as expected. It can be seen from figure 5 that the Si MOSFET Q_{RR} has a strong dependence on the forward biasing duration of the body diode and the current magnitude conducted by the diode. For the Si MOSFET, the ΔQ_{RR} can be estimated from equation 2, and ΔQ_{RR} was measured to be approximately 40 nC for 6 A, 80nC for 10 A, and 135 nC for 14 A for a 50 ns increase in body diode conduction time. From figure 5 (b) it can be seen that the dead-time losses scale proportional to frequency, as predicted in equation 2. The loss increased by more than a factor of two (~2.5) when increasing

the switching frequency from 500 kHz to 1 MHz. This indicates that the Q_{RR} value (nC) has a dependence on f_{sw}, but to a lesser extent than I_{OUT} and t_{Dead_Rise}. In figure 5 (c), a wider range of frequencies, f_{sw}=300 kHz, 500 kHz, and 1 MHz are shown for a load current, I_{OUT}, of 10 A, confirming the eGaN FET was a superior SR over a wide frequency range.

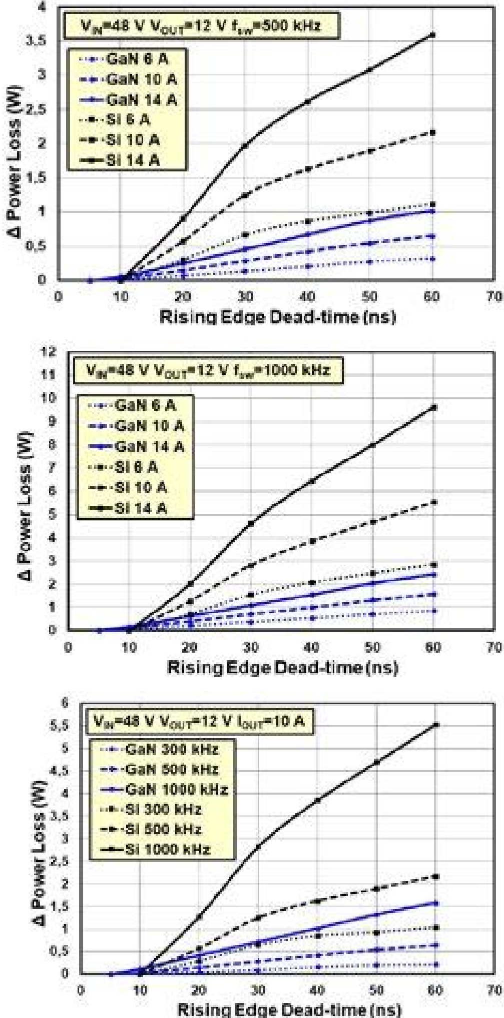


Figure 5: Impact of rising edge dead-time duration on power loss for converters shown in figure 4 with various output currents and a switching frequency of (a) f_{sw}=500 kHz, (b) f_{sw}=1 MHz; and (c) various switching frequencies and an output current of I_{OUT}=10 A

For the eGaN FET with no reverse recovery, losses are proportional to dead-time source-to-drain conduction, as predicted by equation 1. One would expect that the slope of the eGaN FET loss curve would be higher due to the larger V_{SD2} of reverse conduction. Although the slope is higher, the initial high loss from reverse recovery of the Si MOSFETs means that even for large dead-time, the reverse recovery loss of the Si MOSFETs far exceeds losses from the reverse voltage drop of the eGaN FETs. This shows that for SR applications where the body-diode conducts, the GaN transistor is superior to the Si MOSFET as a result of the elimination of Q_{RR}.

The impact of dead-time on system efficiency and power loss was tested and shown in figures 6 (a) and (b), respectively. The eGaN FET based design showed superior performance in all conditions, with the total system losses decreasing by 35% and 40%, and efficiency increasing by 2% and 2.5% for respective rising edge dead-times of 30 ns and 60 ns. The improved switching performance of the eGaN FET based design enables higher power density when the system is optimized, which is discussed in detail in [8].

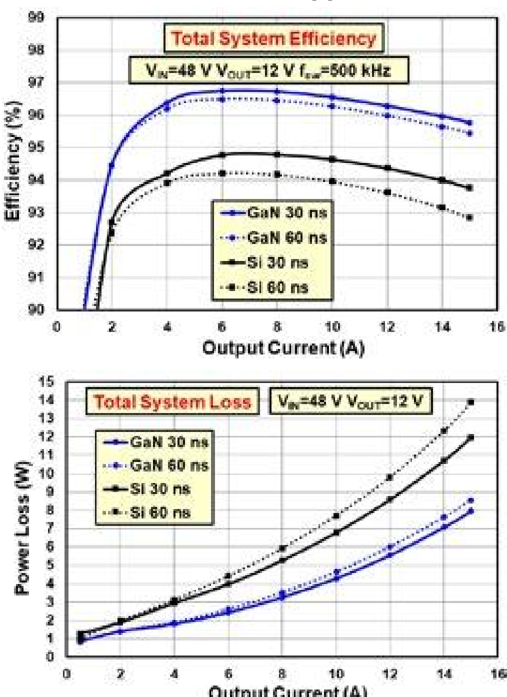


Figure 6: Impact of rising edge dead-time duration on total system (a) efficiency and (b) power loss for experimental converters shown in figure 4 for switching frequency of f_{sw}=500 kHz (IHLP-5050-FD-01)

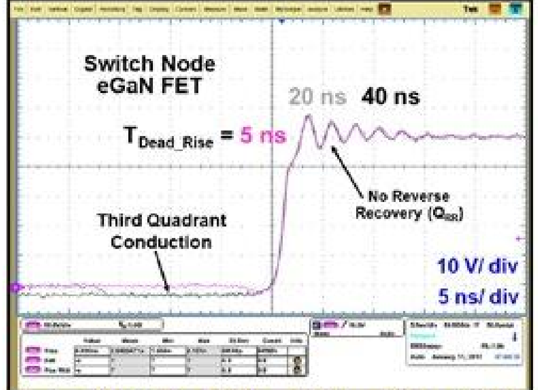
Up to this point, the impact of dead-time on power loss and efficiency was considered exclusively. But the third quadrant "body diode" conduction also has a significant impact on the switching waveforms, which impacts design criteria such as the minimum allowable dead-time, maximum negative switch node voltage of the gate driver/controller, and the peak voltage rating of the device. Shown in figure 7 (a) is the switch node waveform of the eGaN FET for rising edge dead-times of 5 ns, 20 ns, and 40 ns. The eGaN FET, with no reverse recovery, has almost identical switching transitions and peak voltage spikes, allowing a designer to more simply select a minimum dead-time and peak device blocking voltage required. For the eGaN FET based design, the transistor also has a higher third quadrant off-state forward voltage, resulting in a more negative switch node, which impacts driver/controller selection.

For the Si MOSFET based design, the switch node waveforms are shown in figure 7 (b) for dead-times of 5 ns, 20 ns, and 40 ns. The third quadrant body diode voltage is significantly lower than the eGaN FET, but the transitions and peak voltage spikes vary significantly with dead-time, an effect of the reverse recovery charge (Q_{RR}) current. Current will have a similar impact, making it much more challenging for a designer to minimize the dead-time and select a proper device voltage rating.

Conclusions

To summarize the design considerations for effective use of eGaN FETs in synchronous rectification: 1) eGaN FETs have two to three

times higher "body diode" forward voltage drop when compared to Si MOSFETs and the related forward diode conduction losses will increase accordingly and, 2) eGaN FETs completely eliminate reverse recovery Q_{RR} and the related losses are reduced to zero.



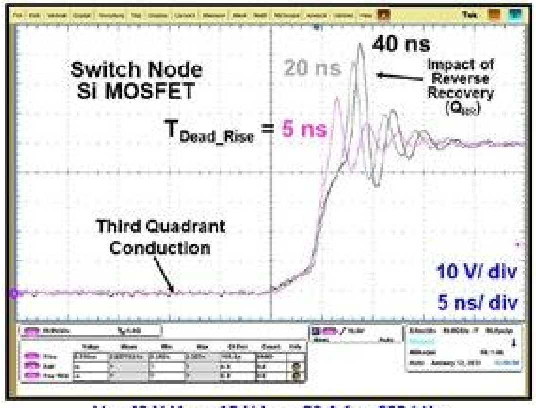


Figure 7: Impact of rising edge dead-time duration on switch node waveforms for (a) GaN transistor based and (b) Si MOSFET based experimental converters shown in figure 4

For higher voltage applications (V_{IN} = 48 V), there is a large impact of QRR on SR loss for Si MOSFETs, and the increase in eGaN FET forward diode conduction loss is very small in comparison, yielding far superior performance for eGaN FET as SRs in most applications. As the voltage increases, the larger the relative advantage will be for eGaN FETs, since Si MOSFET Q_{RR} and related losses both increase with voltage. The dependence of Si MOSFET Q_{RR} on conduction current level was also demonstrated, with higher current levels showing larger advantages for eGaN FETs.

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