

EPC2049 – Enhancement-Mode Power Transistor

Preliminary Specification Sheet

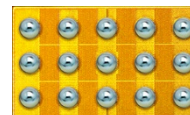
Status: Engineering

Features:

- V_{DS} , 40 V
- Maximum $R_{DS(on)}$, 5 m Ω
- I_D , 16 A

Applications:

- Point of Load Converters
- Envelope Tracking Power Supplies
- LiDAR/Pulsed Power Applications
- Class D Audio
- Low Inductance Motor Drive



EPC2049 eGaN® FETs are supplied in passivated die form with solder bumps.
Die Size: 2.5 mm x 1.5 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	48	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 8^\circ\text{C/W}$)	16	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	175	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.5 \text{ mA}$	40			V
I_{DSS}	Drain Source Leakage	$V_{DS} = 32 \text{ V}$, $V_{GS} = 0 \text{ V}$		0.1	0.4	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.5	5.5	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.1	0.4	mA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 6 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 15 \text{ A}$		4.3	5	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		2		V

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	8.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	64	$^\circ\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

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Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance		670	805	pF
C_{RSS}	Reverse Transfer Capacitance		12		
C_{OSS}	Output Capacitance		350	525	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (note 2)		551		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (note 3)		623		
R_G	Gate Resistance		0.6		Ω
Q_G	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 5\text{ V}, I_D = 15\text{ A}$	6.1	7.6	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 20\text{ V}, I_D = 15\text{ A}$	2.1		
Q_{GD}	Gate-to-Drain Charge		1.1		
$Q_{G(TH)}$	Gate Charge at Threshold		1.5		
Q_{OSS}	Output Charge	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	13	20	
Q_{RR}	Source-Drain Recovery Charge		0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DS} .

Figure 1: Typical Output Characteristics at 25°C

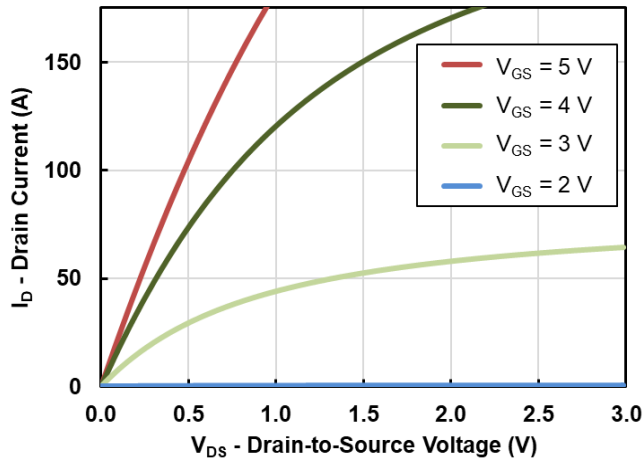
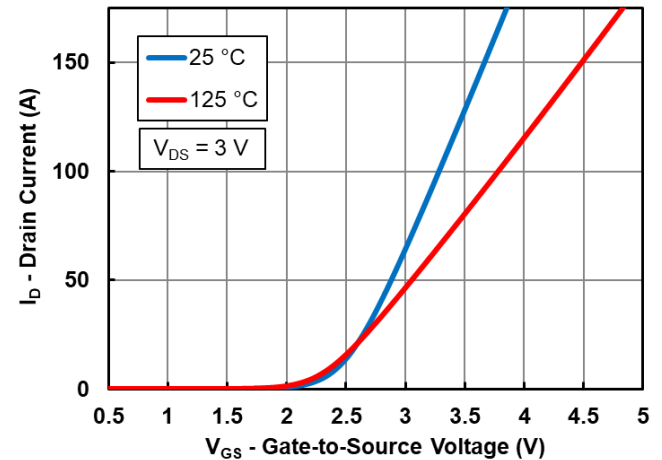


Figure 2: Transfer Characteristics



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Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

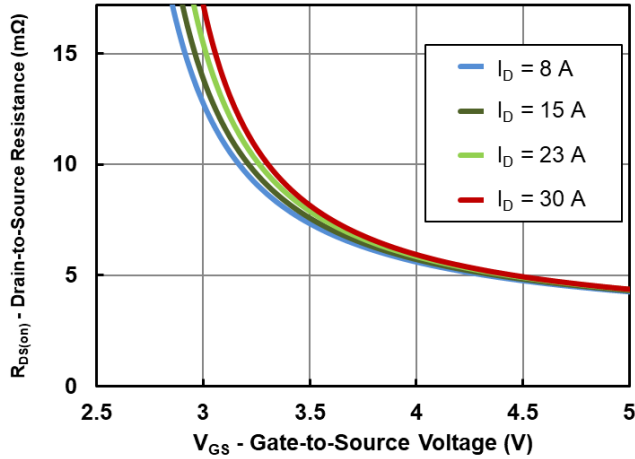


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

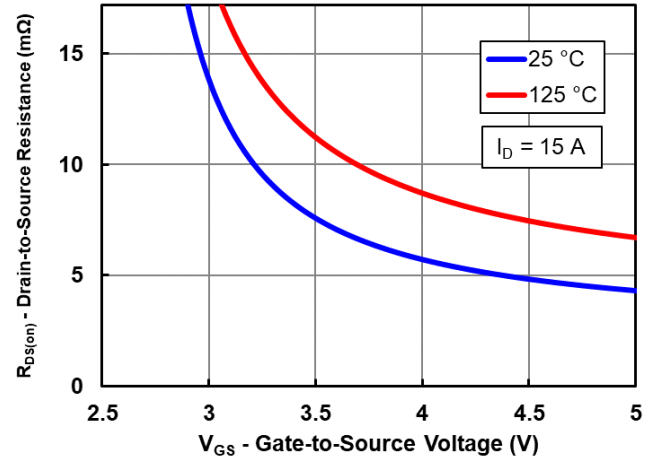


Figure 5a: Capacitance (Linear Scale)

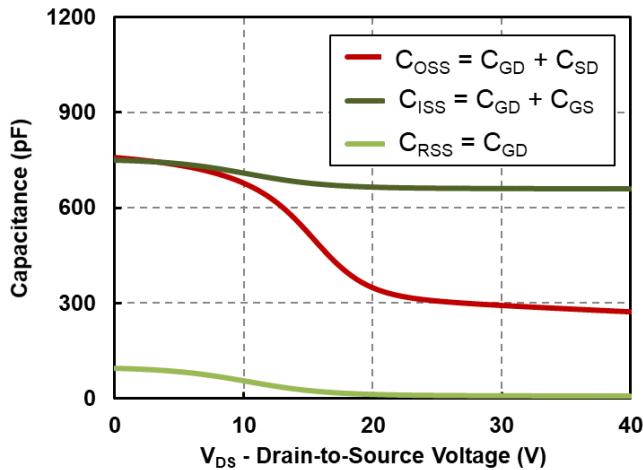


Figure 5b: Capacitance (Log Scale)

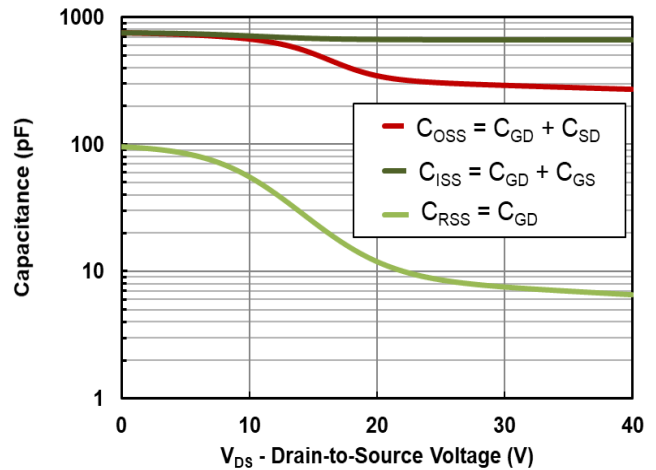


Figure 5c: Output Charge and C_{OSS} Stored Energy

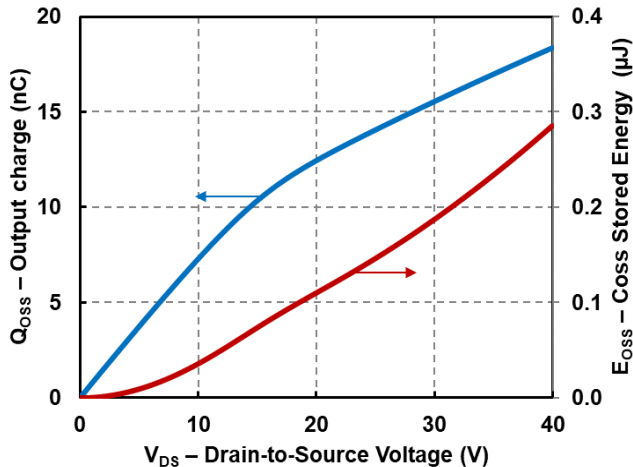
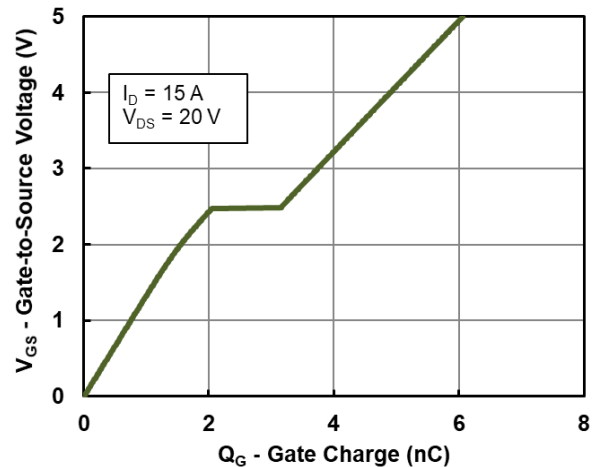


Figure 6: Gate Charge



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Figure 7: Reverse Drain-Source Characteristics

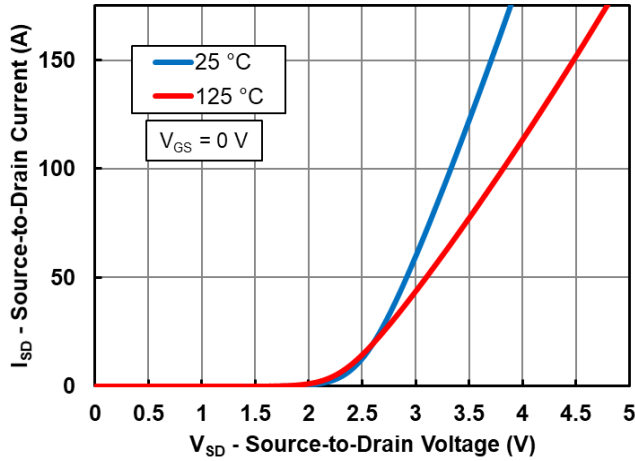


Figure 8: Normalized On-State Resistance vs Temperature

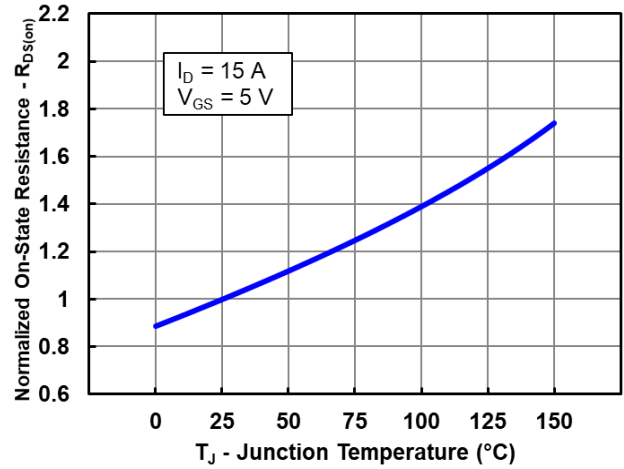


Figure 9: Normalized Threshold Voltage vs Temperature

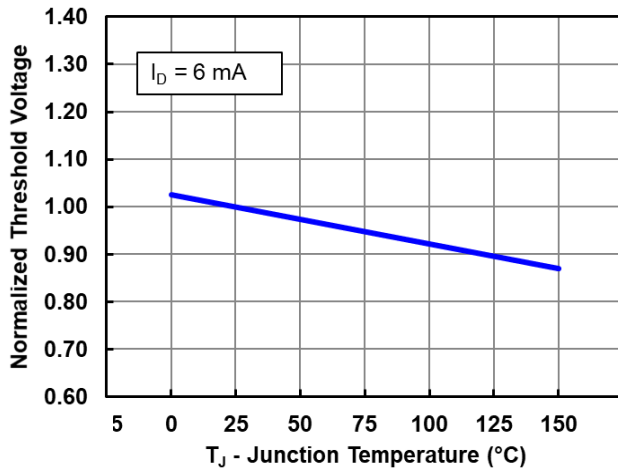
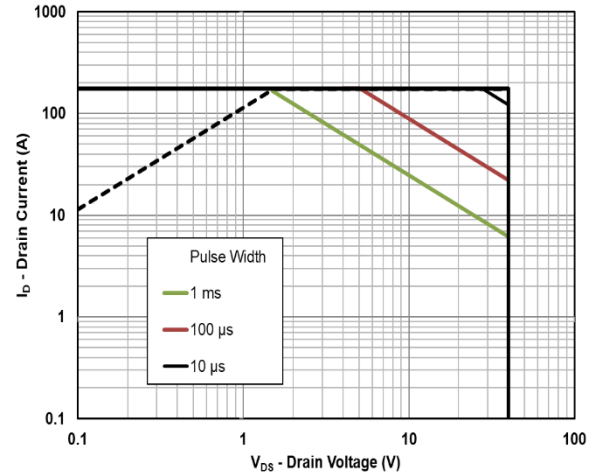


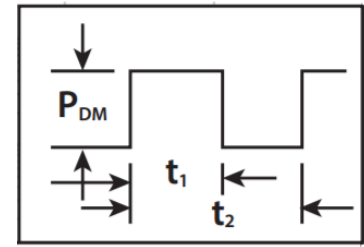
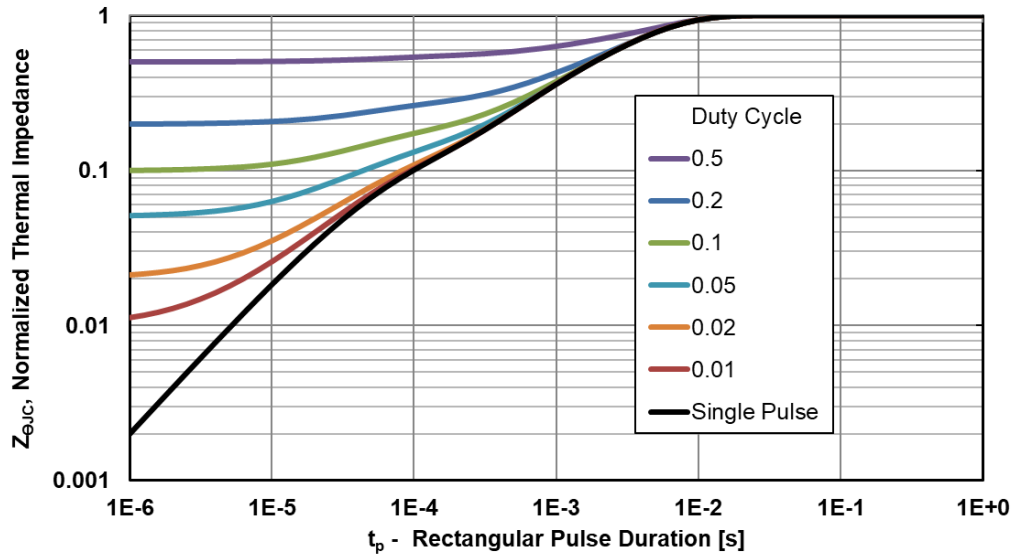
Figure 10: Safe Operating Area



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Figure 11a: Transient Thermal Response Curves (Junction-to-Case)

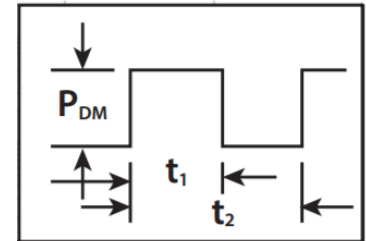
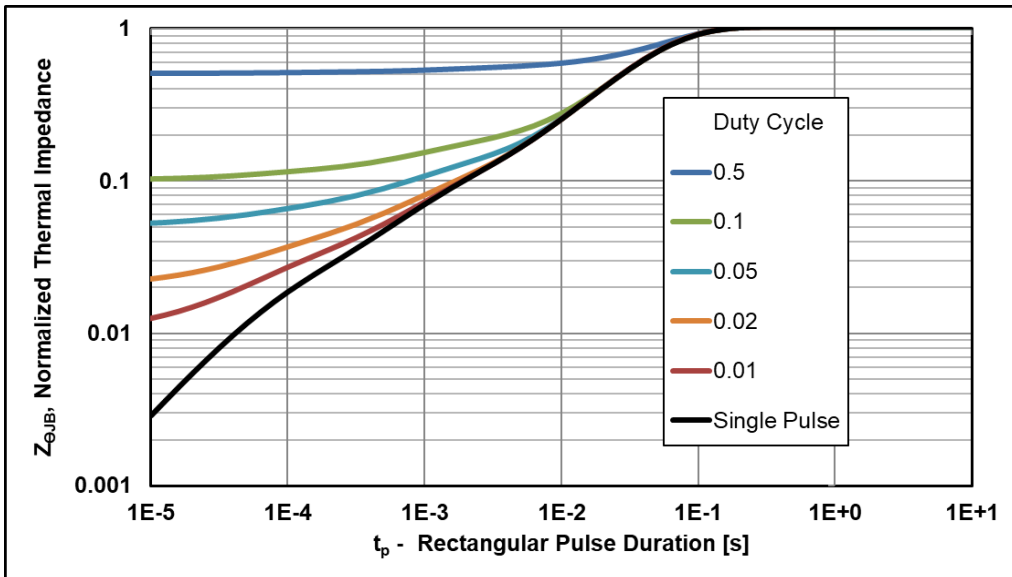


Notes:

Duty Factor: $D = t_1/t_2$

Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 11b: Transient Thermal Response Curves (Junction-to-Board)



Notes:

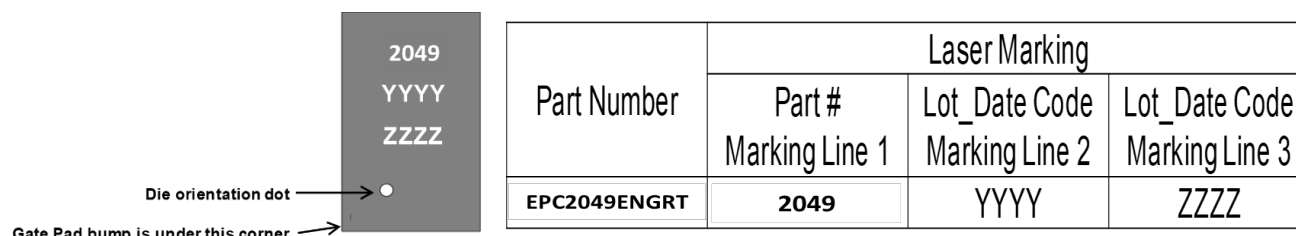
Duty Factor: $D = t_1/t_2$

Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

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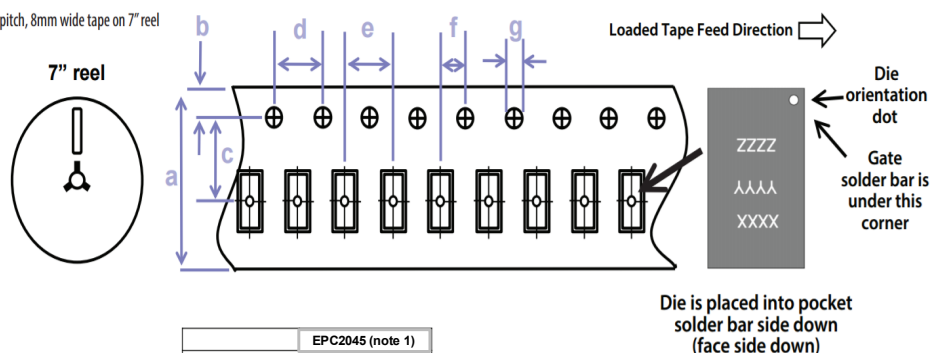
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DIE MARKINGS



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

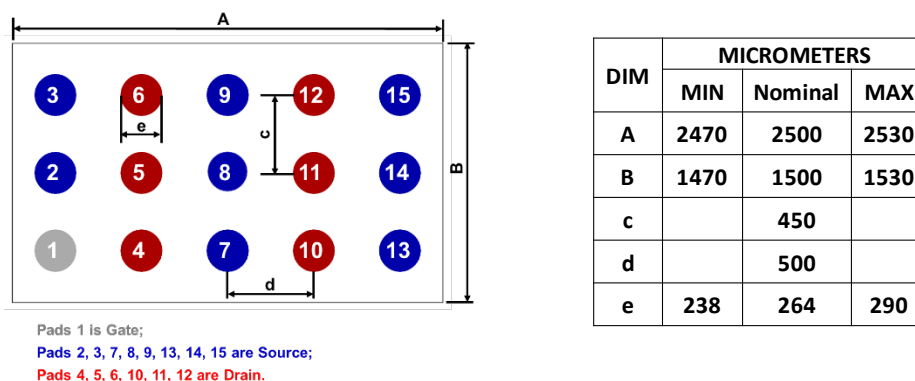


EPC2045 (note 1)			
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

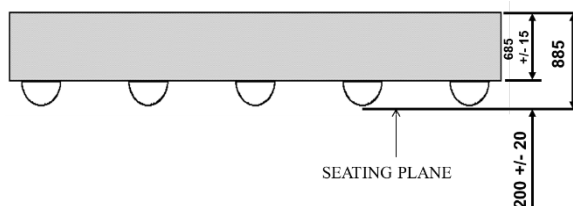
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE OUTLINE

Solder Bar View



Side View

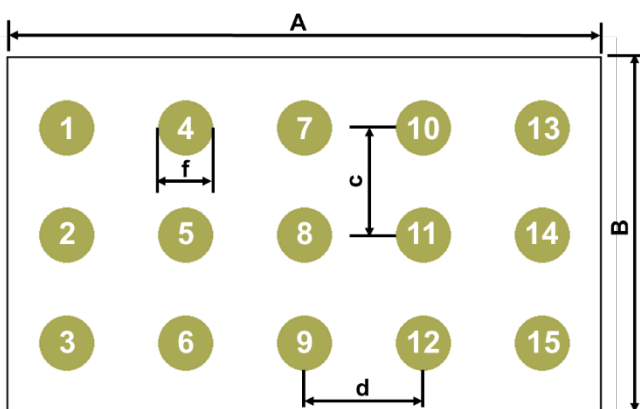


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RECOMMENDED LAND PATTERN

(measurements in μm)



The land pattern is solder mask defined
Solder mask is $10\mu\text{m}$ smaller per side than bump

DIM	MICROMETERS
A	2500
B	1500
c	450
d	500
f	230

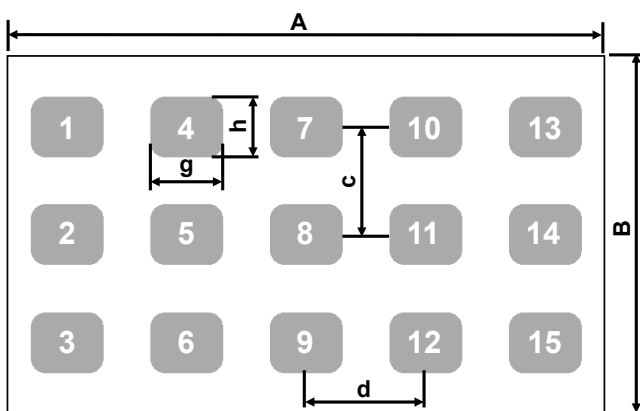
Pads 1 is Gate;

Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

Pads 4, 5, 6, 10, 11, 12 are Drain.

RECOMMENDED STENCIL DRAWING

(measurements in μm)



DIM	MICROMETERS
A	2500
B	1500
c	450
d	500
g	300
h	250

Recommended stencil should be 4mil ($100\mu\text{m}$) thick, must be laser cut, openings per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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