EPC8009 – Enhancement Mode Power Transistor

**V\_DS**, 65 V

**R\_DS(on)**, 130 mΩ

**I\_D**, 4 A

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low R\_DS\_on, while its lateral device structure and majority carrier diode provide exceptionally low Q\_G and zero Q\_RR. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

### Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DS (Drain-to-Source Voltage)</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>Continuous (up to 10,000 pulses)</td>
<td>78</td>
<td>V</td>
</tr>
<tr>
<td>I_D (Continuous, 25°C)</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed (25°C, T_PULSE = 300 µs)</td>
<td>7.5</td>
<td>A</td>
</tr>
<tr>
<td>V_GS (Gate-to-Source Voltage)</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>T_J (Operating Temperature)</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>T_STG (Storage Temperature)</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Static Characteristics (\(T\_J = 25°C\) unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>B_V_DSS (Drain-to-Source Voltage)</td>
<td>V_GS = 0 V, I_D = 125 µA</td>
<td>65</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_DSS (Drain-Source Leakage)</td>
<td>V_DS = 52 V, V_GS = 0 V</td>
<td>50</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_GSS (Gate-to-Source Forward Leakage)</td>
<td>V_GS = 5 V</td>
<td>100</td>
<td>500</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_GS(TH) (Gate-to-Source Reverse Leakage)</td>
<td>V_GS = -4 V</td>
<td>50</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>V_GS_TH (Gate Threshold Voltage)</td>
<td>V_DS = V_GS, I_D = 0.25 mA</td>
<td>0.8</td>
<td>1.4</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>R_D_S_on (Drain-Source On Resistance)</td>
<td>V_GS = 5 V, I_D = 0.5 A</td>
<td>90</td>
<td>130</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>V_SD (Source-Drain Forward Voltage)</td>
<td>I_S = 0.5 A, V_GS = 0 V</td>
<td>2.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Specifications are with substrate shorted to source where applicable.

### Thermal Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_JC (Thermal Resistance, Junction-to-Case)</td>
<td>8.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_J_JB (Thermal Resistance, Junction-to-Board)</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>R_J_A (Thermal Resistance, Junction-to-Ambient)</td>
<td>82</td>
<td></td>
</tr>
</tbody>
</table>

Note: R\_J\_A is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
### Dynamic Characteristics (Tj = 25°C unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{GS}</td>
<td>Input Capacitance</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{DS}</td>
<td>Output Capacitance</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{RSS}</td>
<td>Reverse Transfer Capacitance</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_{G}</td>
<td>Gate Resistance</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Q_{G}</td>
<td>Total Gate Charge</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
<tr>
<td>Q_{GS}</td>
<td>Gate-to-Source Charge</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
<tr>
<td>Q_{GD}</td>
<td>Gate-to-Drain Charge</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
<tr>
<td>Q_{G(TH)}</td>
<td>Gate Charge at Threshold</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
<tr>
<td>Q_{RSS}</td>
<td>Output Charge</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
<tr>
<td>Q_{RR}</td>
<td>Source-Drain Recovery Charge</td>
<td></td>
<td></td>
<td></td>
<td>pC</td>
</tr>
</tbody>
</table>

Specifications are with substrate shorted to source where applicable.

---

**Figure 1:** Typical Output Characteristics at 25°C

- **V_{GS} = 5 V**
- **V_{GS} = 4 V**
- **V_{GS} = 3 V**
- **V_{GS} = 2 V**

**Figure 2:** Transfer Characteristics

- 25°C
- 125°C

**Figure 3:** R_{DS(on)} vs. V_{GS} for Various Drain Currents

- I_{D} = 0.5 A
- I_{D} = 1.0 A
- I_{D} = 1.5 A
- I_{D} = 2.0 A

**Figure 4:** R_{DS(on)} vs. V_{GS} for Various Temperatures

- 25°C
- 125°C

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Figure 5: Capacitance (Linear Scale)

\[ V_{DS} - \text{Drain-to-Source Voltage (V)} \]
\[ C - \text{Capacitance (pF)} \]
\[ C_{oss} = C_{gd} + C_{sd} \]
\[ C_{iss} = C_{gd} + C_{gs} \]
\[ C_{rss} = C_{gd} \]

Figure 5A: Capacitance (Log Scale)

\[ V_{DS} - \text{Drain-to-Source Voltage (V)} \]
\[ C - \text{Capacitance (pF)} \]
\[ C_{oss} = C_{gd} + C_{sd} \]
\[ C_{iss} = C_{gd} + C_{gs} \]
\[ C_{rss} = C_{gd} \]

Figure 6: Gate Charge

\[ Q_G - \text{Gate Charge (pC)} \]
\[ V_G - \text{Gate Voltage (V)} \]
\[ I_D = 1 \text{ A} \]
\[ V_{DS} = 32.5 \text{ V} \]

Figure 7: Reverse Drain-Source Characteristics

\[ V_{SD} - \text{Source-to-Drain Voltage (V)} \]
\[ I_{SD} - \text{Source-to-Drain Current (A)} \]
\[ 25 \degree C \]
\[ 125 \degree C \]

Figure 8: Normalized \( R_{DS(on)} \)

\[ I_D = 1 \text{ A} \]
\[ V_{GS} = 5 \text{ V} \]

Figure 9: Normalized Threshold Voltage vs. Temperature

\[ I_D = 0.25 \text{ mA} \]
**Figure 10: Gate Current**

- **$V_{GS}$ – Gate-to-Source Voltage (V)**
- **$I_g$ – Gate Current (mA)**

- **Red line**: 25°C
- **Blue line**: 125°C

All measurements were done with substrate shortened to source.

**Figure 11: Smith Chart**

*S-Parameter Characteristics*

- $V_{DSQ} = 30$ V, $I_{DSQ} = 0.50$ A
- Pulsed Measurement, Heat-Sink Installed, $Z_0 = 50 \, \Omega$

**Figure 12: Gain Chart**

- **Amplitude [dB]**
- **Frequency (MHz)**

**Figure 13: Device Reflection**

- $S_{11}$ – Gate Reflection
- $S_{22}$ – Drain Reflection

**Figure 14: Taper and Reference Plane details – Device Connection**

- Micro-Strip design: 2-layer
- ½ oz (17.5 µm) thick copper
- 30 mil thick RO4350 substrate

<table>
<thead>
<tr>
<th>Frequency [MHz]</th>
<th>Gate ($Z_{GS}$)</th>
<th>Drain ($Z_{DP}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>1.98 – j8.58</td>
<td>16.83 – j11.29</td>
</tr>
<tr>
<td>500</td>
<td>1.87 – j2.15</td>
<td>10.69 – j9.69</td>
</tr>
<tr>
<td>1000</td>
<td>1.39 + j2.14</td>
<td>5.22 – j5.45</td>
</tr>
<tr>
<td>1200</td>
<td>1.21 + j3.56</td>
<td>3.53 – j3.42</td>
</tr>
<tr>
<td>1500</td>
<td>1.01 + j4.96</td>
<td>2.35 – j0.81</td>
</tr>
<tr>
<td>2000</td>
<td>0.83 + j7.83</td>
<td>1.57 + j3.52</td>
</tr>
<tr>
<td>2400</td>
<td>0.73 + j10.14</td>
<td>1.54 + j6.19</td>
</tr>
<tr>
<td>3000</td>
<td>0.58 + j14.27</td>
<td>1.84 + j10.20</td>
</tr>
</tbody>
</table>

*S-Parameter Table - Download S-parameter files at www.epc-co.com*
Figure 15: Transient Thermal Response Curves

**Junction-to-Board**

- Duty Factors: 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- Normalized Thermal Impedance
- Single Pulse

**Junction-to-Case**

- Duty Factors: 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- Normalized Thermal Impedance
- Single Pulse

Notes:
- Duty Factor = \( \frac{t_p}{T} \)
- Peak \( T_J = P_{DM} \times Z_{\theta_{JB}} \times R_{\theta_{JB}} + T_J \)
- \( t_p \) = Rectangular Pulse Duration (s)
- \( T \) = Total Duration (s)
- \( P_{DM} \) = Power Density

Figure 16: Safe Operating Area

- \( I_D \) = Drain Current (A)
- \( V_{DS} \) = Drain Voltage (V)
- Pulse Width (s)
- Duty Factors: 100 ms, 10 ms, 1 ms, 100 µs
### TAPE AND REEL CONFIGURATION
4mm pitch, 8mm wide tape on 7” reel

![Diagram of TAPE AND REEL CONFIGURATION](image)

<table>
<thead>
<tr>
<th>Dimension (mm)</th>
<th>target</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>8.00</td>
<td>7.90</td>
<td>8.30</td>
</tr>
<tr>
<td>b</td>
<td>1.75</td>
<td>1.65</td>
<td>1.85</td>
</tr>
<tr>
<td>c (see note)</td>
<td>3.50</td>
<td>3.45</td>
<td>3.55</td>
</tr>
<tr>
<td>d</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>e</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>f (see note)</td>
<td>2.00</td>
<td>1.95</td>
<td>2.05</td>
</tr>
<tr>
<td>g</td>
<td>1.5</td>
<td>1.5</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

### DIE MARKINGS

![Diagram of DIE MARKINGS](image)

- Die orientation dot
- Gate Pad bump is under this corner

#### Laser Markings

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Laser Markings</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC8009</td>
<td>Part # Marking Line 1</td>
</tr>
<tr>
<td></td>
<td>EPC8009</td>
</tr>
</tbody>
</table>

### DIE OUTLINE

**Solder Bar View**

![Diagram of DIE OUTLINE](image)

**Side View**

- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate

**Seating Plane**

- 100 +/-20
- 855 Max
- (685)
**RECOMMENDED LAND PATTERN**
*(measurements in µm)*

The land pattern is solder mask defined. Solder mask opening is 5 µm smaller per side than bump.

**RECOMMENDED STENCIL DRAWING**
*(measurements in µm)*

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at:

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