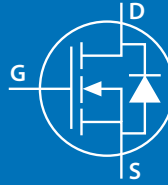


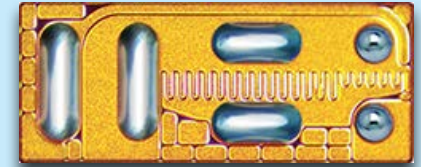
## EPC8009 – Enhancement Mode Power Transistor

 $V_{DS}$ , 65 V $R_{DS(on)}$ , 130 m $\Omega$  $I_D$ , 4 A

Revised July 7, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:  
Ask a GaN  
Expert



Die size: 2.1 x 0.85 mm

EPC8009 eGaN FETs are supplied only in passivated die form with solder bars.

Maximum Ratings			
PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	65	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 125°C)	78	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 33^\circ\text{C/W}$ )	4	A
	Pulsed (25°C, $T_{PULSE} = 300 \mu\text{s}$ )	7.5	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	82	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 125 \mu\text{A}$	65			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 52 \text{ V}$		50	100	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		100	500	$\mu\text{A}$
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		50	100	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 0.25 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 0.5 \text{ A}$		90	130	m $\Omega$
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$V_{GS} = 0 \text{ V}$ , $I_S = 0.5 \text{ A}$		2.2		V

<sup>#</sup> Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Specifications are with substrate connected to source where applicable.

**Applications**

- Ultra high speed DC-DC conversion
- RF envelope tracking
- Wireless power transfer
- Game console and industrial movement sensing (Lidar)

**Benefits**

- Ultra high efficiency
- Ultra low  $R_{DS(on)}$
- Ultra low  $Q_G$
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC8009>

Dynamic Characteristics# (T <sub>j</sub> = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32.5 V		45	52	pF
C <sub>OSS</sub>	Output Capacitance			19	28	
C <sub>RSS</sub>	Reverse Transfer Capacitance			0.5	0.8	
R <sub>G</sub>	Gate Resistance			0.3		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 32.5 V, I <sub>D</sub> = 1 A		370	450	pC
Q <sub>GS</sub>	Gate-to-Source Charge			120		
Q <sub>GD</sub>	Gate-to-Drain Charge			55	94	
Q <sub>G(TH)</sub>	Gate Charge at Threshold			96		
Q <sub>OSS</sub>	Output Charge	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32.5 V		940	1400	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.  
 All measurements were done with substrate connected to source.  
 Specifications are with substrate connected to source where applicable.

Figure 1: Typical Output Characteristics at 25°C

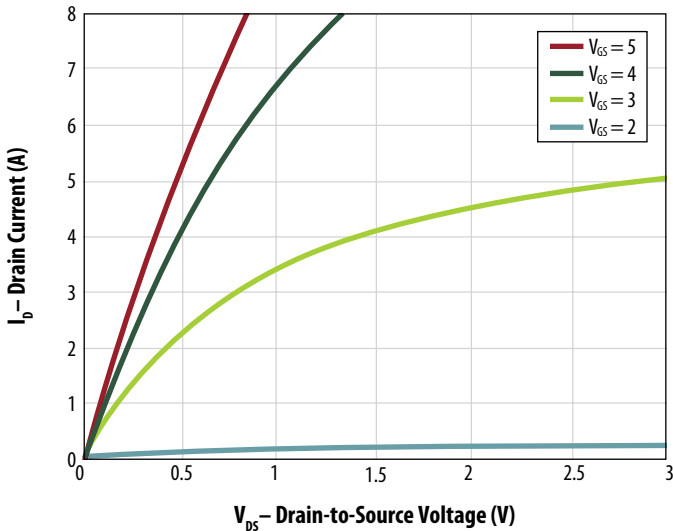


Figure 2: Typical Transfer Characteristics

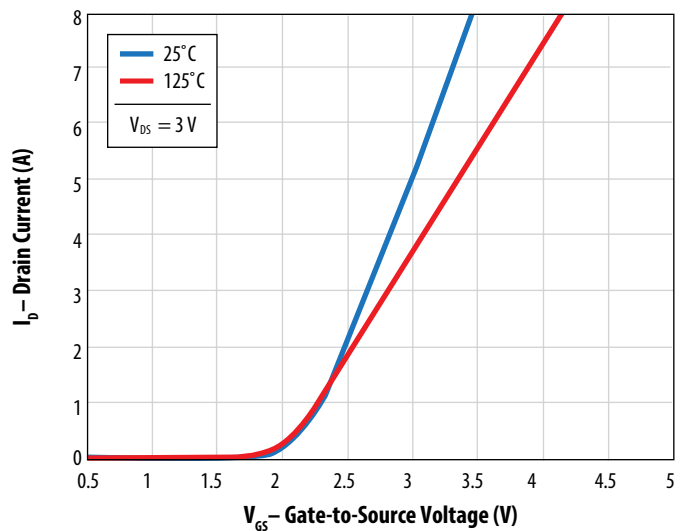


Figure 3: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

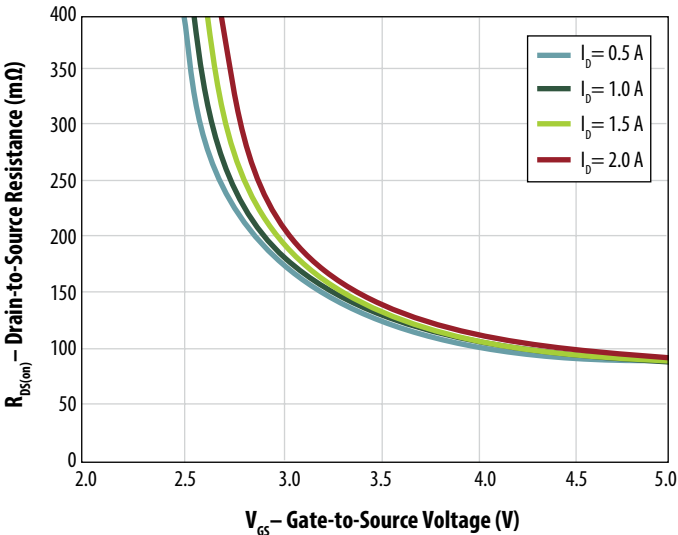


Figure 4: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

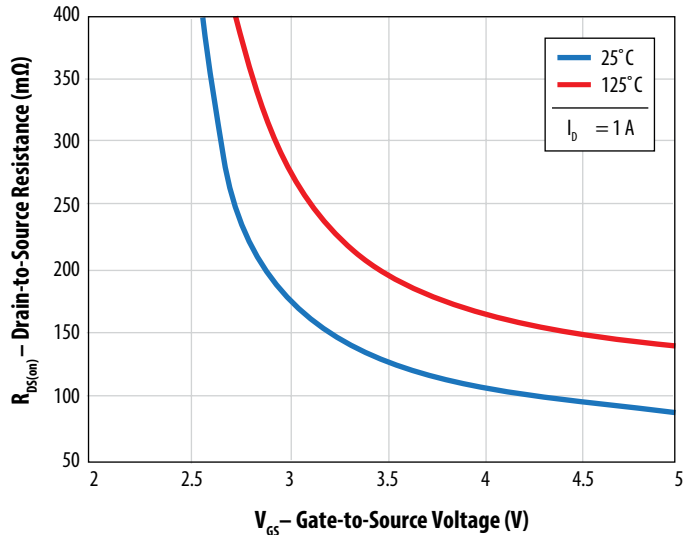


Figure 5: Typical Capacitance (Linear Scale)

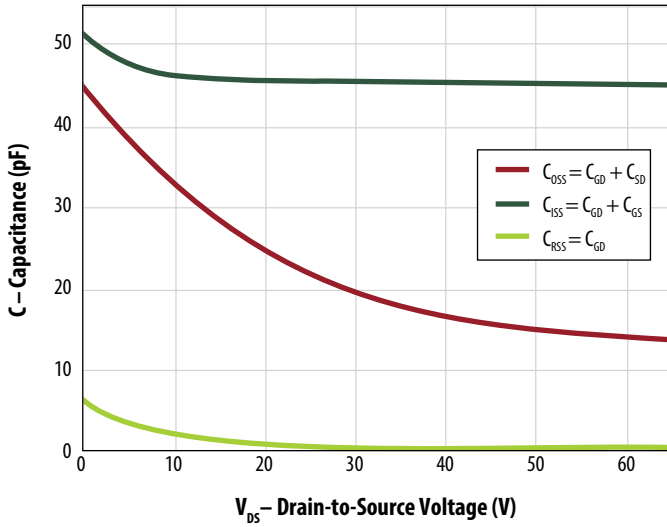


Figure 5A: Typical Capacitance (Log Scale)

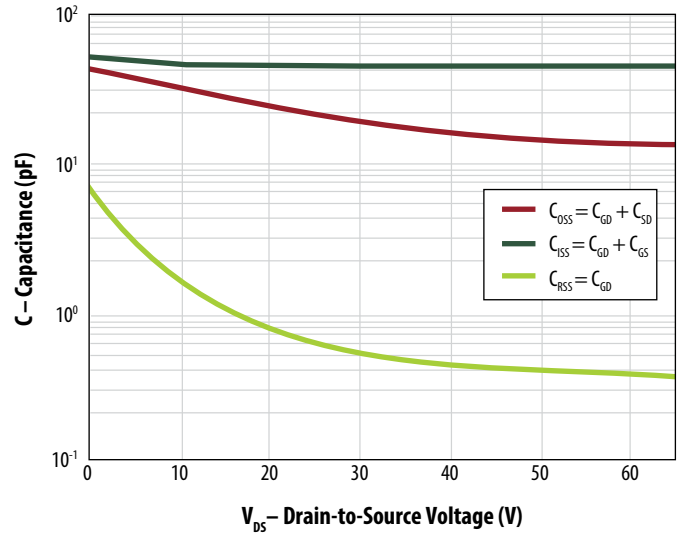


Figure 6: Typical Gate Charge

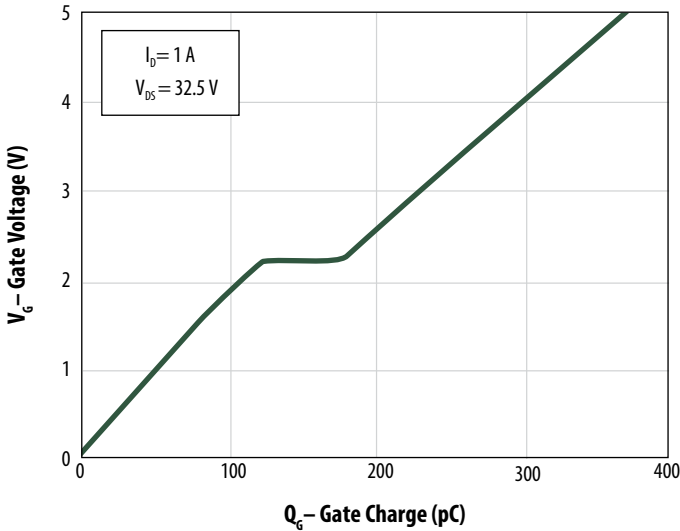
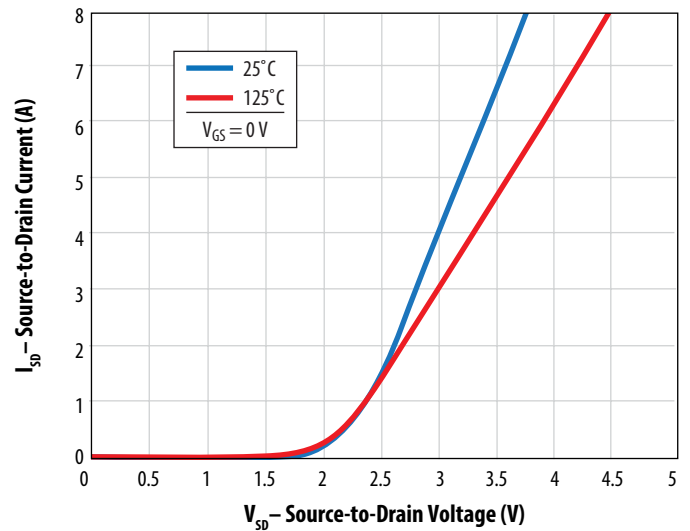


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8: Typical Normalized  $R_{DS(on)}$

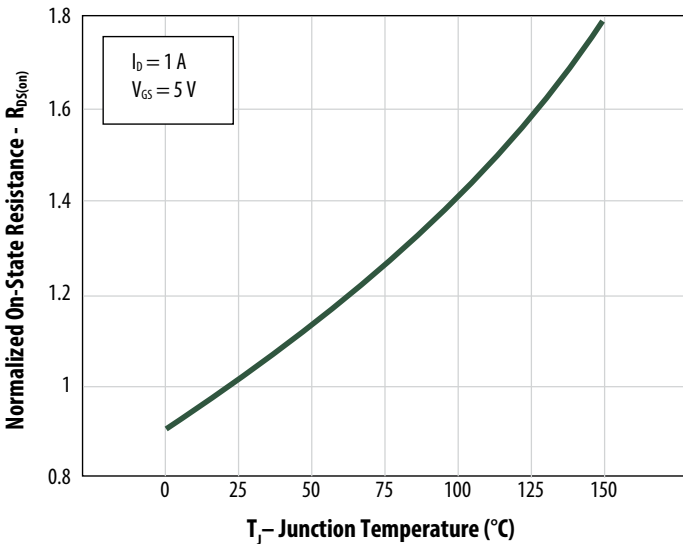


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

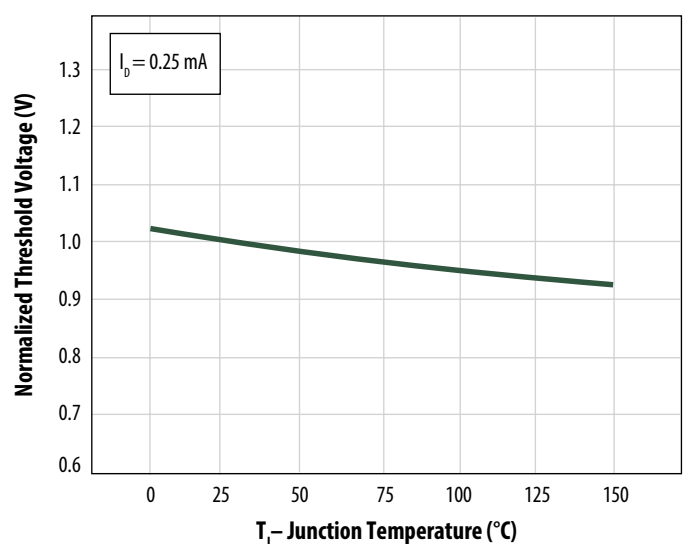


Figure 10: Typical Gate Current

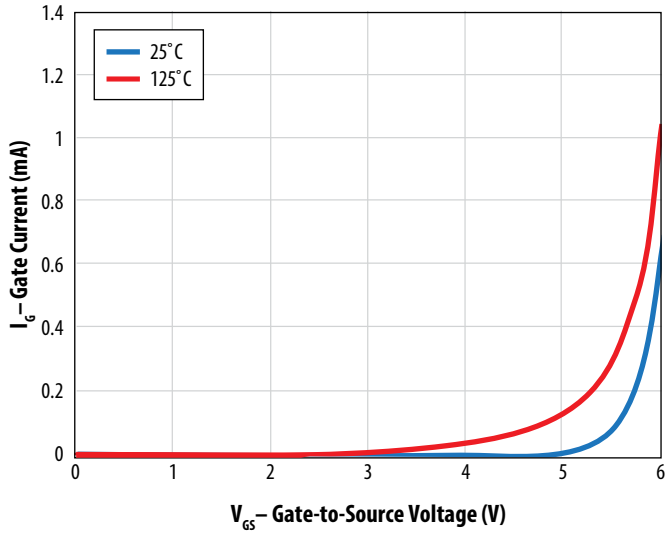


Figure 11: Smith Chart

S-Parameter Characteristics  
 $V_{GS} = 2.36\text{ V}$ ,  $V_{DS} = 30\text{ V}$ ,  $I_{DQ} = 0.50\text{ A}$   
 Pulsed Measurement, Heat-Sink Installed,  $Z_0 = 50\ \Omega$

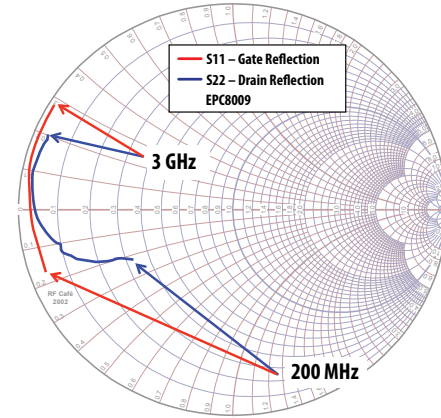


Figure 12: Gain Chart

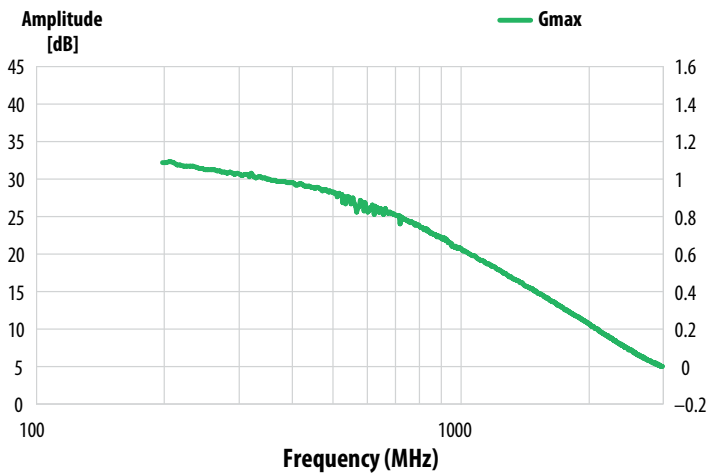


Figure 13: Device Reflection

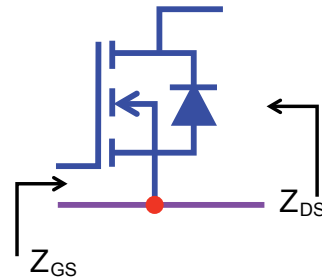
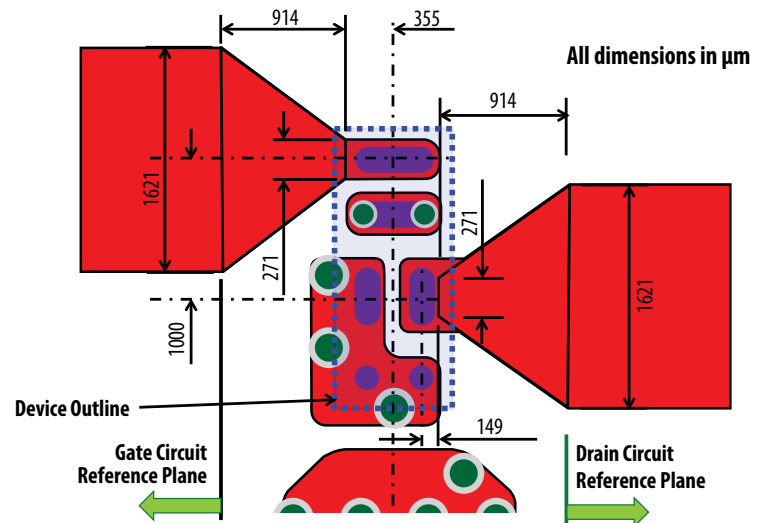


Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer  
 1/2 oz (17.5 μm) thick copper  
 30 mil thick R04350 substrate



Frequency [MHz]	Gate ( $Z_{GS}$ ) [ $\Omega$ ]	Drain ( $Z_{DS}$ ) [ $\Omega$ ]
200	$1.98 - j8.58$	$16.83 - j11.29$
500	$1.87 - j2.15$	$10.69 - j9.69$
1000	$1.39 + j2.14$	$5.22 - j5.45$
1200	$1.21 + j3.56$	$3.53 - j3.42$
1500	$1.01 + j4.96$	$2.35 - j0.81$
2000	$0.83 + j7.83$	$1.57 + j3.52$
2400	$0.73 + j10.14$	$1.54 + j6.19$
3000	$0.58 + j14.27$	$1.84 + j10.20$

S-Parameter Table - Download S-parameter files at [www.epc-co.com](http://www.epc-co.com)

Figure 15: Typical Transient Thermal Response Curves

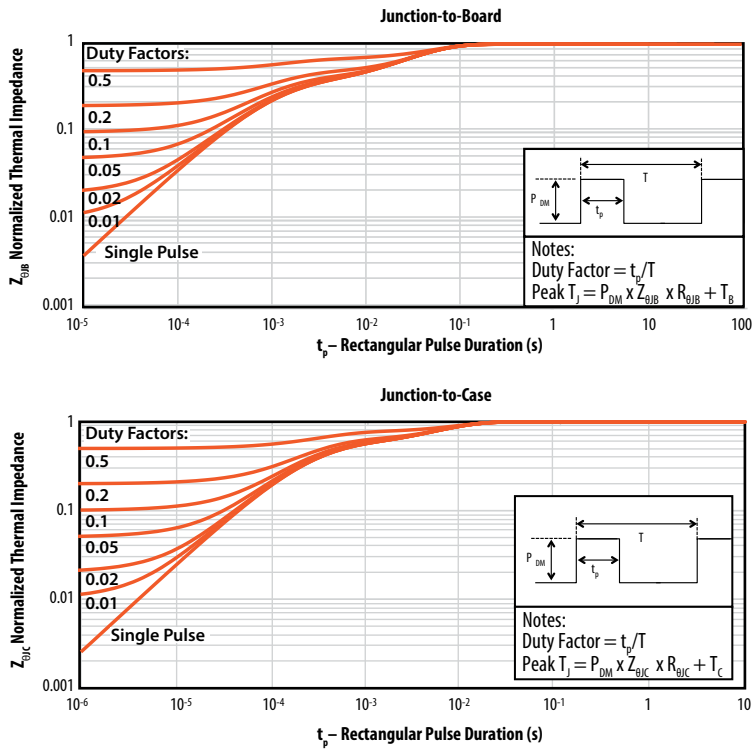
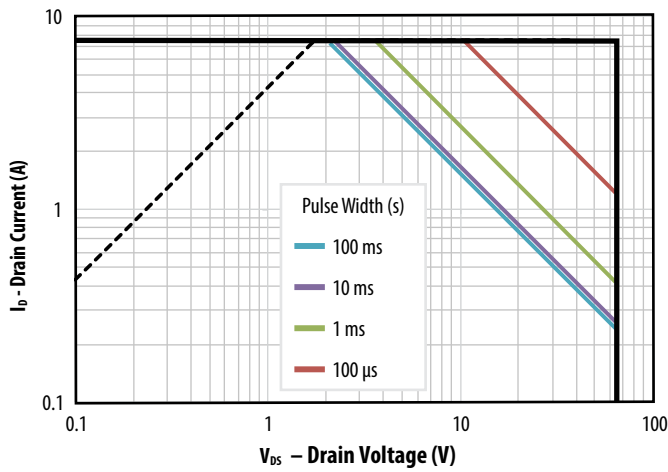
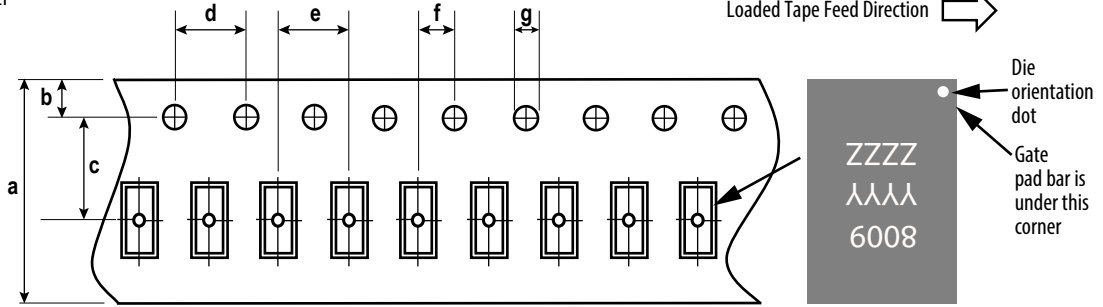
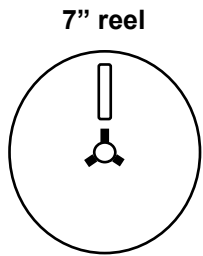


Figure 16: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

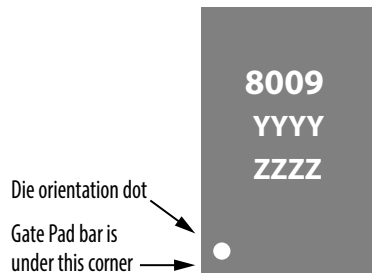


Dimension (mm)	EPC8009 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Die is placed into pocket solder bar side down (face side down)

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

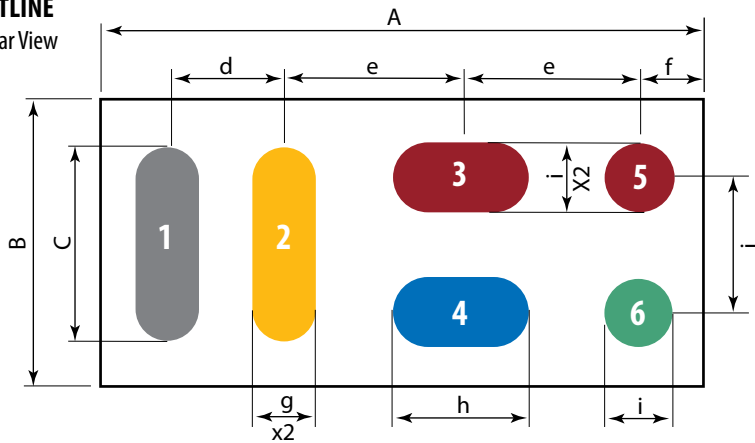
**DIE MARKINGS**



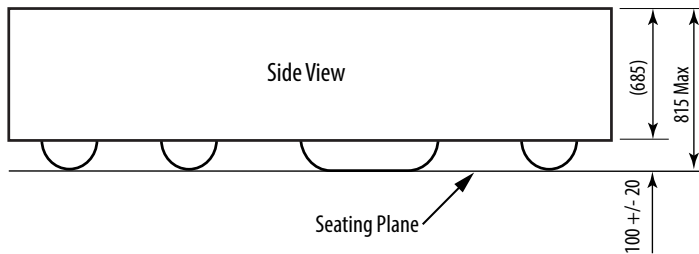
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC8009	8009	YYYY	ZZZZ

**DIE OUTLINE**

Solder Bar View



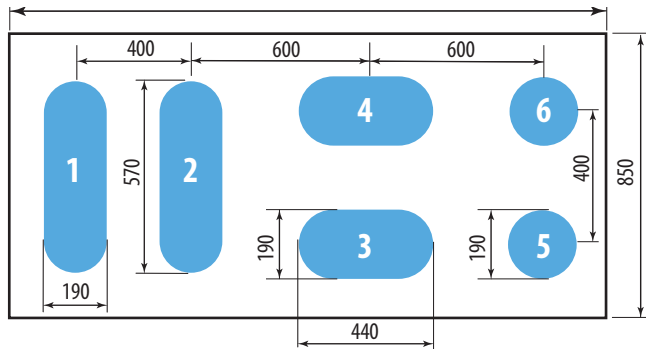
Dim	Micrometers		
	Min	Nominal	Max
A	2020	2050	2080
B	820	850	880
C	555	580	605
d	400	400	400
e	600	600	600
f	200	225	250
g	175	200	225
h	425	450	475
i	175	200	225
j	400	400	400



- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate\*

\*Substrate pin should be connected to Source

**RECOMMENDED LAND PATTERN** (measurements in  $\mu\text{m}$ )

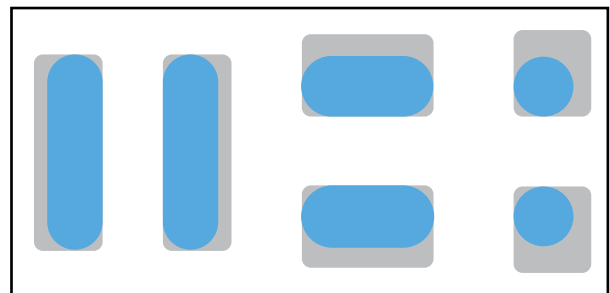
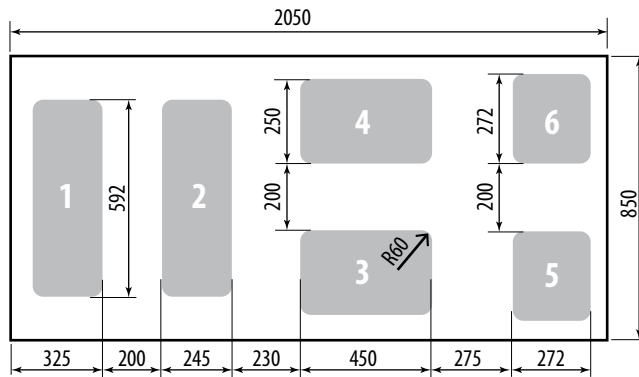


The land pattern is solder mask defined.

- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate\*

\*Substrate pin should be connected to Source

**RECOMMENDED STENCIL DRAWING** (measurements in  $\mu\text{m}$ )



Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: <https://epc-co.com/epc/design-support>

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