Single-Stage 48 V – 1 V DC-DC Conversion Simplifies Power Distribution While Significantly Boosting Conversion Efficiency

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Efficient Power Conversion Corporation's *(EPC) hyper fast Gallium Nitride (GaN) power transistors offer performance enhancements well beyond the realm of silicon-based MOSFETs. Standard power converter topologies can greatly benefit from the added performance and leap to areas not attainable with current MOSFET designs; improving converter efficiency, while maintaining the simplicity of converter designs.*

A 48 V_{DC} to 1 V_{DC} converter using conventional silicon-based power MOSFETS is usually realized in two stages; a preliminary stage that converts the input voltage to a 12 V intermediate voltage, and a point of load (POL) converter that performs the second stage conversion from the intermediate voltage to the required 1 V output. This dual-stage technique is required since a single stage 48 V to 1 V converter will need to operate at a small duty cycle of about 2%. At high frequencies (250 kHz and above) the pulse widths required to operate the converter fall below 100 nsec which is prohibitively short for Silicon based MOSFETs. EPC1001(100 V, 5.6 mΩ) and EPC1007 (100 V, 24 mW) GaN-on-silicon transistors have been shown to operate at pulse widths well below 100 ns. Turn-on and turn-off times of about 4 ns are achieved using an industry standard pin driver.

EPC1001 and EPC1007 Parameter Overview

The EPC1001 and EPC1007 enhancement mode Gallium Nitride power transistors are the first of a new generation of devices that go beyond the limitations of Silicon technology. Whereas similar voltages and $R_{DS(on)}$ can be found in silicon power MOSFETs, the typical gate charge required for switching EPC1001 and EPC1007 devices, 11 nC and 2.7 nC respectively, combined with this voltage and $R_{DS(on)}$ is well beyond silicon's reach. Table 1 compares the capability of these two devices with the benchmark devices on the market today. As can be seen, the product of $R_{DS(on)}$ and Gate Charge ($R_{DS(on)}$ x Q_G product) is six times better than the best performance achieved in silicon.

In addition to the superior $R_{DS(on)}$ x Q_G product, EPC's GaN transistors have an integrated reverse diode with a V_F of about 2 V and no reverse recovery charge.

EPC1001 and EPC1007 transistors are available as bumped "flip-chip" devices. Because of the innovative Gallium-Nitride-on-Silicon technology used by EPC, the substrate is isolated from the active device area by at least 300 V (This parameter is being characterized and may be revised at a future date). This affords an additional opportunity for power density improvements compared with packaged Silicon transistors as the device can be directly connected to a heatsink without an intermediate insulating layer.

Table 1 – Comparison Between EPC1001/EPC1007 GaN Transistors and Silicon Benchmark Devices

Manufacturer	Part Number	Voltage	$R_{DS(on)}$ max	Q_G max	($R_{DS(on)}$ x Q_G)
IR	IRLB4030	100	4.5	130	585
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Fairchild	FDP054N10		5.5	203	1117
Infineon	IPP050N10LG		6.4	163	1043
Fairchild	FDMS86101		8.0	55	440
Infineon	IPD068N10N3G		12.3	68	836
IR	IRLR3110ZPbF		14.0	48	672
Infineon	BSC159N10LSFG		21.5	35	753
Fairchild	FDMC86102		24.0	18	432
Infineon	BSC205N10LS		28.0	41	1148
Vishay	SUD06N 10-225L		225.0	3	608
EPC	**EPC1001**	**100**	**7**	**11**	**77**
EPC	**EPC1007**		**30**	**2.7**	**81**

In Brief

A first-generation buck converter that delivers high efficiency while converting from 48 V to 1 V_{DC} has been designed and characterized. The use of enhancement mode, Gallium Nitride power transistors from EPC has made this practical for the first time.

- New generation of power transistors outperforms silicon in high frequency switching applications by a wide margin
- Promises to open many new doors to applications previously dominated by power MOSFETs.
- EPC is planning a rapid set of introductions through 2009 and 2010 to cover a broad spectrum of power applications:

– Isolated and non-isolated DC-DC conversion
– Synchronous rectification
– Class-D Audio
– Motion control
– Cell phones and base stations

EPC1001 and EPC1007 Gate Characteristics

The equivalent circuit of the gate characteristics of the GaN power transistor is depicted in Fig 1. The gate consists of a small resistor (R_G ~ 0.5 Ω), and a Capacitor, Q_G, with a breakdown above 6 V_{DC}. Full enhancement of the device channel is achieved by 5 V_{GS} and it is important to maintain a gate drive level that will not exceed the 6 V_{DC} absolute maximum. The EPC1001 required Q_G to turn on is only about 10 nC and EPC1007 requires about 2.7 nC.

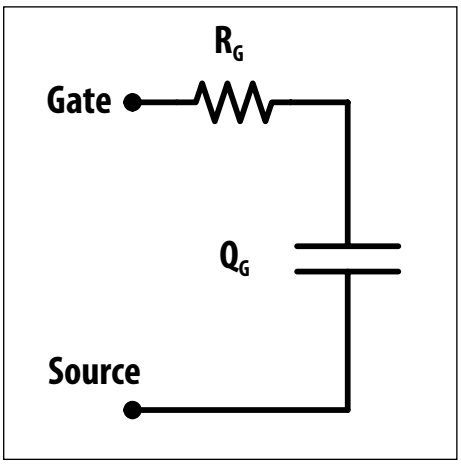

Fig 1 – EPC1001 and EPC1007 Gate Structure

Gate Driver Considerations.

Due to the hyper-fast switching characteristics of the GaN power transistors, high dV/dt's are present when the device switches from one state to another. These high dV/dt's can cause high currents to flow in the miller capacitor (C_{GD}). In a half bridge topology a small driver with a relatively high $R_{DS(on)}$ could cause an undesired turn-on of the lower device when the actual requirement is to keep the device off. This phenomenon will increase the risk of shoot-thru currents and result in excessive losses. Therefore, the selection of a proper driver is not only driven by the current/switching time requirement, but also by the need to provide a low impedance path for stray currents generated by the high dV/dt's.

As an example, with a C_{GD} of ~100 pF and a dV/dt of 12 V/ns, the current injected in the driver equates to about 1.2 A. Since the minimum threshold of the EPC1001 is 0.7 V, the $R_{DS(on)}$ needed to avoid turning the lower device on is:

$R_{DS(on)}$ (Driver) < 0.7 V/1.2 A = 0.58 Ω

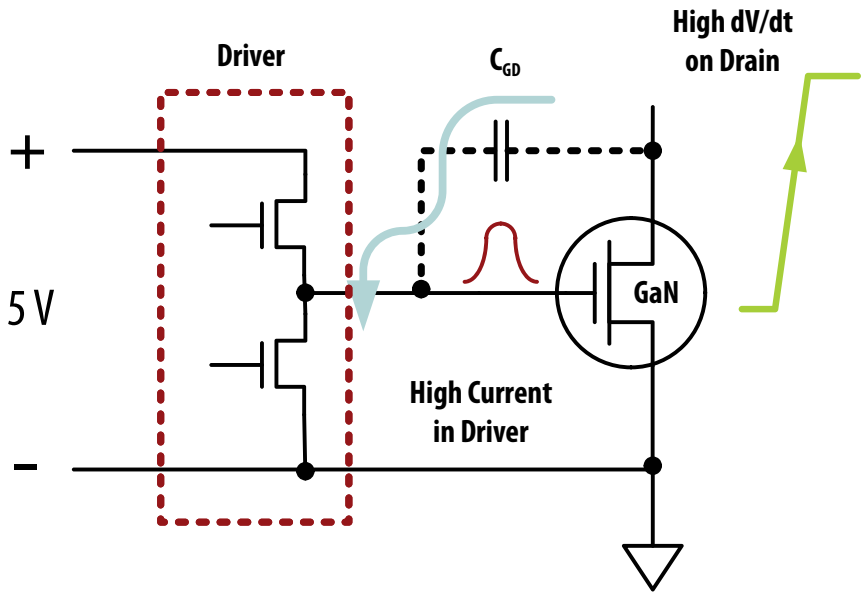

Fig 2 – High dV/dt can cause high currents to flow in the gate driver.

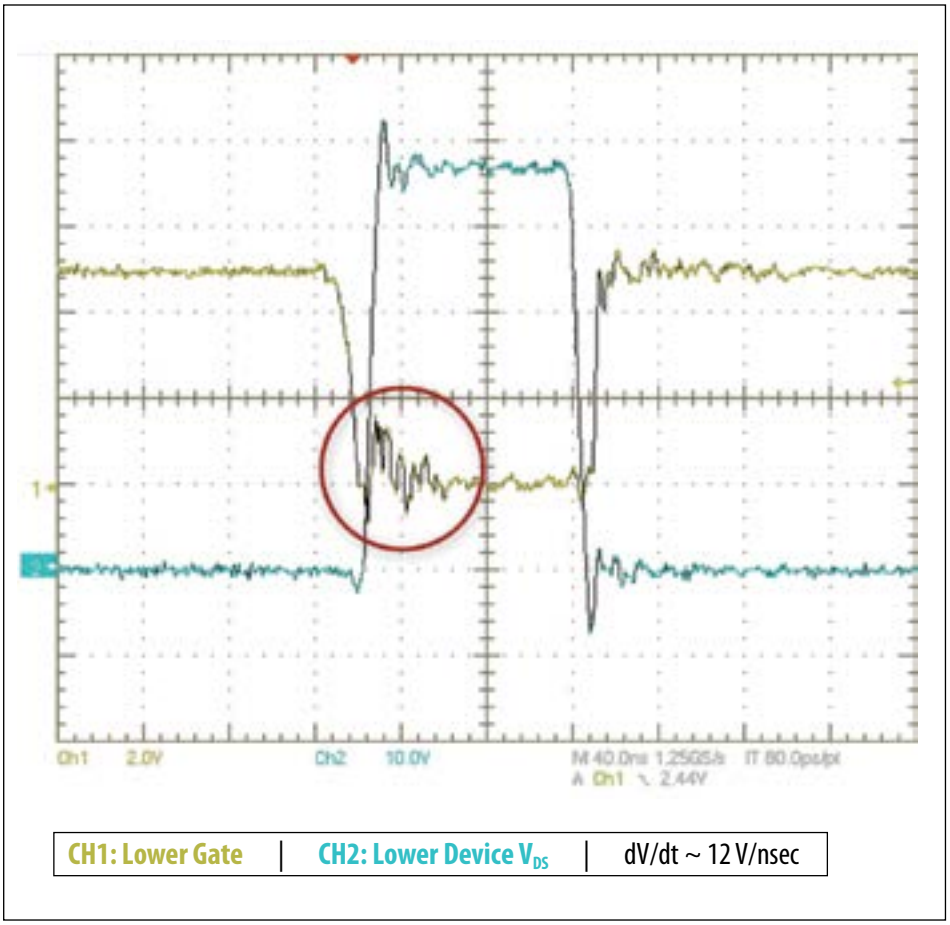

Fig 3 – Half Bridge Topology with high gate drive $R_{DS(on)}$ – High dV/dt causes "Bump" in Lower gate drive.

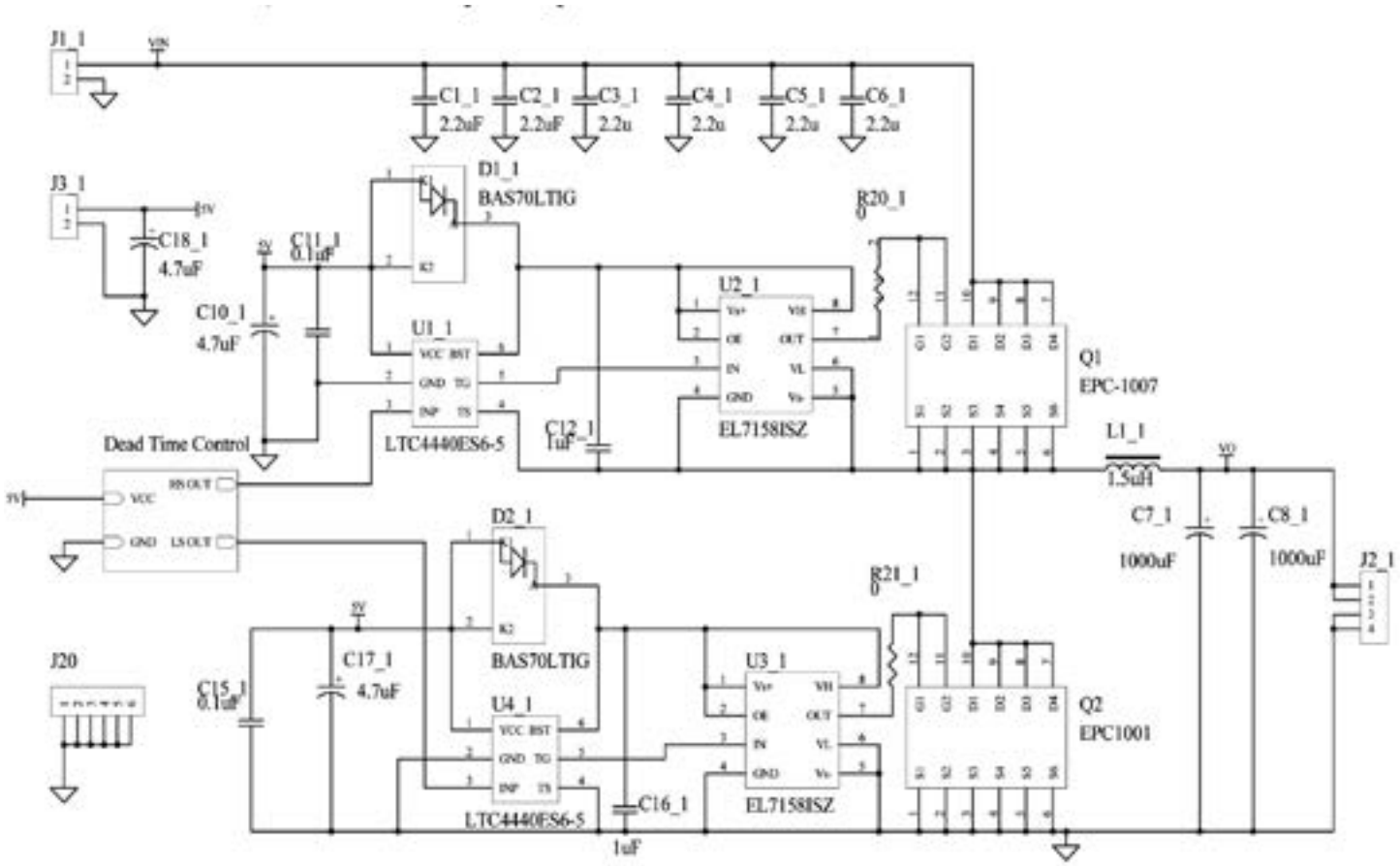

Fig 4a – Schematic of EPC1001/EPC1007 Evaluation Circuit

EPC1001/EPC1007 Evaluation Circuit

The EPC1001/EPC1007 evaluation circuit is a non-isolated "buck" converter capable of operating with up to 72 V_{DC} input, while generating 0.5 to 3.5 V_{DC} output at up to 15 A. A function generator is required to set the PWM pulses for various output voltages and current combinations. Dead time adjustments are accomplished by two on-board potentiometers to optimize performance vs. various dead time settings. The EPC transistors are covered by a detachable heat sink. Due to the internal body diode of the EPC1001, an external re-circulating diode is not necessary.

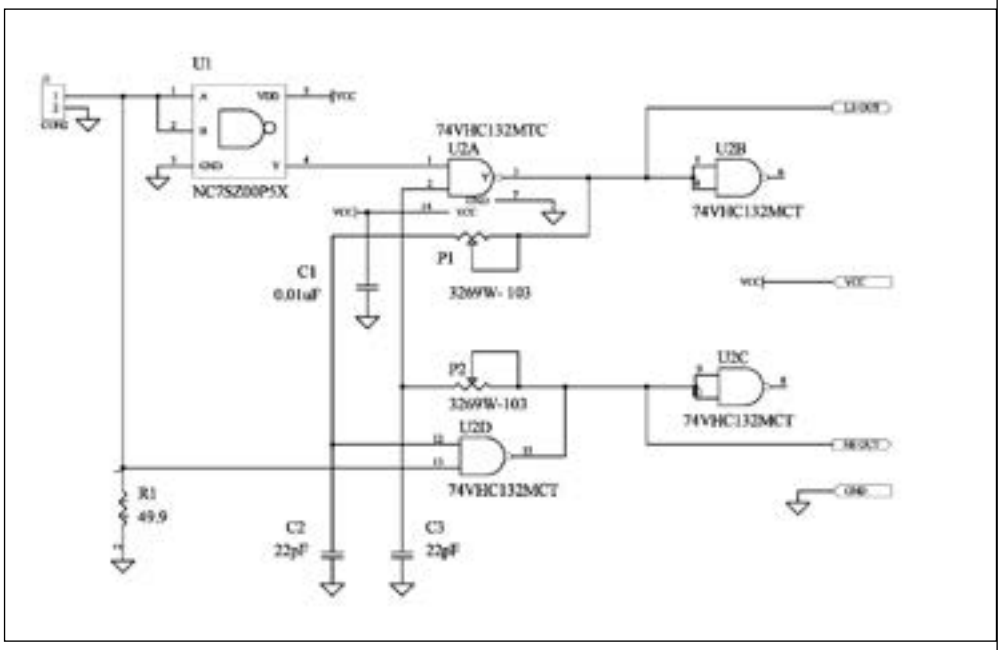

Fig 4b– Schematic of EPC1001/EPC1007 – Dead time generator

EPC1001/ EPC1007 Evaluation Circuit Performance

Typical performance data for the EPC1001/ EPC1007 evaluation circuit has been measured over a range of input voltages, output currents and operating frequencies. Tables 2 and 3, as well as Fig 5, show efficiencies at 24 V_{DC} and 48 V_{DC} to 1 V_{DC} conversion from 2 A to 12 A. All measurements were performed at 250 kHz switching frequency.

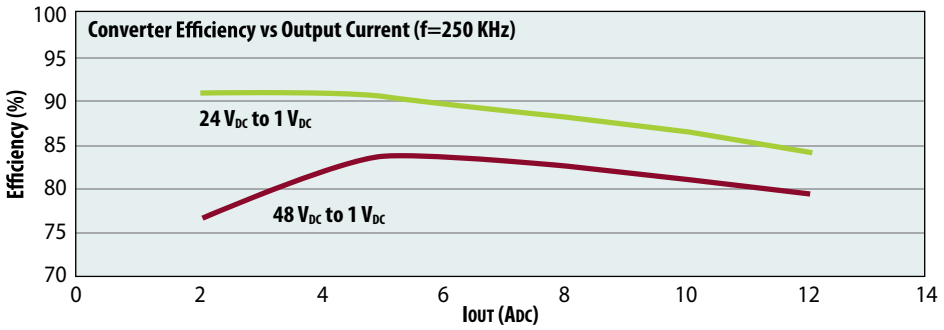

Fig 5 – Converter efficiency vs. input voltage and output current

Table 2 – 48 V_{DC} to 1 V_{DC} conversion

f(kHz)	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT}(A)	% Eff
250	48.06	54.8	1.004	2.0053	76.44
	48.05	126.2	1.004	5.0066	82.89
	48.05	203.8	1.005	8.0079	82.18
	48.04	258.5	1.004	10.006	80.90
	48.03	318	1.005	12.008	79.01

Table 3 – 24 V_{DC} to 1 V_{DC} conversion

f(kHz)	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT}(A)	% Eff
250	24.02	92.58	1.007	2.0053	90.81
	24	231.6	1.006	5.0066	90.61
	23.97	380.6	1.003	8.0079	88.04
	23.97	483.6	1.002	10.006	86.49
	23.96	598.3	1.005	12.008	84.18

Tables 4 and 5 and Fig 6 depict operation of the converter at 24 and 48 V_{DC} inputs over a range of operating frequencies.

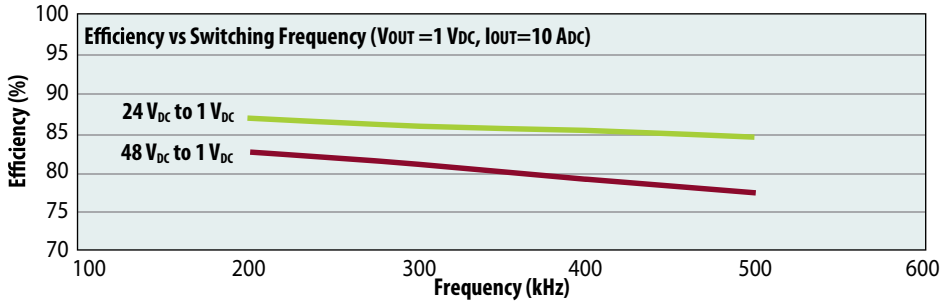

Fig 6 – Converter efficiency vs. switching frequency.

Table 4 – 48 V_{DC} to 1 V_{DC} conversion

f(kHz)	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (A)	% Eff
200	48	252.5	1.001	10.006	82.64
300		258.8	1.005		80.95
400		264.7	1.007		79.30
500		270.3	1.006		77.58

Table 5 – 24 V_{DC} to 1 V_{DC} conversion

f(kHz)	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT}(A)	% Eff
200	23.97	484.7	1.007	10.006	86.73
300		488.1	1.007		86.12
400		492.0	1.006		85.35
500		497.4	1.007		84.51

Fig. 7 shows the loss distribution in the converter for both 24 V and 48 V inputs operating at 250 kHz. Top and bottom device losses include conduction as well as switching losses. Other losses include PCB resistive losses, output capacitor ESR, and parasitic losses due to skin effects and layer to layer capacitances.

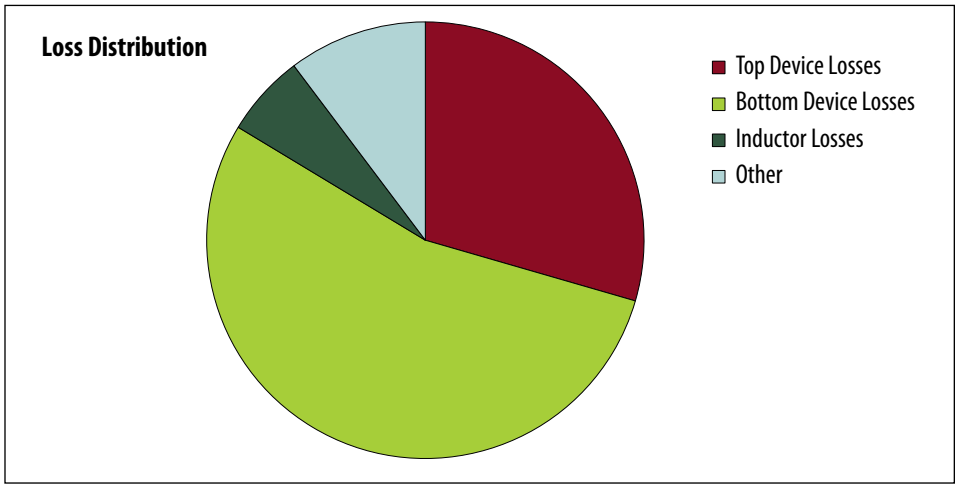

Fig 7 – Distribution of losses in the EPC1001/EPC1007 Evaluation Board (48 or 24 VDC(IN), 1 V/10 AOUT)

Typical Operating Waveforms

Typical waveforms obtained during actual operation are shown in Fig's 8 thru 11. Measurements were performed at 250 kHz operating frequency.

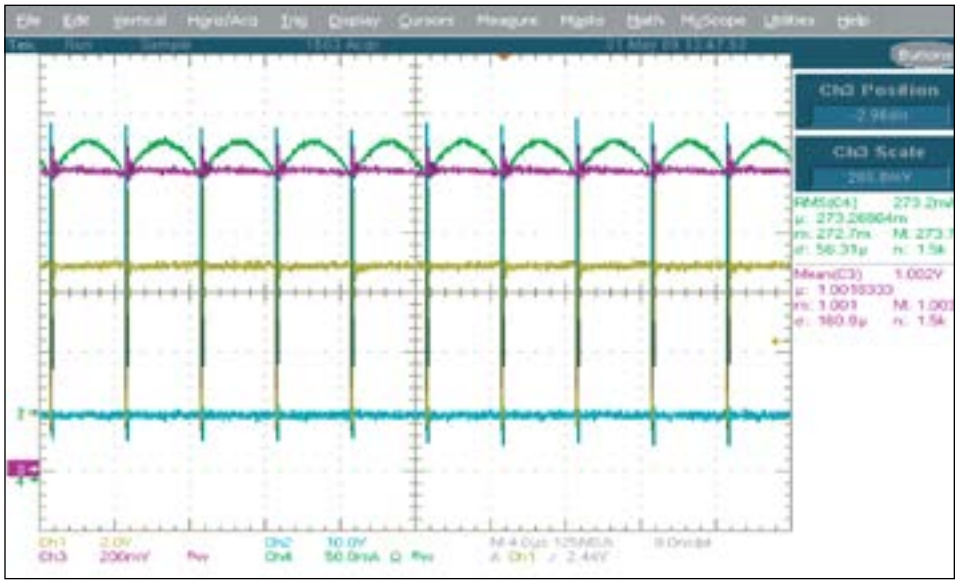

Fig 8 – Overall converter operation (48 VIN, 1 V and 10 AOUT) – 250 kHz

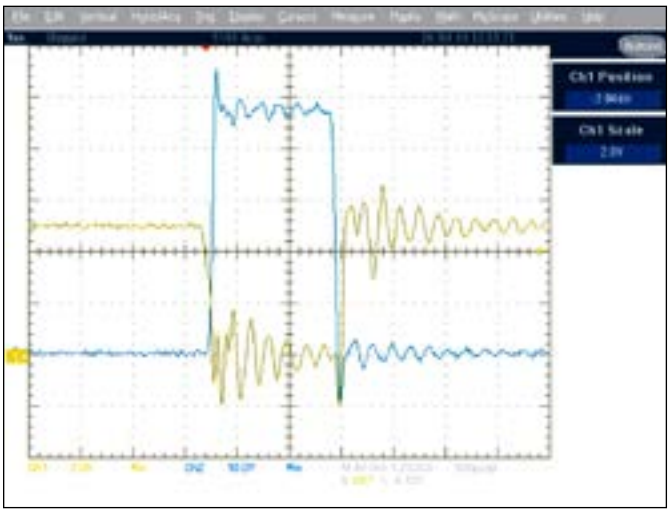

Fig 9 – Low side device gate drive and drain voltage (48 VIN, 1 V and 10 AOUT)

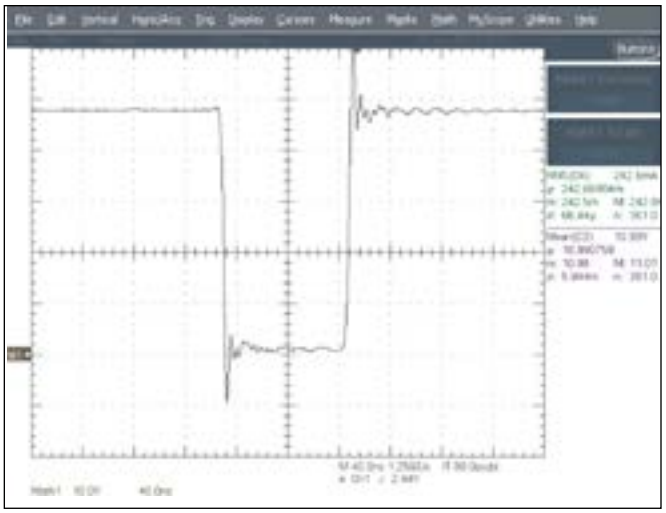

Fig 10 – Top device turn on/off (48 VIN, 1 V and 10 AOUT)

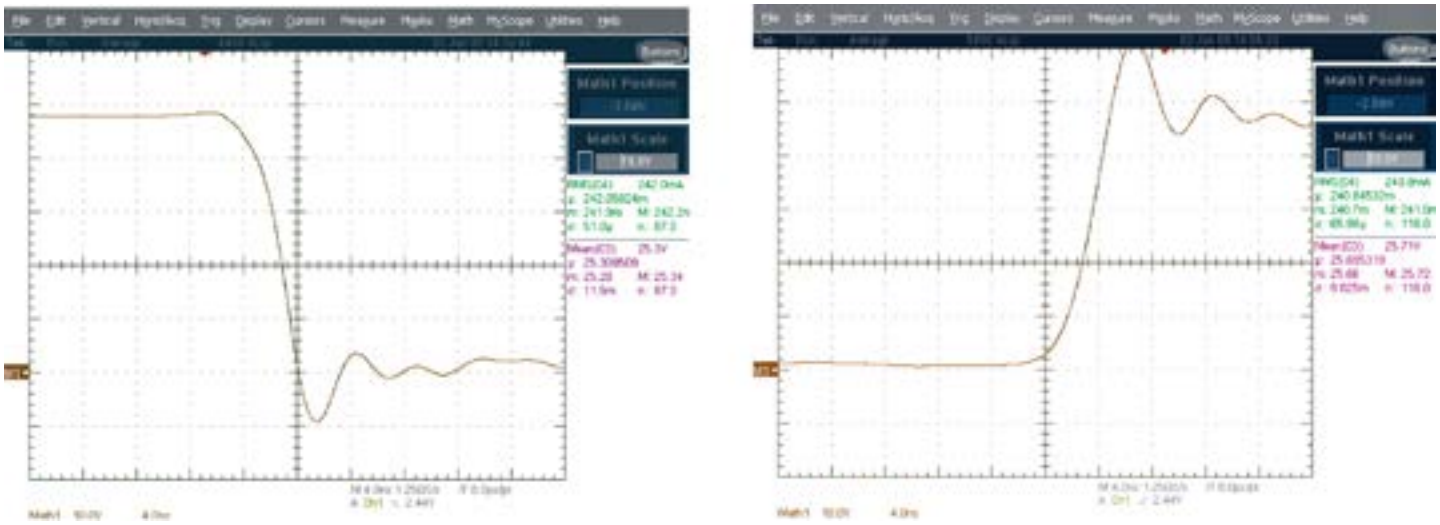

Fig 11 – Top device turn on and turn off times (48 V_{IN}, 1 V and 10 A_{OUT})

Conclusions

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This new generation of power transistors outperforms silicon in high frequency switching applications by a wide margin and promises to open many new doors to applications previously dominated by power MOSFETs.

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