Low-Cost GaN e-mode Transistors and Diodes

Manufactured on an Integrated CMOS-Compatible 8-Inch Platform

Within the power electronics industry, GaN technology is slowly growing out of its niche. The first GaN transistors are winning a small but growing share of the power electronics market. Underpinning this development, a value-chain is developing between R&D cen-ters, substrate providers, device designers and system integrators.

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<Today the market for power devices is still largely dominated by silicon-based designs. But the industry has reached the limits of what it can do with silicon in terms of efficiency and operating frequency. To further improve silicon-based power devices, quite complex 3D architectures are needed.

So the R&D centers and the industry have been looking at alternative materials with better suited properties, such as Silicon Carbide (SiC) or Gallium nitride (GaN) technology. SiC for one, is available only as small diameter and expensive wafers. GaN also is an expen-sive material, but it is possible to grow thin layers of it on inexpensive silicon substrates. And an added advantage is that these wafers may be processed in high-productivity CMOS fabs.

Fabricating suitable large-area substrates, developing a CMOS-compatible flow, and designing superior devices are all considerable challenges. But the outlook is positive, and the growing need for these devices makes for an attractive investment case.

200mm wafers are optimal, but can we make them?
Today, the bulk of the GaN development and fabrication is still done on 6-inch or 4-inch wafers. Considerations of cost efficiency compel us to look at larger wafer sizes, in the first place 8-inch (200mm). But adding to that, the manufacturing platform on 8-inch is much more advanced than on 6-inch or 4-inch. 8-inch equipment is very well supported and innovations developed on 12-inch (300 mm) are in a number of cases even retro-fitted to the 8-inch lines. That means that 8-inch fabrication offers higher productivity, better process control and consequently also a higher yield than smaller wafer sizes.

Imec is one of the R&D centers that has been involved from the start in developing GaN technology. We are one of Europe's premier R&D centers in microelectronics and have actively participated in developing CMOS technology as it is today. We have cleanrooms and state-of-the-art tools for the various wafer formats. So moving GaN from the smaller wafer sizes to 8-inch wafers was a natural step, for which we had the expertise and the tools readily available.

In parallel to our device work on 6-inch wafers, we developed the necessary epitaxy pro-cesses on 8-inch silicon substrates, perfecting the buffer and device layers. The main challenges were growing high-quality, uniform layers, mitigating the stress that develops during the growing processes and controlling the wafer bow. The end result has to be a wafer with extremely uniform device layers that is within the bow specifications that can be handled in the silicon fab.

The stresses that develop are due to the large lattice mismatch between the III-N films (GaN and AlGaN) and the silicon substrate. This has required us to add carefully selected buffer layers between the substrate and the final film, resulting in a wafer bow below ±50µm.

Designing and fabricating devices through collaborative research
With 8-inch wafers ready for 200 fabs added to GaN's superior material properties, it is possible to start designing devices with superior breakdown voltages and lower resistances at a lower price.

To speed up the learning curve and gather all the necessary expertise, imec set up a col-laborative research program. We invited top companies involved in power electronics to do R&D together in imec's world-class 200mm facilities. Today, this partnership includes more than 10 companies setting the specifications and developing this technology. These companies are a mix of device manufacturers, foundries, as well as substrate manufacturers and equipment suppliers.

Our GaN development platform runs on a fully-automated 8 inch pilot line, allowing for fast learning cycles to improve the technology and explore a wide variety of concepts.

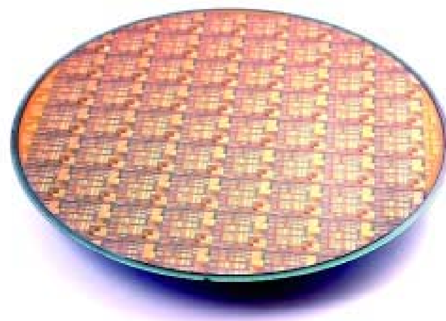

Figure 1: Fully processed 8-inch GaN-on-Si MISHEMT device wafer

We are concentrating on 600V devices, which we think will be a lead driver spec for tech-nology development in power devices. On our test platform we have designed several flavors of devices, which can be tuned towards lower or higher voltages. Some of the companies in our program have a special interest in devices with lower voltage ranges, while a few are looking at voltages going up to 1000 V.

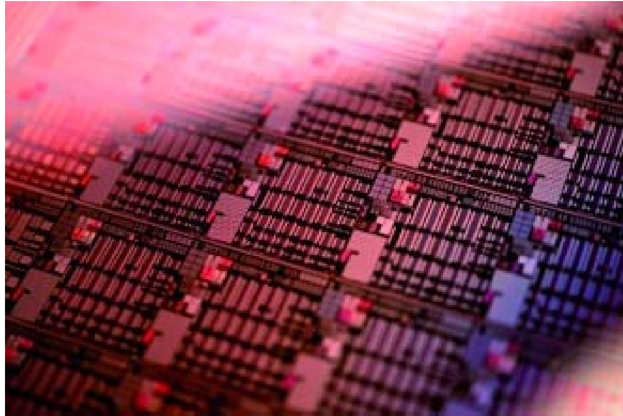

Figure 2: Detail of fully processed MISHEMT device wafer

CMOS compatible processing – access to high-productivity fabs
Our objective is to develop technology that is completely compatible with high-productivity CMOS infrastructure. However, typical GaN device processing requires lift-off metallization schemes using gold (Ni/Au or Mo/Au) to define ohmic and gate contacts. To be compatible, these should be replaced by gold-free metallization schemes, using dry etch patterning instead of lift-off.

However, fabricating gold-free ohmic contacts with a contact resistance below 1.0 ??mm is not straightforward. We have demonstrated a technique that uses AlGaN barrier recess in the ohmic areas, resulting in a contact resistance distribution of 1.25 ± 0.15??mm when leaving ~5 nm AlGaN barrier. We are now investigating how we can further reduce the contact resistance, which is fundamentally important for power devices.

Another concern for CMOS-compatibility is gallium contamination, since gallium is a p-type dopant for silicon. During initial processing test loops on a restricted set of tools, we have observed that the gallium contamination spread from the GaN-on-Si wafers to the transport systems and process chambers of the tools, in most cases exceeding the tolerance limits for gallium contamination. To mitigate this processing contamination, we have developed a cleaning procedure to be applied to the backside of GaN-on-Si wafers. With this procedure, the contamination level is reduced to close to the detection limit.

As a result of these measures and techniques, we can now process GaN-on-Si wafers in between batches of other CMOS development runs, using exactly the same equipment set, without having to make changes. Where we still have to look for further improvements is in the quality of the wafers, in terms of defectivity and uniformity, and also in the throughput of the toolsets. The equipment suppliers in our program are using these development runs as a learning cycle to optimize their hardware for higher throughput and reproducibility.

Making e-mode devices – investigating several approaches
On our platform, we develop both depletion mode and enhancement mode devices. As by nature, GaN power devices are normally-on devices, the challenge is definitely to make enhancement mode, normally-off devices. Our partners in the program have given us the challenge to explore different e-mode architectures side-by-side. That way, they want to identify the one with the highest chance of success that they can transition to manufacturing.

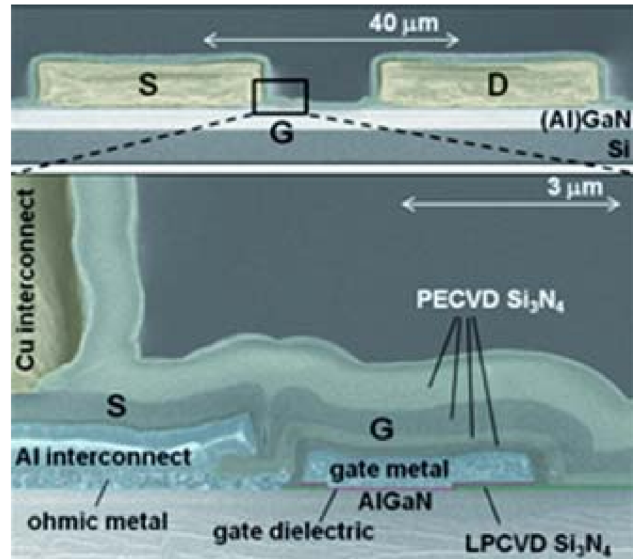

Figure 3: Cross-section SEM pictures of the power device. The top figure shows the source-gate-drain finger configuration, with the 8 µm thick source and drain Cu intercon-nects encapsulated by Si3N4. The bottom picture details the source-gate area: the T-shaped metal gate electrode with the field plate, the gate dielectric, and the metallization stack in the ohmic source area.

Recently, we were able to demonstrate first working e-mode transistors on our 8-inch platform. For these devices, we used a MISHEMT (Metal Insulator Semiconductor High Electron Mobility Transistor) architecture with an isolated gate, to create ultralow leakage GaN transistors. In this architecture, we inserted a gate dielectric between the metal gate electrode and the AlGaN barrier to avoid the creation of a Schottky gate contact, which limits the maximum gate overdrive and reverse leakage current. The maximum output current of these devices is 6 A at VGS = 8 V and VDS = 10 V, which demonstrates the fea-sibility of high current AlGaN/GaN MISHEMT powerbars on 8-inch silicon substrates.

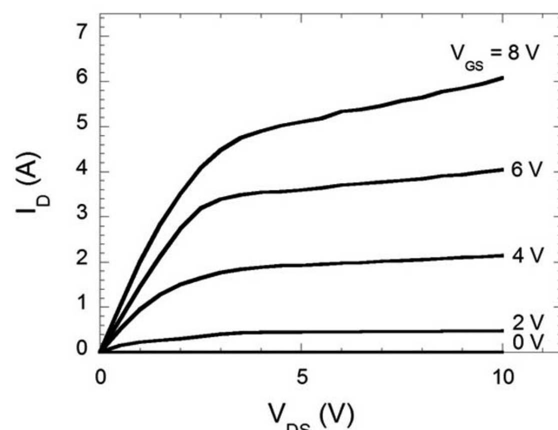

Figure 4: Pulsed ID-VDS output characteristics of an e-mode power device (pulse-width 1 ms), fabricated in our 8-inch technology.