

Evaluation Board EPC9067 Quick Start Guide

65 V Half-Bridge with Sync FET Bootstrap Gate Drive using EPC8009

July 12, 2023

Version 1.0



DESCRIPTION

The EPC9067 evaluation board is a 65 V maximum device voltage, 2.7 A maximum output current, half bridge with onboard gate drives, featuring the EPC8009 enhancement mode (eGaN®) field effect transistor (FET). The gate driver has been configured with a synchronous FET bootstrap circuit featuring the EPC2038 eGaN FET that eliminates high side device losses induced by the reverse recovery losses of the internal bootstrap diode of the gate driver. The purpose of this evaluation board is to simplify the evaluation process of the EPC8009 eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter. The inclusion of the synchronous FET bootstrap circuit enables significant increase in operating frequency capability of the half bridge circuit.

The EPC9067 evaluation board is 2" x 1.5" and has two EPC8009 eGaN FETs in a half bridge configuration using Texas Instruments LM5113 gate driver with supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. The board includes pads for the inclusion of customer components to facilitate testing in a Buck converter or ZVS class-D amplifier configurations. A complete block diagram of the circuit is given in figure 1.

For more information on the EPC8009 and EPC2038 eGaN FETs please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

QUICK START PROCEDURE

Evaluation board EPC9067 is easy to set up to evaluate the performance of the EPC8009 eGaN FET. Refer to figure 2 for proper connect and measurement setup and follow the procedure below:

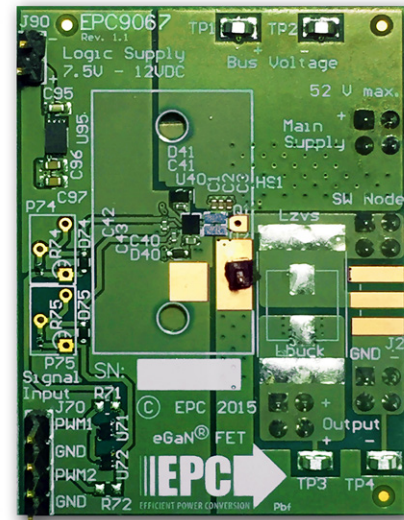
1. Configure the board for either ZVS class-D operation OR Buck converter operation.
2. With power off, connect the input power supply bus to +V_{IN} (J1) and ground / return to -V_{IN} (J4).
3. For ZVS class-D operation, with power off, connect a HF load to the HF output (RF-J2 OR Vsw-J3 and GND-J4). For Buck converter operation, with power off, connect a DC load to the DC output (+V_{OUT}-J5 and GND-J4).
4. With power off, connect the gate drive input to +V_{DD} (J90, Pin-1) and ground return to -V_{DD} (J90, Pin-2).
5. With power off, connect the input PWM control signal to PWM (J70, Pin-1) and ground return to either Pin-2 or Pin-4 of J70.
6. Turn on the gate drive supply – make sure the supply is within the 7.5V and 12V range.
7. Turn on the controller / PWM input source and probe switching node to observe switching operation.

Table 1: Performance Summary (T_A = 25°C) EPC9067

Symbol	Parameter	Conditions	Min	Max	Units
V _{DD}	Gate Drive Input Supply Range		7.5	12	V
V _{IN}	Bus Input Voltage Range			52*	V
V _{OUT}	Switch Node Output Voltage			65	V
I _{OUT}	Switch Node Output Current			2.7*	A
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V _{PWM} rise and fall time < 10ns	40		ns
	Minimum 'Low' State Input Pulse Width	V _{PWM} rise and fall time < 10ns	160#		ns

*Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.

Limited by time needed to 'refresh' high side bootstrap supply voltage.



EPC9067 evaluation board

8. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 52 V on V_{OUT}). Increase voltage slowly while monitoring operation to ensure the FETs are operating within their datasheet parameters.
9. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
10. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node, care must be taken to avoid long ground leads. Measure the switch node by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminal provided. See figure 3 for proper scope probe technique.

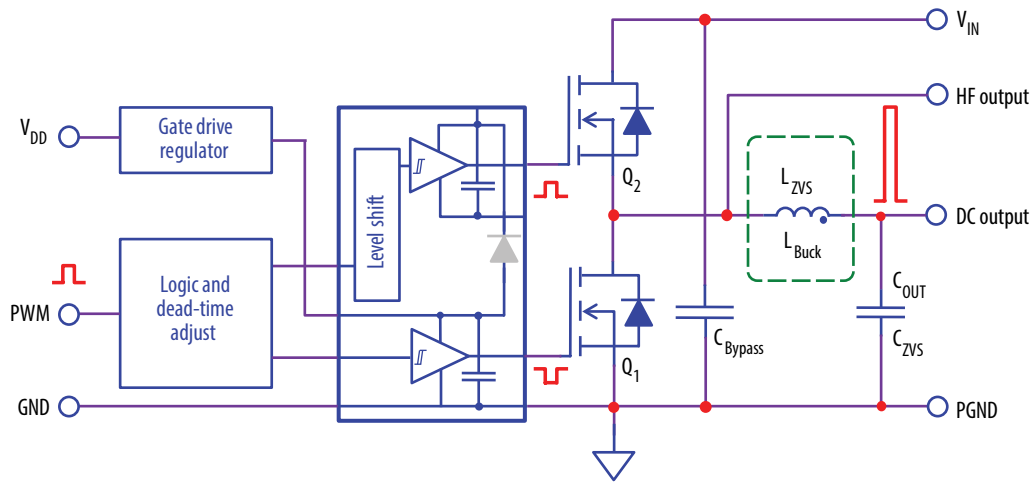


Figure 1: Block diagram of EPC9067 evaluation board

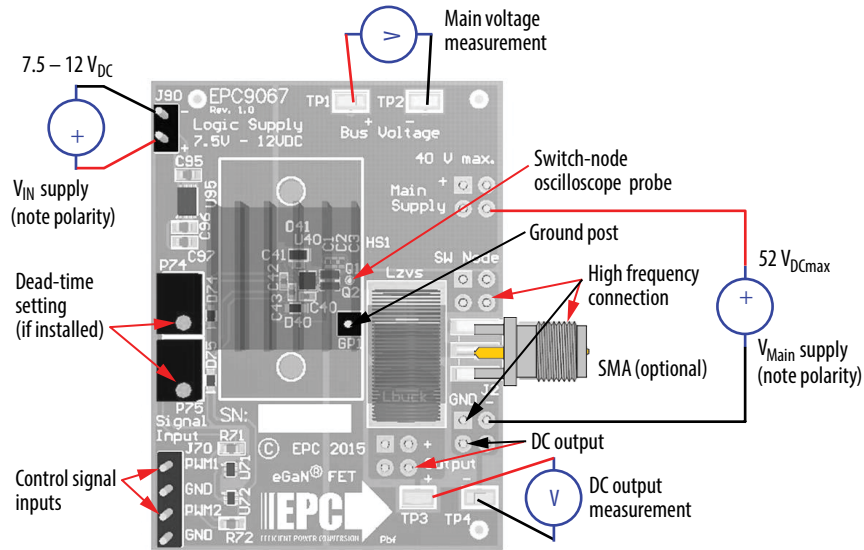


Figure 2: Proper connection and measurement setup

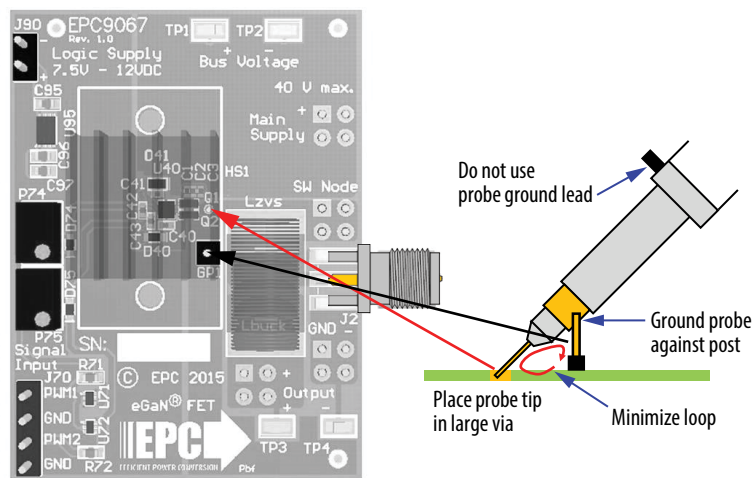


Figure 3: Proper measurement of the switch node

THERMAL CONSIDERATIONS

The EPC9067 evaluation board showcases the EPC8009 eGaN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9067 is intended for bench evaluation with low ambient temperature and convection cooling.

The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9067 evaluation board does not have any current or thermal protection on board.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9067 landing page at: <https://epc-co.com/epc/products/demo-boards/epc9067>

For More Information:

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As an evaluation tool, this board is not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant.

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