# EPC9166

# 12 V Input, 48 V/500 W Output Dual Phase Synchronous Boost Converter Evaluation Board Quick Start Guide

*Using EPC2218 Enhancement Mode eGaN® FET*

November 9, 2021

Version 1.0

EFFICIENT POWER CONVERSION

## DESCRIPTION

The EPC9166 is a 500 W 12 V to 48 V synchronous Boost converter using eGaN® FET. EPC9166 is designed with **EPC2218** enhancement mode eGaN® FET and ISL81807 two phase analog boost controller with integrated eGaN drivers. EPC9166 main features:

- High efficiency: >96.5% with 12 V input and 48 V output
- Switching frequency: 500 kHz
- Reconfigurable output voltage: 36 V, 48 V, 60 V
- Analog controller with integrated gate driver optimized for eGaN® FET
- Other functions:
  - o Soft start
  - o UVLO
  - o Over-current protection
  - o Power good output


EPC9166 board

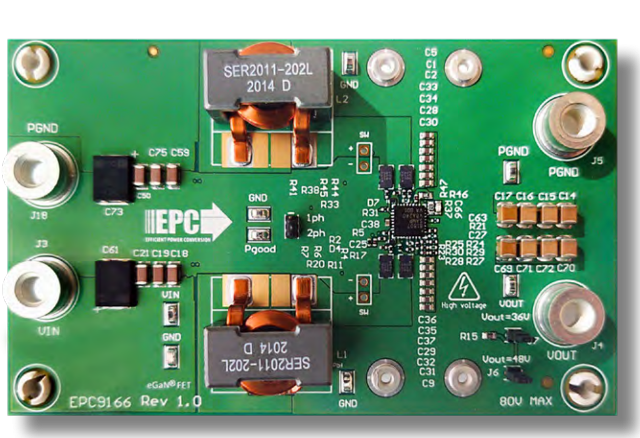
## REGULATORY INFORMATION

This power module is for evaluation purposes only. It is not a full-featured power module and cannot be used in final products. No EMI test was conducted. It is not FCC approved.

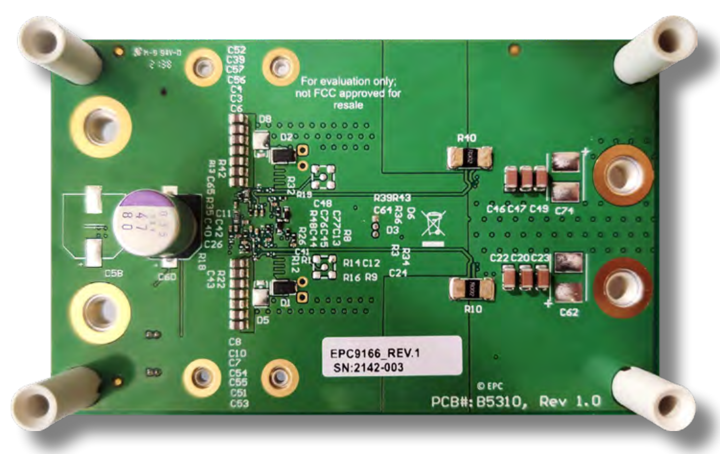
**Table 1: Electrical Characteristics ($T_A$ = 25°C)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | 9 | 12 | 28 | V |
| $V_{UV,Rise}$ | Input UVLO turn on voltage, rising edge | | | 8.3 | | |
| $V_{UV,Fall}$ | Input UVLO turn on voltage, falling edge | | | 7.5 | | |
| $V_{OUT}$ | Output voltage | | 36 | 48 | 60 | |
| $\Delta V_{OUT}$ | Output voltage ripple | Peak to peak | | | 500 | mV |
| $I_{OUT}$ | Output Current | $V_{IN}$ = 12 V, $V_{OUT}$ = 36 V | | | 16[1] | A |
| | | $V_{IN}$ = 12 V, $V_{OUT}$ = 48 V | | | 11[1] | |
| | | $V_{IN}$ = 12 V, $V_{OUT}$ = 60 V | | | 8[1] | |
| $f_S$ | Switching frequency | Mode = CCM | | 490 | | kHz |

[1] The maximum current capability is dependent on thermal conditions. The maximum current shown here is for 1000 LFM or greater. If testing with less than 1000 LFM cooling, the FET temperature should be monitored to ensure the maximum temperature does not exceed the rating in the datasheet.




EPC9166 top view




EPC9166 bottom view

# CUSTOM CIRCUIT CONFIGURATIONS

## Output voltage settings

The EPC9166 output voltage can be configured by table 2.

**Table 2: Output voltage settings**

| Output Voltage | J6 | J7 |
|---|---|---|
| 60 V | Open | Open |
| 48 V (default) | Install | Open |
| 36 V | Open | Install |

# QUICK START PROCEDURE

The evaluation board EPC9166 is easy to set up to evaluate the performance of the EPC2218 eGaN FETs and directly drive from the controller IC. Refer to figure 1 for proper connect and measurement setup and follow the procedure below:

1. Configure the jumpers for phase mode the output voltage setting per figure 1 and table 2. The phase mode jumper J8 sets the 180° phase shift between the two phases in its default location (1). The output voltage is set by jumper J6 and J7 and the default location (2) sets the output voltage at 48 V.
2. With power off, connect the input power supply between VIN (J3) and GND (J18). A shunt can be inserted to measure input current.
3. With power off, connect a programmable load as needed between VOUT (J4) and GND (J5) as shown in figure 1.
4. Turn on the supply voltage to 12 V and **keep the load OFF**. The converter will not start up until the input voltage is above 9 V. The converter is not designed to start up with large load.
5. Check the output voltage is regulated to 48 V to make sure the board is functional. If 48 V is not observed, please carefully re-examine the circuit connections.
6. Activate the programmable load and set to the desired current ensuring the maximum current does not exceed the maximum ratings.
7. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior. For measuring switch node waveforms, please use probes without ground lead and measure as close to the FET. An unpopulated two pin connecter is designed for easy measurement. **Please note polarity**.
8. For shutdown, please follow steps in reverse. For custom configuration please refer the custom configuration section.

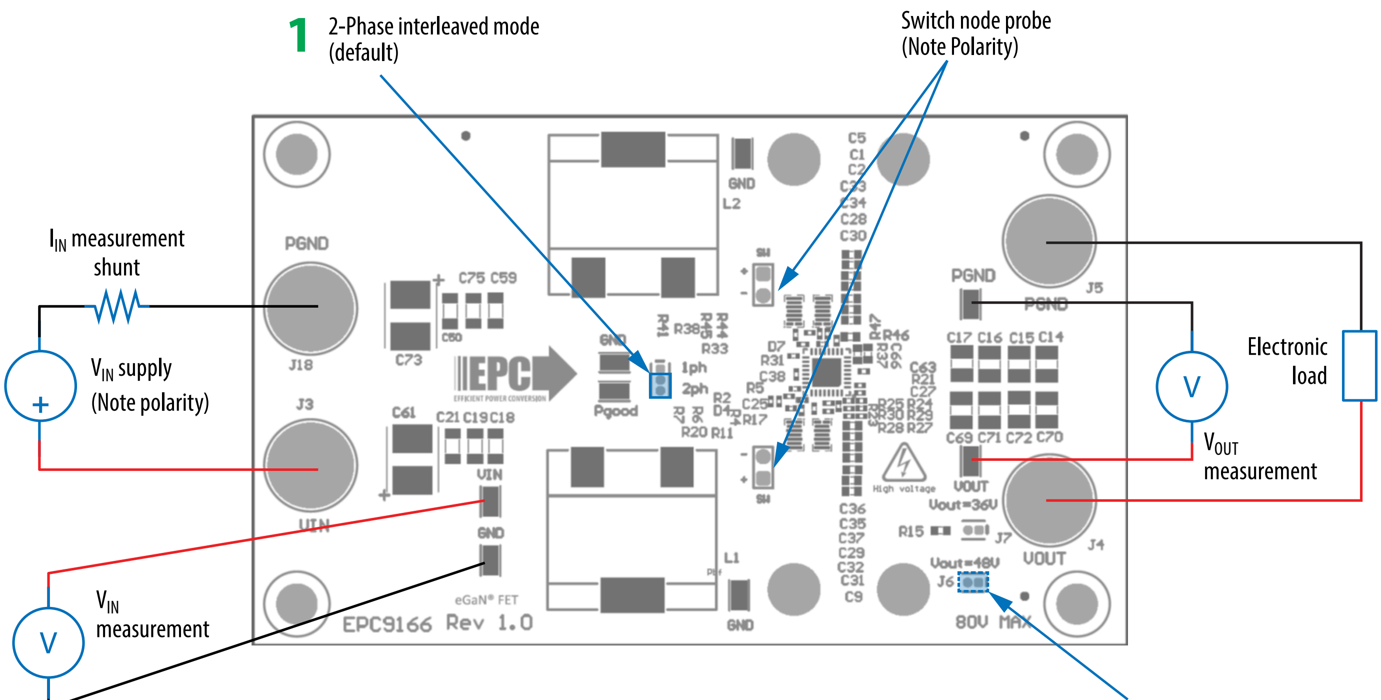



*Figure 1. Proper connection set up and default jumper positions*

## ELECTRICAL PERFORMANCE

### Typical efficiency and power loss

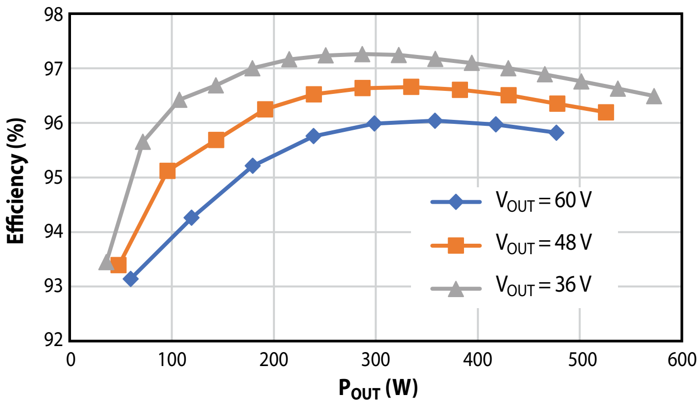



*Figure 2 (a): Typical efficiency for different output voltage (12 V input, 1000 LFM air flow)*

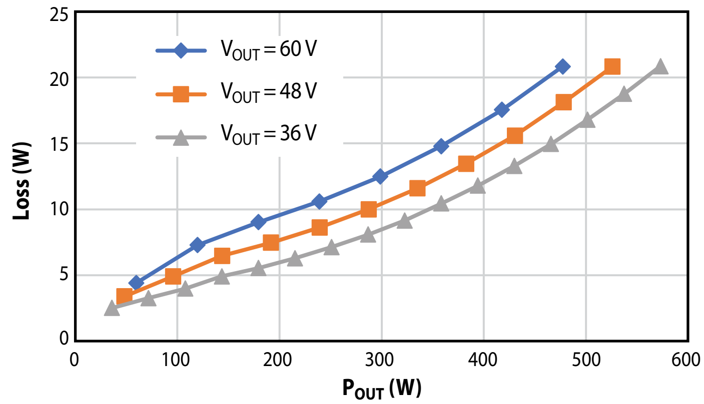



*Figure 2(b): Typical losses for different output voltage (12 V input, 1000 LFM air flow)*

### Typical output voltage ripple

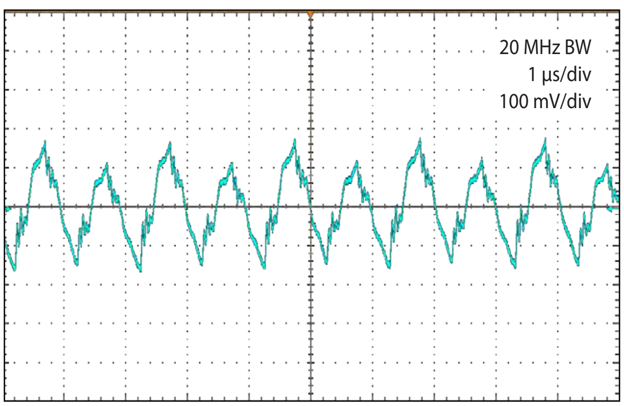



*Figure 3: Typical output voltage ripple: $V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 10 A*

### Typical transient response

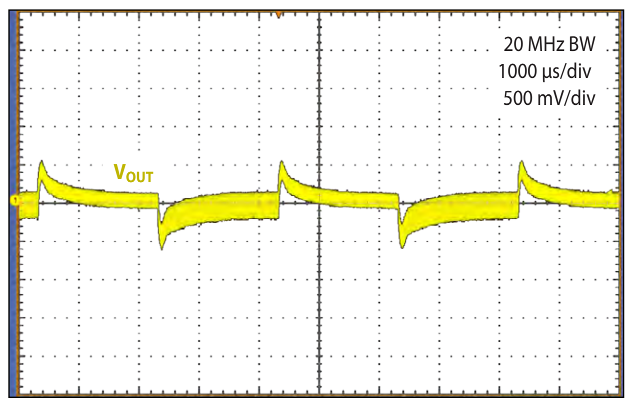



*Figure 4: Typical transient response: $V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, output 5 A to 10 A, di/dt = 2 A/us*

### Typical soft start waveforms

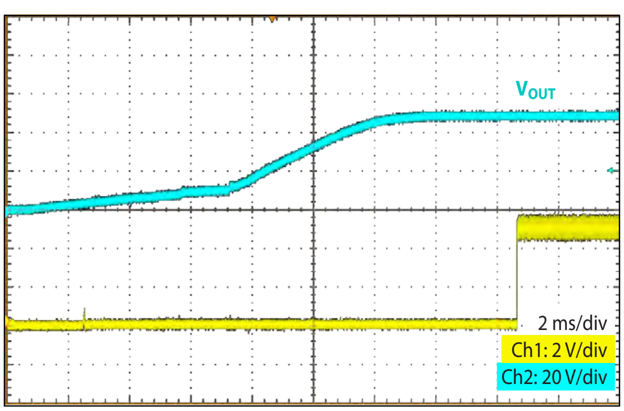



*Figure 5: Soft Start waveform: $V_{IN}$ = 12 V, $V_{OUT}$ = 48 V*

### Typical load regulation

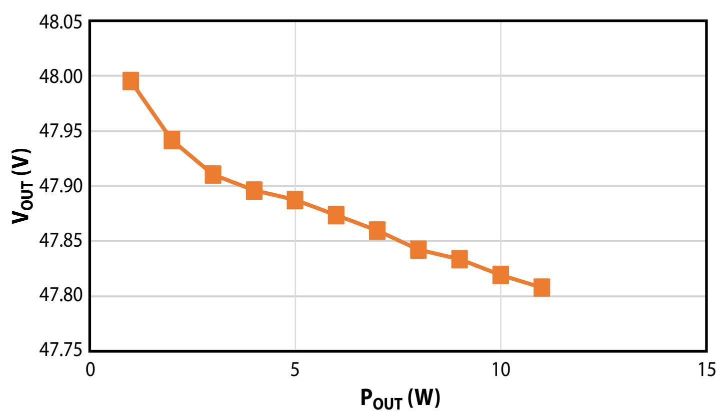



*Figure 6: Typical load regulation: $V_{IN}$ = 12 V, $V_{OUT}$ = 48 V*

## Typical switch node waveform

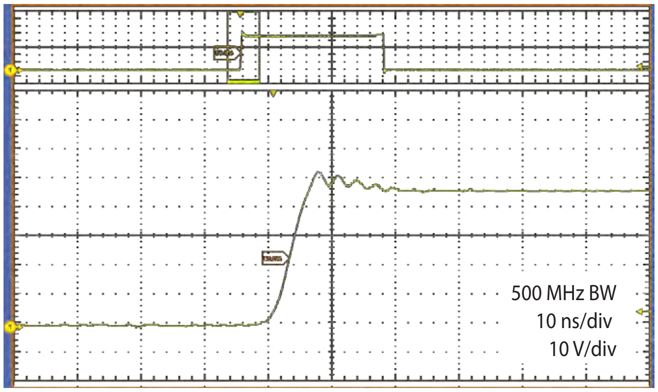



*Figure 7(a): Typical switch node waveform (rising edge):*
*$V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 5 A*

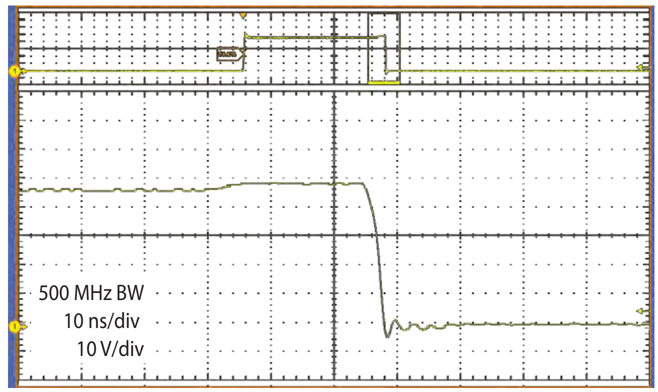
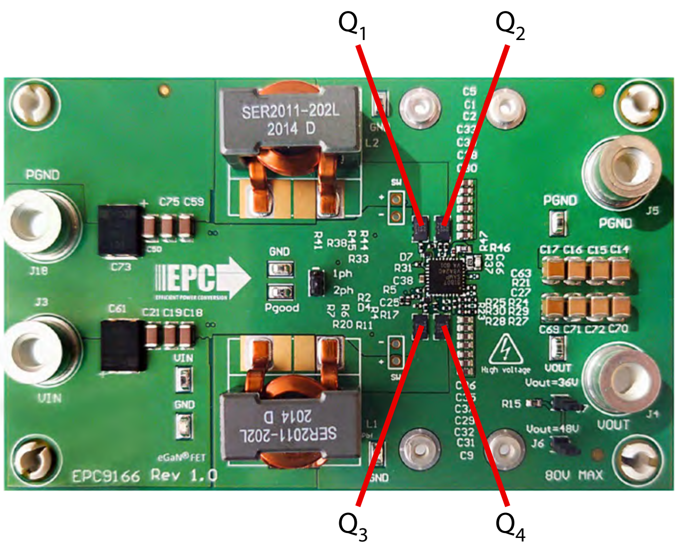



*Figure 7(b): Typical switch node waveform (falling edge):*
*$V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 5 A*

## Typical thermal performance



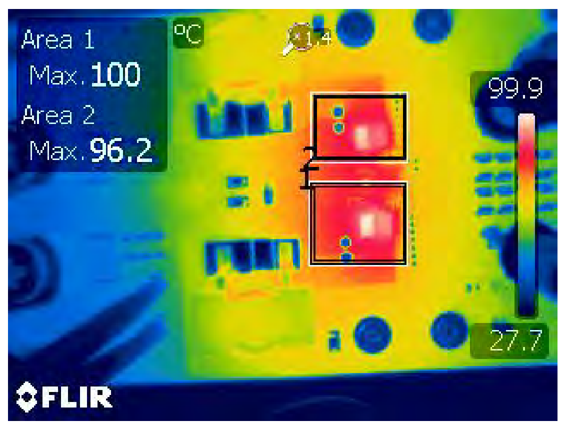




*Figure 8: Typical thermal performance:*
*$V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, $I_{OUT}$ =10 A, 400 LFM air flow*

## Input UVLO adjustment

The input UVLO threshold voltage can be set by R6 and R7 as shown in Figure 9. The default values of Vuv are listed in table 1. If needed, a new UVLO voltage and hysteresis can be set by changing R6 and R7 using equation (1) and (2). Please refer to **ISL81807 datasheet** for more information.

$$V_{uvrise} = \frac{1.8(R6+R7)-2.8\times10^{-6}\,R6R7}{R7} \qquad (1)$$

$$V_{uvfall} = \frac{1.8(R6+R7)-6.8\times10^{-6}\,R6R7}{R7} \qquad (2)$$

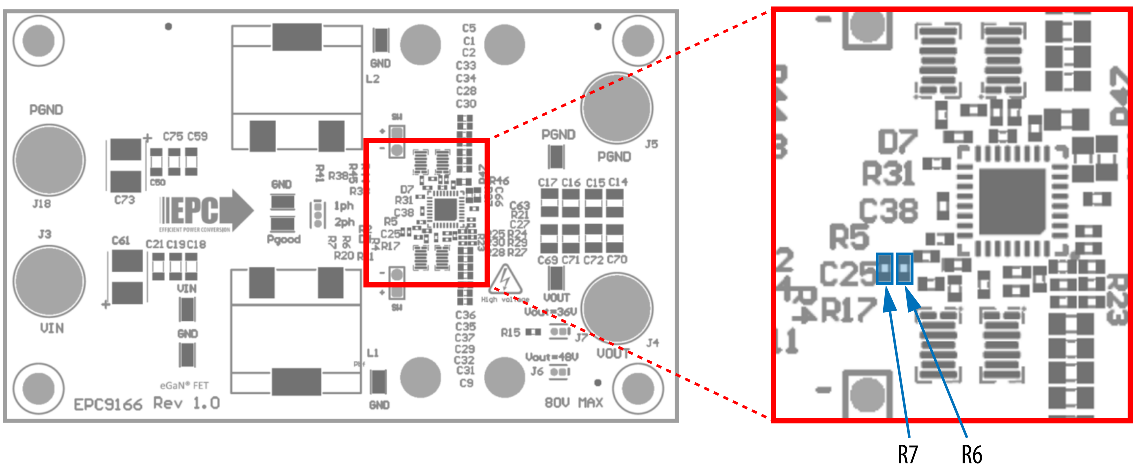



*Figure 9: EPC9166 ULVO settings: location of R6 & R7*

## Switching frequency adjustment

The switching frequency is set by the value of R35 with the frequency given in equation (3). The default frequency is 500 kHz. The location of R35 is shown in Fig 10. Refer to **ISL81807 datasheet** for more information.

$$f_s\,(\text{MHz}) \approx \frac{34\,(\text{MHz})}{R35\,(\text{k}\Omega)} \qquad (3)$$

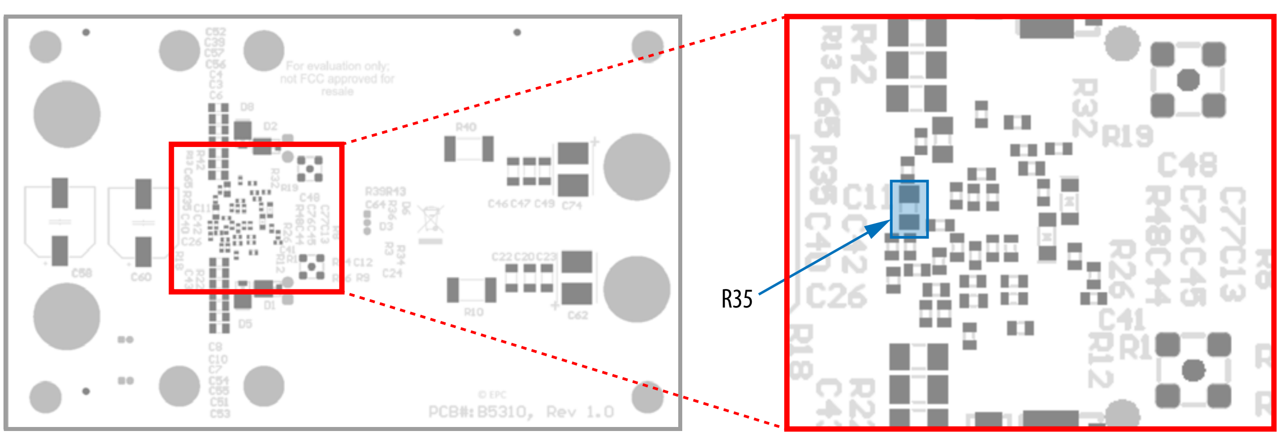



*Figure 10: EPC9166 frequency setting: location of R35*

## THERMAL MANAGEMENT (Optional)

The EPC9166 is intended for bench evaluation at room ambient temperatures and under forced air convection cooling. The addition of heatsink along with forced air cooling is not required but can significantly improve the heat dissipation from the FETs from the top side and increase the current capacity of these devices. A TIM is required between the FETs and the heatsink. The choice of TIM needs to consider the following characteristics:

The EPC9166 board is equipped with four mechanical spacers (S1, S2, S3, S4) that can be used to easily attach a standard eighth-brick converter heatsink as shown in figure 11, and only requires a thermal interface material (TIM), a heatsink, and screws.

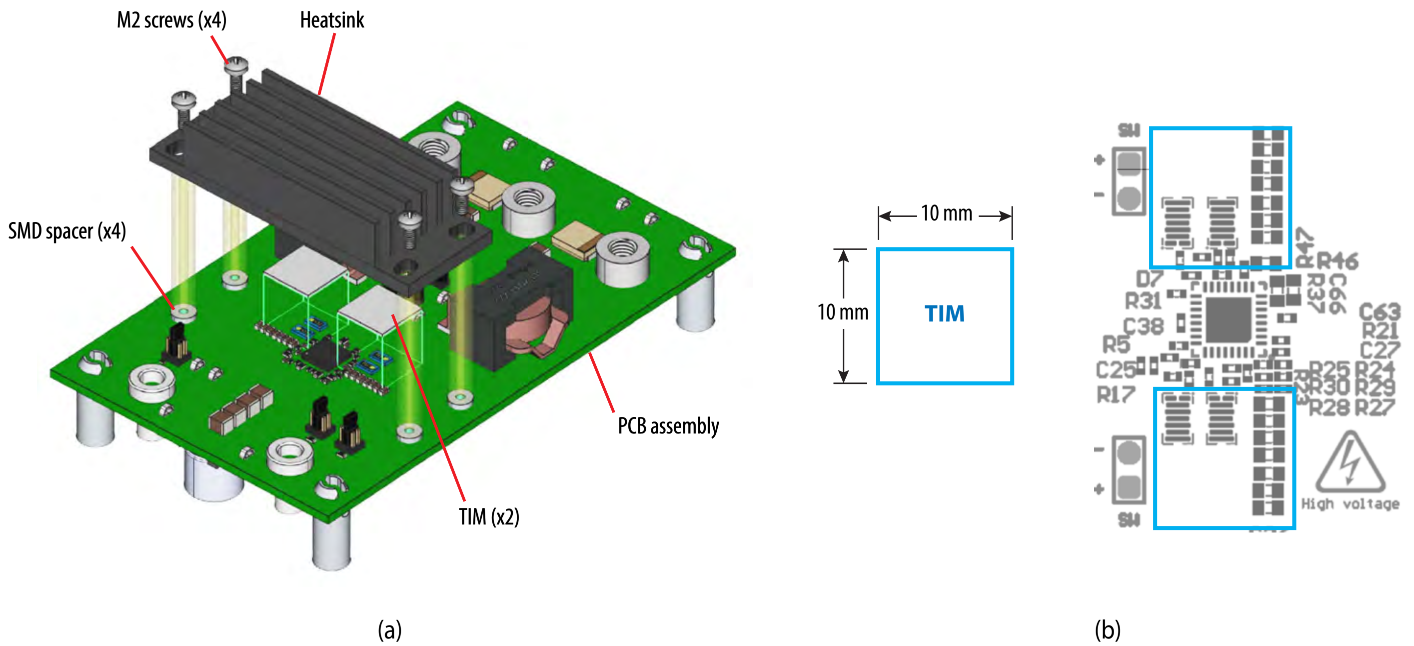



*Figure 11: Exploded 3D assembly of heat sink installment (a) and dimensions and locations of TIM material (b)*

The following heat sink is recommended for EPC9166:

- Wakefield P/N : 567-45AB

A TIM is required between the FETs and the heatsink. The choice of TIM needs to consider the following characteristics:

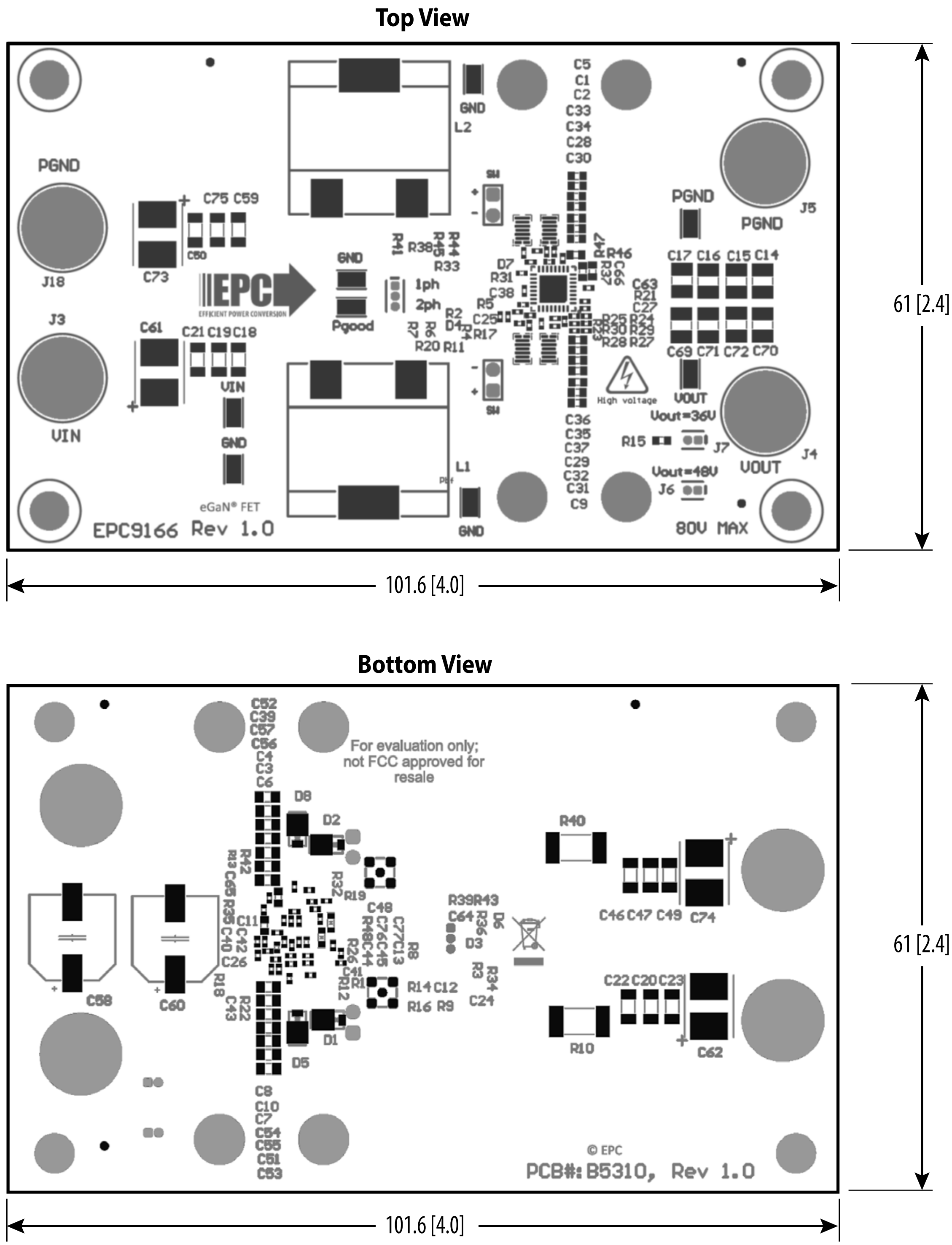
- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

EPC recommends the following thermal interface materials (TIM) for EPC9166:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A620 X 0.5 mm (moderate conductivity of 6.2 W/m·K)

**NOTE**. The EPC9166 evaluation board does not have any current or thermal protection on board.
For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

## MECHANICAL SPECIFICATIONS




Unit: mm [in]

*Figure 12: Mechanical dimensions*

**For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9166 landing page at: https://epc-co.com/epc/products/demo-boards/epc9166**

## For More Information:

Please contact **info@epc-co.com**
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EFFICIENT POWER CONVERSION



**Evaluation Board Notification**

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