

Multi Megahertz Buck Converters using eGaN[®] FETs for Envelope Tracking

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1.4. Wide Bandgap Devices

Preferred Presentation Form: Oral

Abstract

With discrete GaN devices capable of switching at slew rates up to 70 V/ns, the system performance is greatly impacted by aspects outside the active power devices, such as high speed gate drivers and printed circuit board (PCB) layout. In this paper, the latest family of high frequency enhancement mode gallium nitride power transistors (eGaN[®] FETs) is presented for use in multi megahertz buck converters. These devices were designed to address high-frequency hard-switching power applications not practical with discrete Si MOSFETs, thus enabling applications such as envelope tracking that require high-frequency at higher voltages. A number of 10 MHz buck converters are presented with voltages up to 42 V and output power up to 100 W. In this paper, the limitations to switching at these levels using discrete device and drivers are also discussed.

Limitations to the hard switching performance of GaN devices

Consider the ideal hard switching turn-on waveforms (figure omitted). The impact of Q_{GD} on the switching time is apparent and, for hard-switching applications, the use of $Q_{GD} \times R_{DS(ON)}$ as a switching figure of merit (FOM) is common [1]. For cases at lower voltages and higher currents, the current-dependent term, Q_{GS2} , cannot be neglected and the metric used to compare device technologies can be given as [2]:

$$Q_{SW} \times R_{DS(ON)} = (Q_{GD} + Q_{GS2}) \times R_{DS(ON)}$$

where Q_{SW} is the total switching gate charge during the hard switching interval. Figure of merit and the impact of device parameters on switching performance will be discussed in detail in the final paper. Figure 1 shows the FOM reduction achievable with GaN technology over Si MOSFETs for higher current-rated devices. Beyond the device parameters, layout and package dependent parameters such as common source inductance (CSI) and power loop inductance also play a critical role in hard-switching losses [3]. The impact of parasitics will be discussed in the final paper.

Increasing switching frequency and voltage with eGaN FETs:

From the analysis above it becomes apparent that to push the frequency and voltage capability of GaN devices in traditional hard switching topologies, the FOM must improve and the die size must shrink. The EPC8000 series is the latest eGaN FET and targets high frequency applications such as envelope tracking and compares favorably in terms of FOM to similar voltage rated existing EPC2000 series parts as shown in Table 1. To maximize the performance of this technology it is important to minimize CSI, reduce high frequency power loop inductance, and minimize gate loop inductance. This is achieved not just through optimizing PCB layout, but also by improving the eGaN FET package layout. The details of the package and PCB layout improvements for a high frequency converter design will be covered in the final paper.

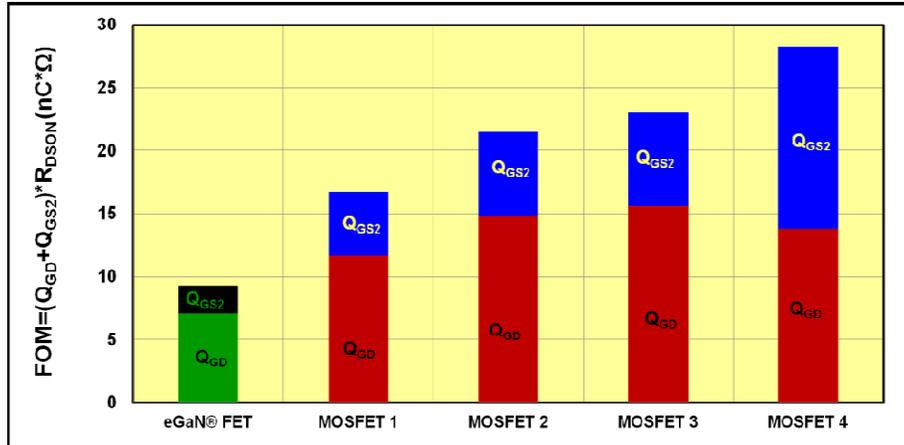


Figure 1: Comparison of hard-switching FOM of 40V eGaN FET and MOSFETs (VDS=20 V, IDS=20

Experimental Verification

To evaluate the system performance using improved layout design together with the improved performance eGaN FETs, a development board was constructed as basis for the investigation. The layout of the resulting power stage is shown in figure 2. To minimize gate loop inductance, while still being able to adjust pull-up and pull-down resistances separately, two 0201 size resistors were placed in parallel per gate resistor. The use of a BGA gate driver [4] with no wire-bonds, together with the internal copper layer design helped to further minimize gate loop inductance. This, together with the power loop layout and eGaN FET device pin-out, will be shown in the final paper.

With this setup, effective rise times in the range of one nanosecond were achieved at 42 V input, and rise times of less than 500ps at 20V input. The switch node voltage waveform for the 42 V input buck converter with 2 A load is shown in figure 3. At this high switching speed the line between the classical di/dt and dv/dt switching intervals are blurred. The initial bump in the rising switch node is due to the rising commutation current across the power loop inductance. Once the load current has commutated, and the plateau voltage has been reached, the real dv/dt interval slew rate can be as high as 75V/ns. This will be discussed in greater detail in the final paper. *This design also tests the limits of the silicon gate driver and additional improvements that can be made to it to further improve performance will be discussed.*

Experimental results

This buck converter is designed for envelope tracking [5-7] and the need for multi-phase high frequency buck converters will be discussed in the final paper. Previous results at 10 MHz and a similar 2:1 conversion ratio have shown peak efficiencies of ~83% [5] at 20 W - 25 W output operating from a 24 V input using eGaN FETs. This same paper also shows around a 20 percentage point improvement in converter efficiency when comparing to MOSFETs and RF LDMOS devices. The results in figure 4 show a peak output efficiency of ~89% at around 35 W, operating from a 42 V input. The same circuit, operated at 5 MHz, peaked at 94% efficient at around 30 W. In the final paper, additional 10 MHz buck converter results at lower voltages with other EPC8000 series parts will also be presented. At these lower voltages, switching times below 500ps are possible at currents as high as 4 A.

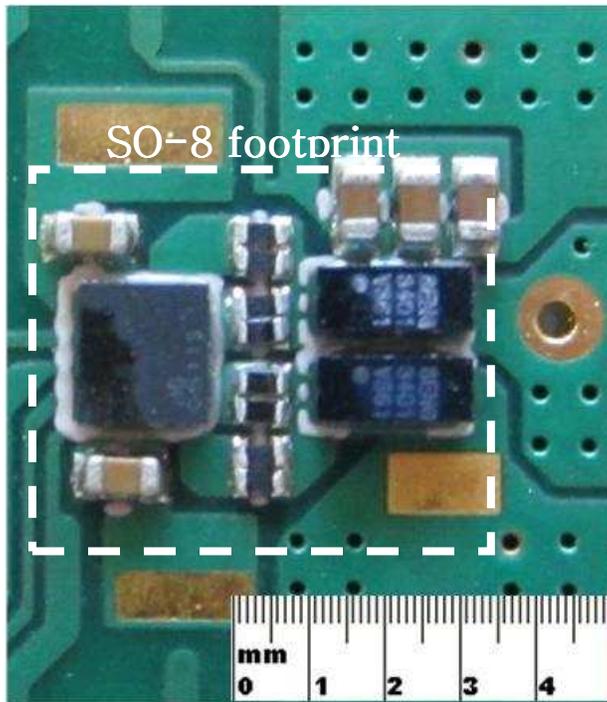


Figure 2: Experimental power stage layout of a 10 MHz Buck converter

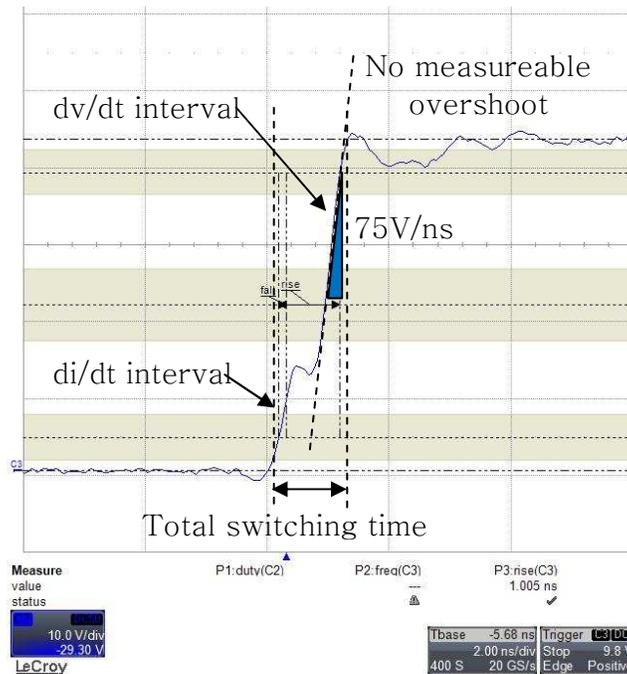


Figure 3: Hard switching rising edge showing a combined rise-time of around 1ns.

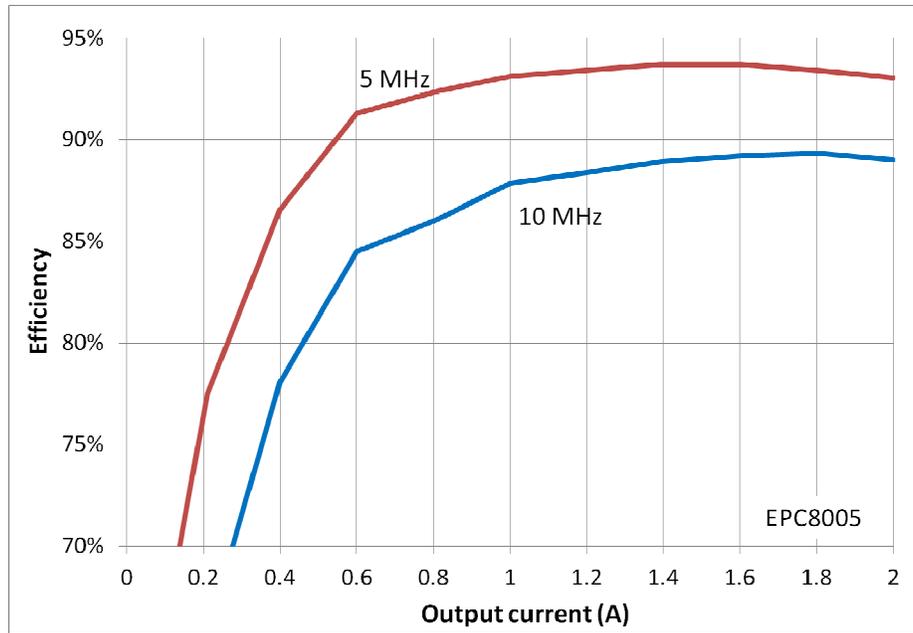


Figure 4: Efficiency versus load current for a 42 V_{IN}, to 20 V_{OUT} hard-switching buck converter switching at 5 MHz and 10 MHz respectively.

Summary

This paper will discuss the merits of GaN technology and its ability to increase the frequency of discrete hard switching designs well beyond the capability of Si MOSFETs in the 40 V to 100 V device range. The latest family of eGaN FETs, designed to enhance high frequency performance is presented, and the design requirements to achieve a 10 MHz, 42 to 20 V, 2 A buck converter operating at peak efficiencies around 89% will be discussed.

References

- [1] Alex Q. Huang, "New Unipolar Switching Power Device Figures of Merit," IEEE Electron Device Lett., vol. 25, pp. 298-301, 2004.
- [2] Yucheng Ying, "Device selection criteria---based on loss modeling and Figure of Merit", Thesis of Master of Science in Electrical Engineering of Virginia Tech, 2008.
- [3] D. Reusch, J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," Applied Power Electronics Conference, APEC 2013, pp.649-655, 16-21 March 2013.
- [4] LM5113TM half bridge driver, <http://www.ti.com/product/lm5113>
- [5] D. Čučak, M. Vasić, O. García, J. A. Oliver, P. Alou, J. A. Cobos et al, "Application of eGaN FETs for highly efficient Radio Frequency Power Amplifier," Conference on Integrated Power Electronics Systems, CIPS 2012, paper P22, March 2012.
- [6] M. Norris and D. Maksimovic, "10 MHz Large Signal Bandwidth, 95% Efficient Power Supply for 3G-4G Cell Phone Base Stations," Applied Power Electronics Conference, APEC 2012, pp. 7-13, Feb. 2012.
- [7] J.T. Strydom, "eGaN® FET- Silicon Power Shoot-Out Volume 8: Envelope Tracking," Power electronics magazine, April 2012, <http://powerelectronics.com/gan-transistors/egan-fet-silicon-power-shoot-out-volume-8-envelope-tracking>