GaN Reliability and Lifetime Projections: Phase 15

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The rapid adoption of GaN devices in many diverse applications calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices, including integrated circuits (ICs). It is also necessary to look for information from real-world experience that either confirms the laboratory-derived data or opens new questions about mission robustness. This Phase 15 Reliability Report documents continued work using test-to-fail methodology and adds specific reliability metrics and predictions for solar optimizers, lidar sensors, and DC-DC converters.

NEED FOR ADDITIONAL STANDARD QUALIFICATION TESTING

Why test-to-fail in addition to standard qualification testing?

Standard qualification testing for semiconductors typically involves stressing devices at or near the limits specified in their datasheets for a prolonged period, or for a certain number of cycles. The goal of standard qualification testing is to have zero failures out of a relatively large group of parts tested.

This type of qualification testing is inadequate since it only reports parts that passed a very specific test condition. By testing parts to the point of failure, an understanding of the amount of margin between the datasheet limits can be developed, and more importantly, an understanding of the intrinsic failure mechanisms can be found. By knowing the intrinsic failure mechanisms, the root cause of failure, and the behavior of this mechanism over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions (For an excellent description of test-to-fail methodology for testing semiconductor devices, see reference [1]).

Key Stress Conditions and Intrinsic Failure Mechanisms for GaN Power Devices

What are the key stress conditions encountered by GaN power devices and what are the intrinsic failure mechanisms for each stress condition?

As with all power transistors, the key stress conditions involve voltage, current, temperature, and humidity, as well as various mechanical stresses. There are, however, many ways of applying these stress conditions. For example, voltage stress on a GaN transistor can be applied from the gate terminal to the source terminal (V_{GS}), as well as from the drain terminal to the source terminal (V_{DS}). For example, these stresses can be applied continuously as a DC bias, they can be cycled on-and-off, or they can be applied as high-speed pulses. Current stress can be applied as a continuous DC current, or as a pulsed current. Thermal stresses can be applied continuously by operating devices at a predetermined temperature extreme for a period of time, or temperature can be cycled in a variety of ways.

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the datasheet limits of the product. Care needs to be taken to make certain the excess stress condition does not induce a failure mechanism that would never be encountered during normal operation. To make certain that excess stress conditions did not cause the failure, the failed parts need to be carefully analyzed to determine the root cause of their failure. Only by verifying the root cause can an complete understanding of the behavior of a device under a wide range of stress conditions be developed. It should be noted that, as more understanding of intrinsic failure modes in eGaN® devices has been gained, two facts have become clear; (1) eGaN devices are more robust than Si-based MOSFETs, and (2) MOSFET intrinsic failure models are not valid when predicting eGaN device lifetime under extreme or long-term electrical stress conditions.

Table 1 lists in the left-hand column all the various stressors to which a transistor can be subjected during assembly or operation. Using the various test methods listed in the third column from the left, and taking devices to the point of failure, the intrinsic failure mechanisms can be discovered. The failure mechanisms confirmed as of this writing are shown in the column on the right.

Stressor	Device/ Package	Test Method	Intrinsic Failure Mechanism
Voltage	Device	HTGB	Dielectric failure (TDDB)
			Threshold shift
		HTRB	Threshold shift
			$R_{DS(on)}$ shift
		ESD	Dielectric rupture
Current	Device	DC Current (EM)	Electromigration
			Thermomigration
Current + Voltage (Power)	Device	SOA	Thermal Runaway
		Short Circuit	Thermal Runaway
Voltage Rising/Falling	Device	Hard-switching Reliability	$R_{DS(on)}$ shift
Current Rising/Falling	Device	Pulsed Current (Lidar reliability)	None found
Temperature	Package	HTS	None found
Humidity	Package	MSL1	None found
		H3TRB	None found
		AC	None found
		Solderability	Solder corrosion
		uHAST	Denrite Formation/Corrosion
Mechanical / Thermo-mechanical	Package	TC	Solder Fatigue
		IOL	Solder Fatigue
		Bending Force Test	Delamination
		Bending Force Test	Solder Strength
		Bending Force Test	Piezoelectric Effects
		Die shear	Solder Strength
		Package force	Film Cracking

Table 1: Stress conditions and intrinsic failure mechanisms for GaN transistors

FOCUS AND STRUCTURE OF THIS REPORT

The first topic discussed in this report (**Section 1**) is the intrinsic failure mechanism impacting the gate electrode of GaN devices. In this section is a summary of the physics-based lifetime model first derived in the Phase 14 report [2].

The second section (**Section 2**) summarizes the intrinsic mechanisms underlying dynamic $R_{DS(on)}$. As with the gate stress section, the work on dynamic $R_{DS(on)}$ was enhanced through the development of a physics-based model in the Phase 14 report that explains all known behaviors in eGaN transistors relating to changes in $R_{DS(on)}$. This model is therefore most useful for predicting lifetimes in more complex mission profiles.

Section 3 focuses on the safe operating area (SOA) of GaN devices. This subject has been studied extensively in silicon-based power MOSFETs, where a secondary breakdown mechanism is observed that limits their utility under high drain bias conditions [3]. Several GaN products were tested exhaustively throughout their datasheet SOA, and then taken to failure to probe the safety margins. In all cases, the data shows that GaN transistors will not fail when operated within the datasheet SOA.

In **Section 4**, eGaN devices are tested to destruction under short-circuit conditions. The purpose of this test is to determine how long and what energy density they withstand before catastrophic failure. This information is vital to industrial power and motor drive engineers needing to include short-circuit protection in their designs.

In **Section 5**, the subject of mechanical force testing of wafer level chip-scale packages (WLCSP) is presented. Test-to-fail results for die shear (in-plane force) demonstrate robustness that exceeds MIL-STD-883E recommendations. Backside pressure (out-of-plane) tests show the package is capable of 400 psi without failure. Bending-force tests examine both solder joint robustness and look for any piezoelectric effects that might modulate device electrical parameters. All devices passed a 4-mm deflection (250 N) based on the Q200-005A test standard, with first failures occurring at 6-mm deflection. No electrical parameter changes could be measured. At the end of this section, it is shown that the bending forces required to physically break the devices are well below forces required to change electrical characteristics due to modulation of the piezoelectrically generated fields.

Section 6 examines the issue of thermo-mechanical stresses generated by both temperature cycling and cycling based on self-heating. An extensive study of underfill products was conducted to experimentally generate lifetime predictions. A finite element analysis at the end of this section explains the experimental results and generates guidelines for selection of underfill based on key material properties.

In **Section 7 through 9**, EPC has tested or modeled devices using application-specific mission profiles. For example, GaN devices have been extensively applied in light detection and ranging (lidar) equipment used on autonomous cars, trucks, robots, consumer products, and drones. The fast-switching speed, small size, and high pulsed current capabilities of GaN devices add to a lidar system's ability to "see" at a greater distance with higher resolution. Lidar systems push the limits of dynamic voltage and current (di/dt and dv/dt) beyond anything experienced in silicon. The Phase 14 Reliability Report documented that GaN devices passed over thirteen trillion pulses (about triple a typical automotive lifetime) without failure or significant parametric drift.

In this Phase 15 report, new data are reported on qualification testing as well as test-to-fail studies that confirm that GaN ICs have a high degree of robustness even when stressed beyond datasheet limits.

In **Section 8**, EPC's extensive library of lifetime models are applied to demonstrate GaN device lifetimes greater than 25 years with sub-one-percent failure rates under the stringent requirements of rooftop solar installations.

In the penultimate section (**Section 9**), the previously reported modeling of GaN devices in DC-DC buck converters and synchronous rectifiers is summarized to predict the degradation of GaN power devices under extreme repetitive voltage overshoot conditions.

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SECTION 1: VOLTAGE/TEMPERATURE STRESS ON THE GATE

Based on the work shown in the Phase 14 Reliability Report, we have all of the mathematical ingredients to derive a lifetime equation applicable to p-GaN gates:

$$MTTF = \frac{Q_C}{G} = \frac{qQ_C}{\alpha_n J_n} = \frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V+V_0}\right)^m\right] \quad \text{Eq. 1}$$

with parameters listed below:

m = 1.9
V_0 = 1.0 V
B = 57.0 V
A = 1.7×10^{-6} s
c = $6.5 \times 10^{-3}\ K^{-1}$

The lifetime equation (Equation 1) is plotted against a more recently measured acceleration data for EPC2212 in Figure 1. To produce this fit, all parameters in Equation 1 were fixed except A and B. The resulting best fit for B, (when converted into a field by dividing by the gate thickness), resulted in a value of bn = 7.6×10^6 V/cm, in very close agreement with Ooi's value of 7.2×10^6 V/cm [4].

Figure 2 shows the temperature dependence of the lifetime equation at –75°C, 25°C, and 125°C. The temperature dependence (contained in the parameter c) is taken directly from Ozbek without fitting to data. Note that at higher temperature, the MTTF is slightly higher, which is consistent with the measured data reported in the Phase 14 report.

This gate lifetime model was developed by including all aspects of the unique characteristics that were identified through accelerated gate testing in a representative GaN product (EPC2212). The data in figure 1 shows that when keeping the gate bias below the maximum rated voltage (V_{GS} = 6 V), eGaN devices should have less than 1 ppm failure rate for 10 years of lifetime under continuous DC bias. This projected result is consistent with EPC's field experience for gate failures.

1.2 Summary of Physics-Based Derivation of Gate Lifetime Model

The impact ionization model of gate lifetime in GaN transistors (Equation 1) successfully accounts for a host of observed factors:

- Positive temperature coefficient of MTTF (which is unusual in semiconductor physics of failure).
- Very high acceleration with gate bias, and acceleration that is steeper than exponential at decreasing gate bias.
- Dielectric rupture through a high quality Si_3N_4 film at a nominal field strength well below breakdown (as a result of hole injection and trapping from the adjacent pGaN region).

This lifetime equation is not simply borrowed from the body of standard reliability models developed for MOSFETs. Instead, it represents the first gate lifetime model, built up from the root physics of failure, specifically applicable to GaN transistors.

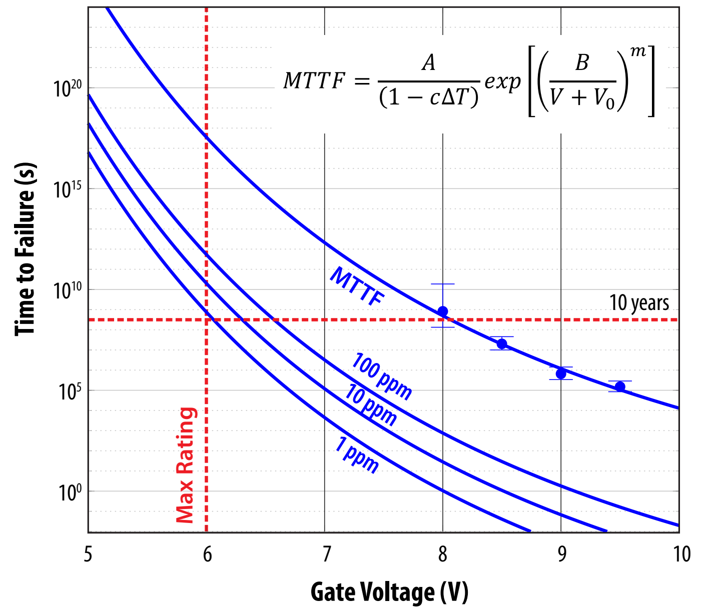


Figure 1: EPC2212 MTTF (recently measured) vs. V_{GS} at 25°C (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

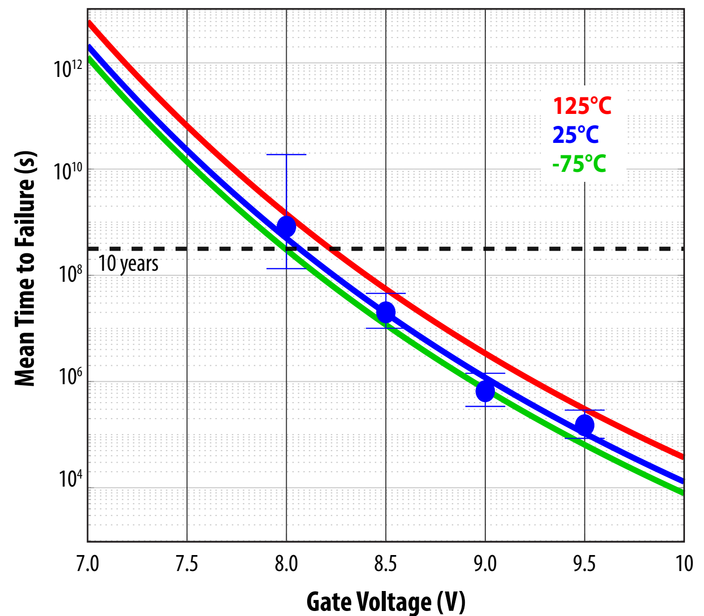


Figure 2: MTTF for EPC2212 (25°C) measured at four different gate biases. Blue line is lifetime model. Red and green lines are predictions of the lifetime model at 125°C and –75°C respectively.

SECTION 2: VOLTAGE/TEMPERATURE STRESS ON THE DRAIN

This same test-to-fail methodology can be adapted to every other stress condition. For example, one common concern among GaN transistor users is dynamic on-resistance. This is a condition whereby the on-resistance of a transistor increases when the device is exposed to high drain-source voltage (V_{DS}). The traditional way to test for this condition is to apply maximum-rated DC V_{DS} at maximum-rated temperature (typically 150°C). If there are no failures after a certain amount of time – usually 1000 hours – the product is considered good.

As shown in the Phase 14 report, the dominant mechanism causing the on-resistance to increase is the trapping of electrons in trap-states near the channel. As the trapped charge accumulates, it depletes electrons from the two-dimensional electron gas (2DEG) in the ON state, leading to an increase in $R_{DS(on)}$.

Figure 3 is a magnified image of an EPC2016C GaN transistor showing thermal emissions in the 1–2 µm optical range. Emissions in this part of the spectrum are consistent with hot electrons and their location in the device is consistent with the location of the highest electric fields when the device is under drain-source bias.

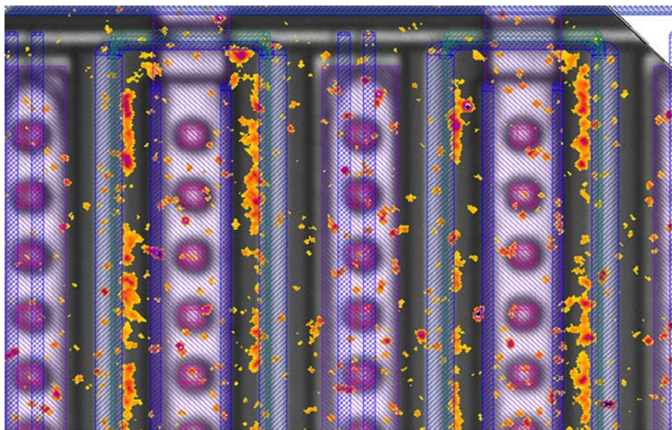
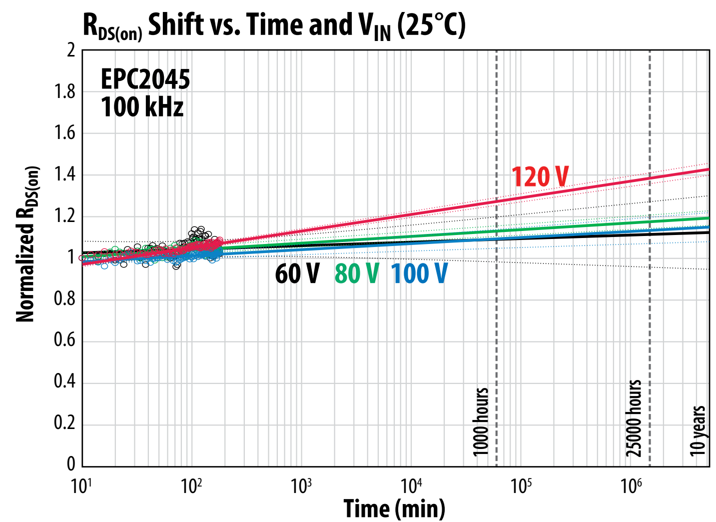


Figure 3: A magnified image of an EPC2016C GaN transistor showing light emission in the 1–2 µm wavelength short-wave infrared light range (SWIR) that is consistent with hot electrons. The SWIR emission (red-orange) has been overlaid on a regular (visible wavelength) microscope image.

Knowing that hot electrons in this region of the device are the source of trapped electrons, a better understanding of how to minimize the dynamic on-resistance can be achieved with improved designs and processes. By understanding the general behavior of hot electrons, their behavior over a wider range of stress conditions can be generalized.

Figure 4 shows how the $R_{DS(on)}$ of a fifth-generation EPC2045 GaN transistor [5], designed with the knowledge that hot electrons trapping is accelerated with peak electric fields near the drain, increases over time at various voltage stress levels and temperatures. On the left, the devices were tested at 25°C, at voltages from 60 V to 120 V (EPC2045 has a $V_{DS(max)}$ of 100 V). The horizontal axis shows time measured in minutes, with the right side ending at 10 years. The graph on the right shows the evolution of $R_{DS(on)}$ when biased at 120 V at different temperatures. The counter-intuitive result shows that the on-resistance increases faster at lower temperatures. This is consistent with hot-carrier injection because hot electrons travel further between scattering events at lower temperatures and therefore are accelerated to greater kinetic energies by a given electric field. The result is that the electrons can get to different layers where they are more prone to become trapped. This suggests that traditional testing methods, where a device is tested at maximum voltage and temperature, may not be enough to determine the reliability of a device.



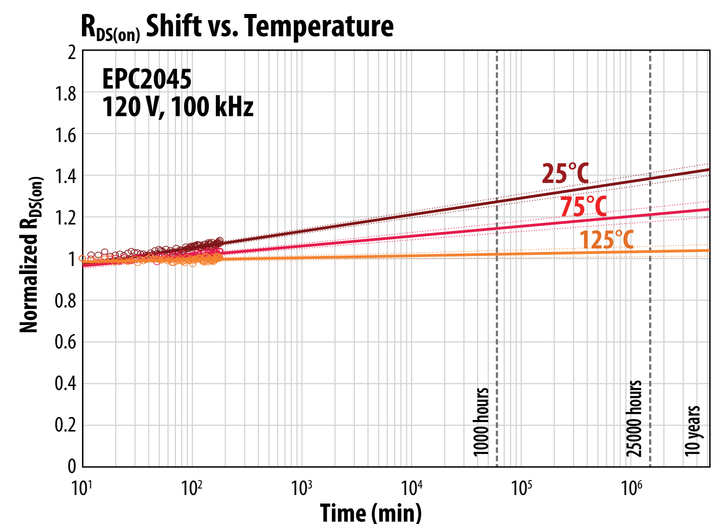


Figure 4: The $R_{DS(on)}$ of a fifth-generation EPC2045 eGaN FET over time at various voltage stress levels and temperatures. On the top, the devices were tested at 25°C at voltages from 60 V to 120 V. The graph on the bottom shows the evolution of $R_{DS(on)}$ at 120 V at various temperatures.

In the original publication of the HTRB results [2, 6], the MTTF was found to be the highest at 90°C as compared to 35°C and 150°C, which was a mystery at the time. The results now can be better understood. As the device is heated under DC bias, the leakage current increases. The shorter mean free path of the hot carriers, however, counters the increase in available electrons such that the $R_{DS(on)}$ increase over time climbs from room temperature to 90°C, but then starts declining at higher temperatures – another counter-intuitive result. The original publication of these results has led to great interest in the GaN community, along with many questions and some skepticism as well.

2.1 Physics-Based Dynamic $R_{DS(on)}$ and Lifetime Models

In the Phase 14 Reliability Report a first-principles mathematical model to describe the dynamic $R_{DS(on)}$ effect in GaN transistors from the basic physics of hot carrier scattering into surface traps was reported. The model successfully predicted all the following phenomena:

- $R_{DS(on)}$ growth with time
- The slope of $R_{DS(on)}$ over time has a negative temperature coefficient (i.e., lower slope at higher temperature)
- Switching frequency does not affect the slope, but causes a small vertical offset
- Switching current does not affect the slope
- Negligible difference between inductive and resistive hard switching

The final mathematical model for $R_{DS(on)}$ growth as a function of time, temperature, and drain voltage was shown in Equation 2.

$$\frac{\Delta R}{R} = a + b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\log(t) \qquad \text{Eq. 2}$$

Independent Variables:

V_{DS} = Drain voltage (V)
T = Device temperature (K)
t = Time (min)

Parameters:

a = 0.00 (unitless)
b = 2.0E-5 ($K^{-1/2}$)
$\hbar\omega_{LO}$ = 92 meV
V_{FD} = 100 V (appropriate for Gen5 100 V products only)
α = 10 (V)
k = Boltzmann constant=0.0862 meV/K

Many customers require lifetime estimates under specific use conditions to fulfill certain quality or reliability requirements. By defining the lifetime (under hard-switching conditions) as the time <t> at which $R_{DS(on)}$ will rise 20% from its initial value, Equation 3 can be inverted in a straightforward manner to obtain.

$$\langle t\rangle = \exp\left[\frac{(0.2-a)}{b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)}\right](\text{min}) \qquad \text{Eq. 3}$$

This equation gives the expected MTTF under hard-switching conditions as a function of operating voltage and temperature. Typically, worst case values (highest voltage, lowest temperature) are used to provide a lower bound. As before, the lifetime will be in units of minutes. Other definitions of lifetime can be applied and extracted from Equation 3 as well.

2.2 Effect of Switching Frequency and Switching Current

In the analysis so far, the effects of switching frequency (f) and switch current (I) on the $R_{DS(on)}$ growth characteristics have been ignored. The current directly impacts the number of electrons injected into the high field region during the hard-switching transition, and therefore has a linear effect on the hot carrier density. Likewise, the switching frequency determines the number of hot carrier pulses seen at the drain in a given time interval, and therefore also has a linear effect on the surface trapping rate.

By assuming that the surface trapping rate is linearly proportional to both frequency (f) and current (I), the effects of f and I are included in Equation 4, where a simple scaling term is derived to relate the $R_{DS(on)}$ growth in one switching condition (f_1, I_1) to another (f_2, I_2).

$$R(t;f_2,I_2) = R(t;f_1,I_1) + b\left(\log\left(\frac{f_2}{f_1}\right)+\log\left(\frac{I_2}{I_1}\right)\right) \qquad \text{Eq. 4}$$

Mathematically, the effect of changing the switching frequency or current is to simply offset the $R_{DS(on)}$ growth curve vertically by a small amount. The offset depends on the logarithm of f and I, and therefore has a fundamentally weak dependence on these variables. Furthermore, the offset depends on the overall slope b of the log(t) growth characteristic. Therefore, if the FET is operated under conditions with low $R_{DS(on)}$ rise (low slope b), the effect of changing frequency or current will be negligible.

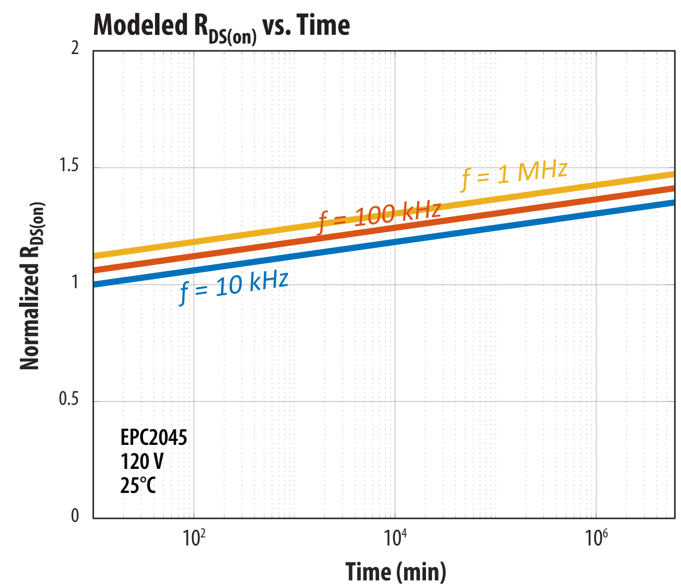


Figure 5: Modeled $R_{DS(on)}$ vs. Time at three different switching frequencies, covering two orders of magnitude. Note that the effect of frequency change is a small vertical offset in the growth characteristic. The same offset would occur at different switch currents.

Figure 5 compares the modeled $R_{DS(on)}$ vs. time for an EPC2045 at three different switching frequencies, from 10 kHz to 1 MHz. Note that the curves are simply offset from each other vertically. The same would be true had we compared different switch currents. Because the offset changes as the logarithm of f (or I), even a 10x increase in switching frequency (or current) would be difficult to observe experimentally owing to ±10% noise in the measurement and projection.

2.3 Impact of Higher Stress Voltages

In the case where the amount of trapped charge approaches the number of electrons available in the 2DEG (the surface trapped charges (Q_S) approaches the built-in 2DEG piezoelectric charge (Q_P), the simplifying assumption used in Equation 2 is no longer valid. This situation could occur when devices are taken to voltages well above their design limits. Figure 6 shows results for EPC2045 devices tested up to 150 V at 75°C and 125°C. Note how the straight-line extrapolation that would occur with a simple log(time) dependence is no longer applicable. By removing the simplified assumption that only a small fraction of Q_P is trapped and become Q_S, the following result is obtained as shown in Equation 5. Calculating Equation 5 using the expanded list of parameters yields the solid lines in Figure 6, giving further evidence of the validity and applicability of this physics-based model.

$$\frac{\Delta R}{R} = a_1\left[\frac{a_2\Psi \log(1+a_3 t/\Psi)}{1-a_2\Psi \log(1+a_3 t/\Psi)}\right]$$

where: $$\Psi \equiv \frac{qF\lambda}{\beta} \quad a_1 \equiv \frac{C}{Q_P} \quad a_2 \equiv \frac{1}{Q_P} \quad a_3 \equiv B \qquad \text{Eq. 5}$$

with the following expanded list of parameters:

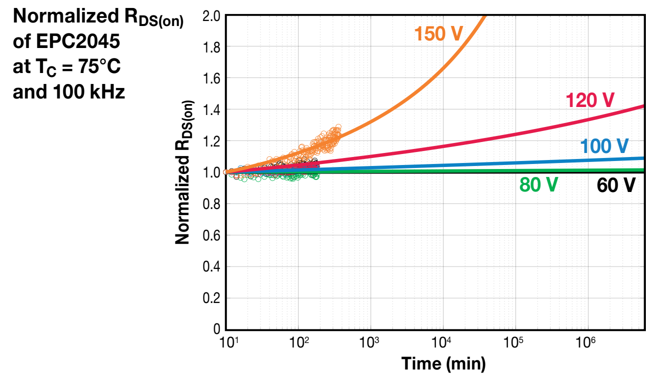
- a_1 = 0.6 (unitless)
- a_2 = b/a_1 (where b = 2.0E-5 $K^{-1/2}$ from [7])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = 100 V (appropriate for Gen5 100 V products only)
- α = 10 (V)
- T = Device temperature (K)
- t = Time (min)

2.3.1 200 V Model

A similar analysis was developed for 200 V GaN transistors.
The resultant variables are as follows:

- a_1 = 0.6 (unitless)
- a_2 = $2.8 \cdot b/a_1$ (where b = 2.0E-5 $K^{-1/2}$ from [7])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = *100V (appropriate for generation 5 100V products, including EPC2045, EPC2204, EPC2218, EPC2071, and EPC2302)*
- α = 25 (V) (appropriate for Gen5 200 V products only)
- T = Device temperature (K)
- t = Time (min)

Figure 7 shows the results from Equation 2 using the variables for 200 V devices. These calculated results are then compared against actual measurements. On the left is the normalized $R_{DS(on)}$ for the fifth-generation, 200 V rated EPC2215 at three voltages. The highest voltage, 280 V, is 40% above the maximum rating. On the right are measurements compared with the model at two different temperature and at the maximum rated voltage.



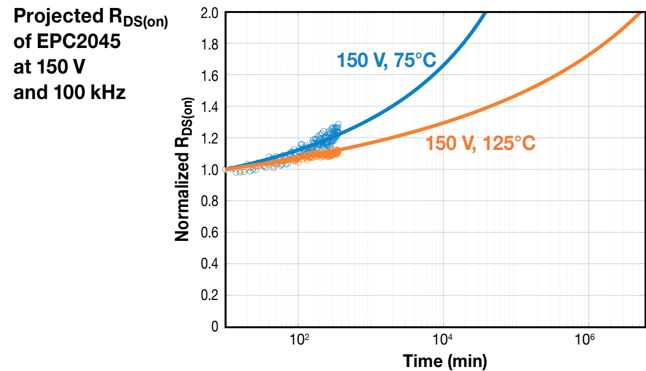
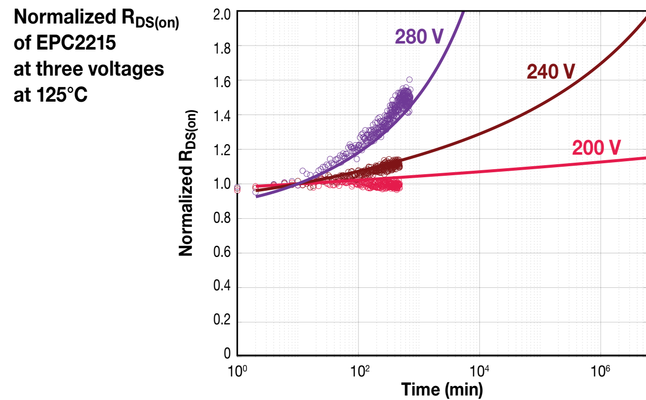


Figure 6: 100 V EPC2045 devices in hard-switching circuit at various voltages up to 150% of design rating (top), and at two different temperatures, also at 150% of design rating (bottom). The solid lines are the model predictions, and the dots represent measurement point.



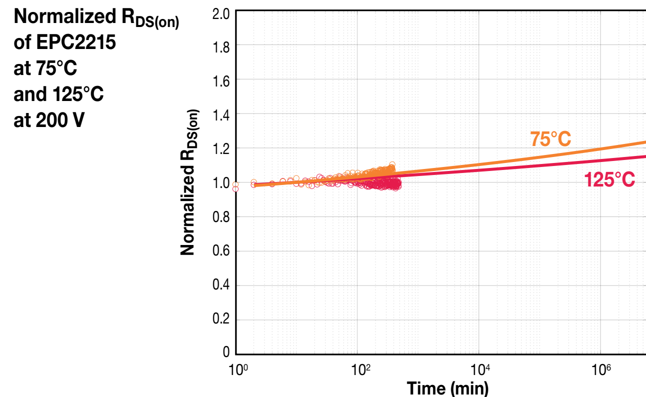


Figure 7: (top) 200 V EPC2215 normalized $R_{DS(on)}$ at three voltages. Note that 280 V is 40% above the maximum rated voltage (bottom). EPC2215 at 75°C and 125°C and 200 V. The solid lines are the results from Equation 2 using variables for 200 V devices, and the dots are actual measurements.

2.4 Conclusions for Physics-Based Dynamic $R_{DS(on)}$ Model

EPC has developed a first principles physics-based model to explain $R_{DS(on)}$ rise in GaN transistors under hard-switching conditions. The model is predicated on the assumption that hot electrons inject over a surface potential into the conduction band of the surface dielectric. Once inside, the electrons quickly fall into deep mid-gap states, where they are assumed to be trapped permanently (no de-trapping). Hot electrons are created during the switching transition, where the transient combination of high injection current and high fields leads to a hot carrier energy distribution with long tails into the high energy regime.

This model predicts the following observations:

- $R_{DS(on)}$ growth with time
- The slope of $R_{DS(on)}$ over time has a negative temperature coefficient (i.e., lower slope as temperature rises).
- Switching frequency does not affect the slope but causes a small vertical offset.
- Switching current does not affect the slope.

The time dependence results from a rapidly self-quenching charge trapping dynamic that involves two inter-twined effects: (1) a hot electron energy distribution that is exponential in energy; and (2) an accumulating surface charge Q_S that steadily raises the barrier for electron injection into the dielectric. The combination of these effects leads to a trapping rate that becomes exponentially slower as charge accumulates, leading to a slow time dependence. As the number of trapped charges approaches the number of available electrons in the 2DEG, the $R_{DS(on)}$ appears to climb faster than a straight log(time) dependence. The trapping mechanism, however, continues to follow a true log(time) dependence.

The negative temperature dependence results from the effect of LO-phonon scattering on the hot carrier energy distribution. At lower temperature, decreased scattering improves the mean free path, allowing electrons to gain higher energy in an electric field.

Key parameters in the mathematical model were fit to measured results for the EPC2045 across a range of drain voltages and temperatures. The model allows users to project long-term $R_{DS(on)}$ growth as a function of four key input variables: drain voltage, temperature, switching frequency, and switching current. The model was adapted to provide a simple MTTF equation, allowing users to predict lifetime under arbitrary conditions.

SECTION 3: SAFE OPERATING AREA

Safe operating area (SOA) testing exposes the GaN transistor to simultaneous high current (I_D) and high voltage (V_{DS}) for a specified pulse duration. The primary purpose is to verify the transistor can be operated without failure at every point (I_D, V_{DS}) within the datasheet SOA graph. It is also used to probe the safety margins by testing to fail outside the safe zone. During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure.

In Si MOSFETs, another failure mechanism known as secondary breakdown (or Spirito effect [2]) has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D, is caused by an unstable feedback between junction temperature and threshold V_{TH}. As the junction temperature rises during a pulse, V_{TH} drops, which can cause pulse current to rise. The rising current, in turn, causes temperature to rise faster, thereby completing a positive feedback loop that leads to thermal runaway and ultimate failure. A goal of this study is to determine if the Spirito effect exists in GaN transistors.

For DC, or long-duration pulses, the SOA capability of the transistor is highly dependent on the heatsinking of the device. This can present a huge technical challenge to assess the true SOA capability, often requiring specialty water-cooled heatsinks. However, for short pulses (< 1 ms), the heatsinking does not impact SOA performance. This is because on short timescales, the heat generated in the junction does not have sufficient time to diffuse to any external heatsink. Instead, all the electrical power is converted to raising the temperature (thermal capacitance) of the GaN film and nearby silicon substrate. As a result of these considerations, SOA tests were conducted at two pulse durations: 1 ms and 100 µs.

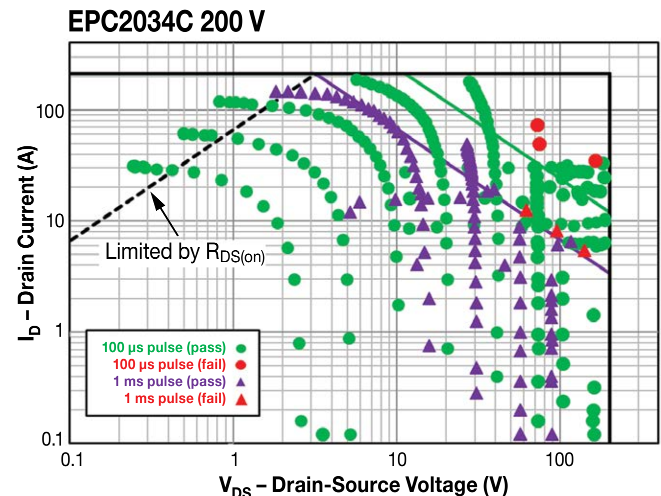


Figure 8: EPC2034C SOA plot. The "Limited by $R_{DS(on)}$" line is based on datasheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the datasheet SOA region.

Figure 8 shows the SOA data of 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D, V_{DS}) space. These points are overlaid on the datasheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. Green dots correspond to 100 µs pulses in which a part passed, whereas red dots indicate where a part failed. A broad area of the SOA was interrogated without any failures (all green dots), ranging from low V_{DS} all the way to V_{DSmax} (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the datasheet graph. The same applies to 1 ms pulse data (purple and red triangles); all failures occurred outside of the datasheet SOA.

Figure 9 provides SOA data for three more parts, AEC EPC2212 (4th generation automotive 100 V), EPC2045 (5th generation 100 V), and EPC2014C (4th generation 40 V). In all cases, the datasheet safe operating area has been interrogated without failures, and all failures occur outside of SOA limits, often well outside the limits.

The datasheet SOA graph is generated with finite element analysis, using a thermal model of the device including all relevant layers along with their heat conductivity and heat capacity. Based on transient simulations, the SOA limits are determined by a simple criterion: for a given pulse duration, the power dissipation must be such that the junction temperature does not exceed 150°C before the end of the pulse. This criterion results in limits based on constant power, denoted by the 45° green (100 µs) and purple (1 ms) lines in the SOA graph. This approach leads to a datasheet graph that defines a conservative safe operating zone, as evidenced by the extensive test data in this study. In power MOSFETs, the same constant power approach leads to an overestimate of capability in the high voltage regime, where failure occurs prematurely due to thermal instability (Spirito effect).

While the exact physics of failure is yet to be determined, the main outcome of this study is clear – GaN transistors will not fail when operated within their datasheet SOA.

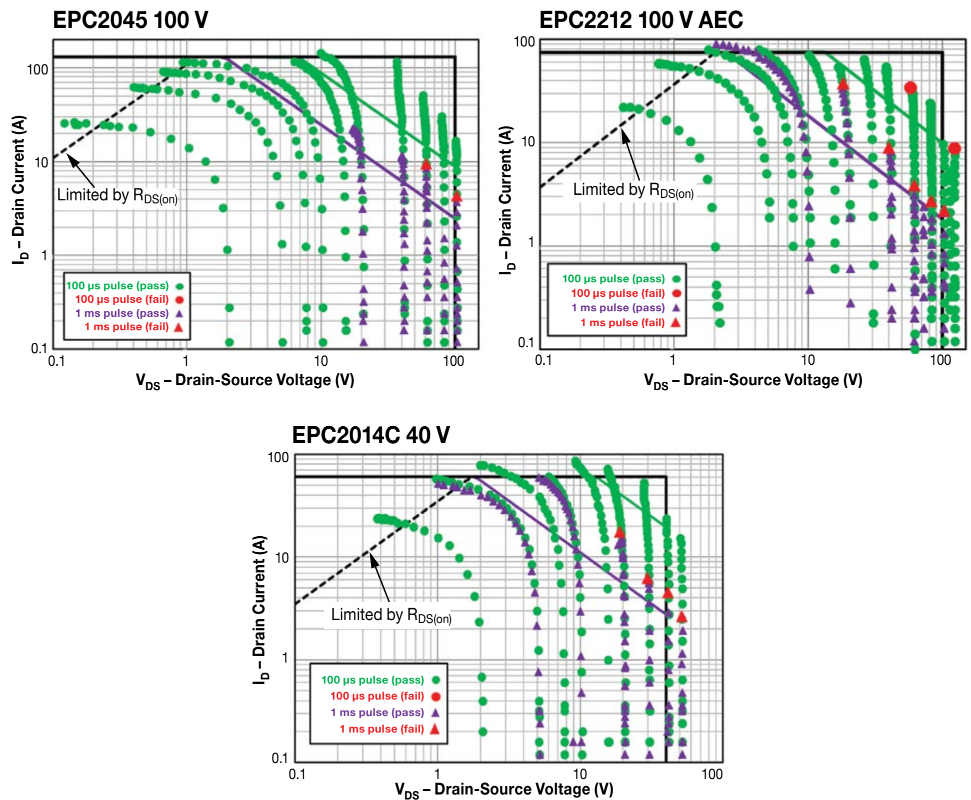


Figure 9: SOA plots for EPC2045 (top-left), EPC2212 (top-right), EPC2014C (bottom). The "Limited by $R_{DS(on)}$" line is based on datasheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the datasheet SOA region.

SECTION 4: SHORT-CIRCUIT ROBUSTNESS TESTING

Short circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in a power converter while in the ON (conducting) state. In such an event, the device will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor and the circuit parasitic resistance, which varies with the application and location of the fault. If the short-circuit state is not quenched by protection circuitry, the extreme power dissipation will ultimately lead to thermal failure of the transistor. The goal of short-circuit testing is to quantify the "withstand time" the part can survive under these conditions.

Typical protection circuits (e.g., de-saturation protection for IGBT gate drivers) can detect and react to over-current conditions in 2–3 µs. It is therefore desirable if the GaN transistor can withstand unclamped short-circuit conditions for about 5 µs or longer.

The two main test circuits used for short-circuit robustness evaluation are described in [8]. They are:

- Hard-switched fault (HSF): gate is switched ON (and OFF) with drain voltage applied
- Fault under load (FUL): drain voltage is switched ON while gate is ON

For this study, devices were tested in both fault modes and no significant differences in the withstand time were found. Therefore, the focus will be on FUL results for the remainder of this discussion. However, it is important to note that from HSF testing, GaN transistors did not exhibit any latching or loss of gate control that can occur in silicon-based IGBTs [9]. This result was expected given the lack of parasitic bipolar structures with the GaN devices. Until the time the transistors fail catastrophically, the short circuit can be fully quenched by switching the gate low, an advantageous feature for protection circuitry design.

Two representative GaN transistors were tested:

1) EPC2203 (80 V): 4th generation automotive grade (AEC) device
2) EPC2051 (100 V): 5th generation device

These devices were chosen because they are the smallest in their product families. This simplified the testing owing to the high currents required for short-circuit evaluation. However, based on simple thermal scaling arguments, the withstand time is expected to be identical for other in-family devices. EPC2203 results cover EPC2202, EPC2206, EPC2201 and EPC2212; EPC2051 covers EPC2045 and EPC2053.

Figure 10 shows fault-under-load data on EPC2203 for a series of increasing drain voltages. With V_{GS} at 6 V (the datasheet maximum), and a 10 µs drain pulse, the device did not fail all the way up to V_{DS} of 60 V. Under these conditions, over 1.5 kW is dissipated in a 0.9 x 0.9 mm die. At the higher V_{DS}, the current is seen to decay over time during the pulse. This is a result of rising junction temperature within the device and does not signify any permanent degradation.

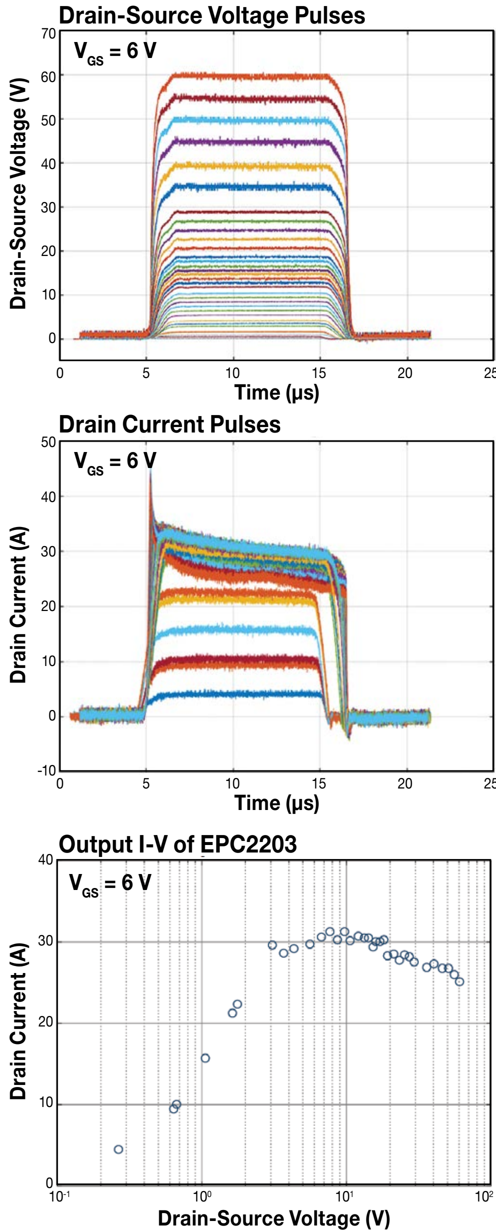


Figure 10: EPC2203 fault under load test (FUL) waveforms for a series of increasing drain voltages. Drain pulse is 10 µs and V_{GS} = 6 V. The device did not fail for this pulse width. V_{DS} vs. time. V_{DS} is Kelvin-sensed directly at the device terminals (top). I_{DS} vs. time. Note that I_{DS} decreases over time due to self-heating (center). Resulting output curve for this test sequence (bottom). Drain current is reported as the average current during the pulse. Drain current rolls over in the saturation region owing to device heating at higher V_{DS}.

Using a longer pulse duration (25 µs), the parts eventually fail from thermal overload. Representative waveforms are shown in Figure 11. The time of failure is marked by the abrupt sharp rise in drain current. After this event, the devices are permanently damaged. The withstand time is measured from the beginning of the pulse to the time of failure.

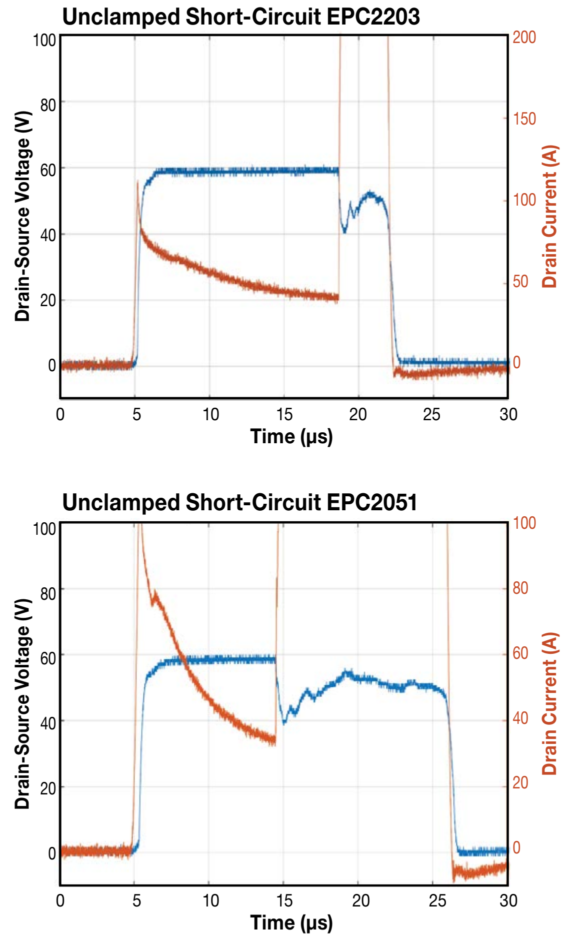


Figure 11: Fault-under-load test waveforms for a typical EPC2203 (top) and EPC2051 (bottom) at V_{DS} = 60 V, V_{GS} = 6 V, and a 25 µs drain pulse. The abrupt rise in drain current marks the time of catastrophic thermal failure.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure using this approach. Table 2 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS(max)}$), with mean withstand time of 20 µs and 13 µs respectively. Note that the device survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 µs) compared with the EPC2203 at 6 V. This is expected because of the more aggressive scaling and current density of 5th generation products. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 2 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was simulated to determine the rise in junction temperature ΔT_J during the short-circuit pulse. The results are shown in Figure 12.

Short-circuit pulse $V_{DS} = 60$ V	EPC2203 (Gen 4)		EPC2051 (Gen 5)	
	$V_{GS} = 6$ V	$V_{GS} = 5$ V	$V_{GS} = 6$ V	$V_{GS} = 5$ V
Mean TTF (µs)	13.1	20.0	9.33	21.87
Std. dev. (µs)	0.78	0.37	0.21	2.95
Min. TTF (µs)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	1.764	1.4	3.03	2.03
Energy (mJ)	23.83	27.6	27.71	42.49
Die area (mm^2)	0.9025		1.105	
Avg power/area (kW/mm^2)	1.95	1.55	2.74	1.84
Energy/area (mJ/mm^2)	26.4	30.59	25.08	38.46

Table 2: Short-circuit withstand time statistics for EPC2203 and EPC2051

Note: Statistics derived from eight devices in each condition. Withstand times are tightly distributed around mean value. Average pulse power and energy correspond to a typical part within the population.

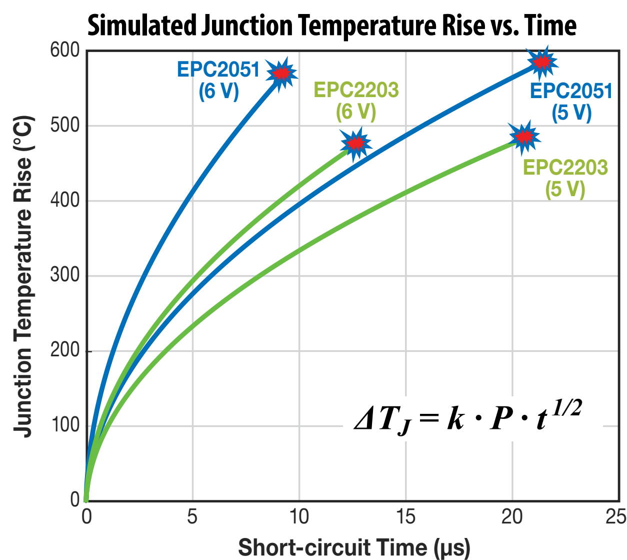


Figure 12: Simulated junction temperature rise versus time during the short-circuit pulses for both EPC2051 and EPC2203 at both 5 and 6 V_{GS}. Measured failure times are indicated by red markers. Note that EPC2203 fails catastrophically at a ΔT_J of around 475°C, whereas EPC2051 fails around 575°C. The simulated ΔT_J is well fit by a simple square root dependence on time (heat diffusion), as shown in the equation. P denotes the average power per unit area, and $k = 6.73 \times 10^{-5}$ K m^2/W $s^{1/2}$.

The intense power density during the pulse leads to rapid heating in the GaN layer and nearby silicon substrate. Because the pulse is short and heat transfer is relatively slow, only a small thickness of semiconductor (< ~100 µm in depth) can help to absorb the energy. The temperature grows as the square root of time (characteristic of heat diffusion), and linearly with the pulse power. As can be seen in Figure 12, for EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of ~475°C. The same is true for EPC2051, where both conditions fail at the same ΔT_J of ~575°C. Three key conclusions stem from these results:

1) For a given device, the time to failure is inversely proportional to the power dissipation squared (P^{-2}). This applies for short-circuit and SOA pulses of duration < ~1 ms.
2) The intrinsic failure mode resulting from high power pulses is directly linked to the junction temperature exceeding a certain critical value.
3) Wide bandgap eGaN devices can survive junction temperatures (> 400°C) that are totally inaccessible to silicon devices owing to free-carrier thermal runaway.

To establish whether devices could survive these extreme conditions repetitively, several parts were subjected to over 500,000 cycles under short-circuit conditions that caused device currents about twice the maximum rated pulse current listed on their datasheets. In the test setup, gate bias of either 5 or 6 V_{DC} was applied to the gate of the device under test (DUT). Drain bias was set at 10 V_{DC} and a 60 mF capacitor was connected across the drain supply. A low $R_{DS(on)}$ high-side transistor in series with the DUT controlled the otherwise unlimited flow of current. The control transistor was then pulsed with 5 µs pulses at 1 Hz to give the channel time to re-equilibrate. Table 3 shows the various types of devices tested, their datasheet rating for maximum pulsed current, and the amount of short-circuit current that pulsed through the device during each cycle at the start of the test.

Device	Type	Datasheet pulsed (A)	V_{GS}	Mean (A)	Sigma (A)
EPC2203	80 V AEC Gen4	17	5	35	2.4
			6	43	2.5
EPC2212	100 V AEC Gen4	75	5	124	2.1
			6	160	3.5
EPC2051	100 V Gen5	37	5	68	1.0
			6	87	1.3
EPC2052	100 V Gen5	74	5	147	1.6
			6	163	2.2
EPC2207	200 V Gen5	54	5	99	4.7
			6	132	5.0

Table 3: Devices tested under extreme pulsed short circuit current, typically twice the maximum datasheet limit

Table 4 shows the various key device parameters for the EPC2051, the same part number as used in Table 3 and in Figure 12. Even under these extreme conditions of 500,000 85 A pulses that are more than twice the datasheet maximum ratings, all electrical characteristics remained within datasheet specifications. There was, however, a small reduction in the amount of short circuit current "consumed" by the DUT over time, consistent with the small increase in VTH. After this 500 k pulse sequence, this part underwent an unbiased 10 minute anneal at 175°C. As can be seen in the right-hand column of Table 4, the electrical parameters and short-circuit current recovered to near their values before being subjected to repetitive pulse stresses. This recovery indicates that no permanent damage occurred from repetitive high-current pulses.

EPC2051	t = 0	100 k pulses	500 k pulses	Post 10 min. 175°C Anneal
V_{TH} (V)	1.8	2	2.1	1.8
I_{GSS} (µA)	11	33	55	23
I_{DSS} (µA)	7	5.5	5.1	5.6
$R_{DS(on)}$ (mΩ)	22	22.3	22.3	22
$I_{short\ circuit}$	84	77	74	82

Table 4: Key device parameters for EPC2051 at the start of pulse testing, after 100 k pulses, after 500 k pulses, and after a 175°C, 10 minute anneal. Device parameters stayed within datasheet limits at all times.

SECTION 5: MECHANICAL STRESS

The ultimate lifetime of a product, or its suitability in a given application, may be limited by the mechanical stresses encountered. In this section, some of the most common mechanical stressors, die shear, backside pressure, and bending force are characterized, and the WLSCP package is demonstrated to be robust under normal assembly or mounting conditions.

5.1 Die Shear Test

The purpose of die shear test is to evaluate the integrity of the solder joints used to attach eGaN devices to PCBs. This determination is based on the in-plane force at which, when applied to a mounted device, the die shears from the PCB. All testing followed the military test standard, MIL-STD-883E, Method 2019 [12].

Figure 13 shows the test results of four selected GaN transistors. Ten parts were tested for each product. The smallest die tested is EPC2036/EPC2203, which only has four solder balls with a diameter of 200 µm and a die area of 0.81 mm². As expected, this product turned out to have the least shear strength, however, it exceeds the minimum force requirement specified by the MIL standard, as shown in Figure 13. The largest die tested was EPC2206, a land grid array (LGA) product with die area of 13.94 mm². EPC2206 exceeds the minimum force requirement more than a factor of ten. Within the size spectrum, two additional products were tested: EPC2212 (100 V LGA) and EPC2034C (200 V BGA). Both products surpassed the minimum force significantly.

In Figure 13, the results show that all WLCSP GaN products are mechanically robust against environmental shear stress under the most stringent conditions.

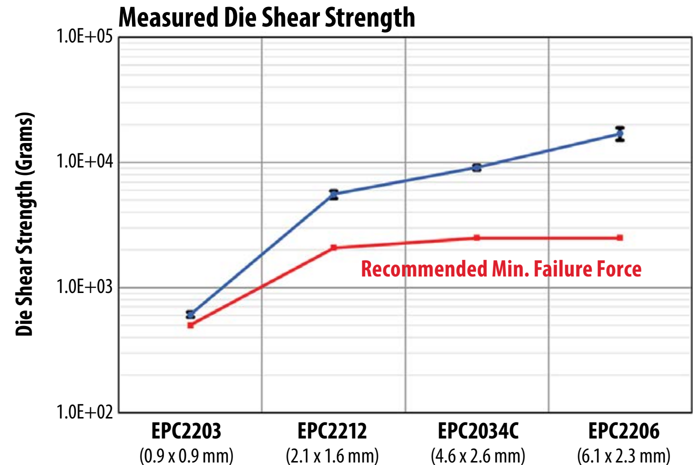


Figure 13: Various die sizes and solder configurations of GaN transistors were tested to failure while measuring the shear strength. The results are shown with black dots. The red dots show the minimum recommended die shear strength under MIL-STD-883E, Method 2019.

5.2 Backside Pressure Test

Another critical aspect of the mechanical robustness of GaN devices is how well they handle backside pressure. This is an important consideration for applications that require backside heatsinking to the die. It is also important to determine the safe "pick-and-place" place force during assembly.

Backside pressure tests up to 400 psi were performed, where the pressure is calculated by the force applied divided by the die area. Figure 44 shows the laboratory pressure tester that was employed. The pressure was applied directly to the backside of the die using a loading speed of 0.6 mm/min. Before and after the pressure test, parametric testing was performed to determine pass or fail. Subsequently, the parts were exposed to humidity-bias testing (H3TRB) at 60 V_{DS}, 85°C, and 85% relative humidity for 300 hours. H3TRB is effective to determine if there were any latent failures caused by mechanical damage (internal cracking) from the pressure test.

EPC2212 (100 V, LGA) and EPC2034C (200 V, BGA) were tested and both passed 400 psi. The data is included in Table 5. These results show that eGaN FETs have enough margin to handle backside pressure that is normally used at a PCB assembly house. Though these parts survived 400 psi, EPC recommends limiting maximum backside pressure to 50 psi or less.

Product	Sample Size	Die Area	Backside Pressure	Force Applied	Failures in Parametric Test after Pessure Test	Failures after 300 hours H3TRB test
EPC2212 (LGA)	16	2.1 x 1.6 mm	400 psi	9.3 N (2.1 lbs)	0/16	0/16
EPC2034C (BGA)	16	4.6 x 2.6 mm	400 psi	33.0 N (7.4 lbs)	0/16	0/16

Table 5: eGaN device pressure test results

Note: Small and relatively large eGaN devices were tested under high backside pressure with no mechanical failures, and no failures after stress testing under temperature, humidity, and bias.

5.3 Bending Force Test

The purpose of the bending force test is to determine the ability of a GaN transistor to withstand flexure of the PCB, which might occur during handling, assembly, or operation. Though this test standard was developed for passive surface mount components (AEC-Q200) [13], many customers have concerns about bending forces on GaN transistors for two main reasons:

1. Robustness of the WLCSP solder joints;
2. Piezoelectric effects within the transistor that may alter device parametric values and disrupt circuit operation.

To address these concerns, bending force testing on four EPC2206 devices following the AEC-Q200-005A test standard [14] were conducted. Devices are assembled near the center of an FR4 PCB (100 mm long x 40 mm wide x 1.6 mm thick). With ends rigidly clamped, a force is applied on the opposite side from the device, leading to an upward deflection of the PCB. After a 60 second dwell in this flexed state, all device electrical parameters are measured.

Table 6 shows normalized $R_{DS(on)}$ versus board deflection for all four devices under test. All devices passed the 2 mm test requirement. Two devices failed at 6 mm deflection, while the remaining two survived all the way to 8 mm. Postmortem analysis revealed that the failure mode was solder joint cracking, leading to an open gate connection. Up until failure, $R_{DS(on)}$ did not show any appreciable response to board flexure. The same result was observed in other electrical characteristics like V_{TH} and I_{DSS}.

	0 mm	2 mm	4 mm	6 mm	8 mm
DUT1	1.00	1.01	1.00	0.98	0.98
DUT2	1.00	1.02	1.01	*Failed*	-
DUT3	1.00	1.01	1.03	*Failed*	-
DUT4	1.00	0.99	0.99	1.03	1.04

Table 6:. Normalized $R_{DS(on)}$ versus board deflection for four devices during bending force test

Note: Values are normalized to the $R_{DS(on)}$ in the unflexed case. Two of four devices failed at 6 mm deflection, while the remaining two devices survived 8 mm. No significant stress response was seen in any device parameter.

SECTION 6: THERMO-MECHANICAL STRESS

GaN transistors in WLCSP have excellent thermo-mechanical reliability when tested according to AEC or JEDEC standards. This is because of the inherent simplicity of the "package," the lack of wire bonds, no use of dissimilar materials, or presence of mold compound . In summary, all WLCSP GaN transistors are capable of –40°C to 150°C in bare die form.

In addition to the component-level reliability, there are other industry specific standards like IPC-9592, or OEM environmental requirements that impose system or board-level tests for components mounted on a PCB. Among these, there is always a subset that induces severe thermo-mechanical stress on surface-mounted parts such as GaN transistors, and especially on the solder joints between the parts and the board. For instance, the most stringent temperature cycling requirement (Class II, Category 2) from the IPC-9592 standard calls for 700 cycles at –40°C to 125°C without failure in a sample size of 30 units. The reliability of the solder attachments depends on several factors that are independent of the device, including the PCB layout, the design and material, the assembly process, the heatsinking solution in operation, and the nature of the application. Therefore, providing a precise model to predict time to failure in a particular application becomes infeasible and impractical. Nevertheless, in the past, EPC published a model to predict time to failure of solder joints based on the correlation between strain energy density and fatigue lifetime [15].

More Temperature Cycling, and Intermittent Operating Life (also known as Power Temperature Cycling) results are presented under different conditions. In addition, this section provides data and analysis on how to improve solder joint reliability with the use of underfill materials. Underfills are commonly used in applications that may expose surface-mount devices to the harshest environmental conditions.

It is important to emphasize that underfill is not required to ensure proper operation of WLCSP GaN transistors. In fact, for most of the reliability tests conducted during product qualification, the devices under test are mounted on FR4 boards with no underfill. The list of tests includes HTRB, HTGB, H3TRB, uHAST, MSL1, IOL, HTOL, ELFR, HTS, and in many cases, TC. However, underfill may be used for improved board-level reliability, since it reduces the stress on the solder joints resulting from coefficient of thermal expansion (CTE) mismatches between the die and PCB. Moreover, underfill provides pollution protection and additional electrical isolation in those cases with strict creepage and clearance requirements. Finally, underfill also helps in reducing the junction-to-board thermal impedance since the materials used have higher thermal conductivity than air, although lower than typical thermal interface materials. Note that the incorrect choice of an underfill material could also worsen solder joint reliability. Therefore, this section provides guidelines for the selection of underfill based on simulation and experimental results.

6.1 Criteria for Choosing a Suitable Underfill

The selection of underfill material should consider a few key properties of the material as well as the die and solder interconnections. Firstly, the glass transition temperature of the underfill material should be higher than the maximum operating temperature in application. Also, the CTE of the underfill needs to be as close as possible to that of the solder since both will need to expand/contract at the same rate to avoid additional tensile/compressive stress in the solder joints. As a reference, typical lead-free SAC305 and Sn63/Pb37 have CTEs of approximately 23 ppm/°C. Note that when operating above the glass transition temperature (Tg), the CTE increases drastically. Besides Tg, and CTE, the Young Modulus is also important. A very stiff underfill can help reduce the shear stress in the solder bump, but it increases the stress at the corner of the device, as it will be shown later in this section. Low viscosity (to improve underfill flow under the die) and high thermal conductivity are also desirable properties. Table 7 compares the key material properties of the underfills tested in this study.

Manufacturer	Part number	CTE (ppm/C)			Storage modulus (DMA) at 25°C (N/mm^2)	Viscosity at 25°C	Poisson's ratio	Volume resistivity	Thermal conductivity	Dielectric strength
		Tg (TMA) [C]	Below Tg	Above Tg						
HENKELS LOCTITE	ECCOBOND-UF 1173	160	26	103	6000	7.5 Pa*S				
NAMICS	U8437-2	137	32	100	8500	40 Pa*S	0.33	>1E15 Ω-cm	0.67 W/m·K	
NAMCIS	XS8410-406	138	19	70	13000	30 Pa*S				
MASTERBOND	EP3UF	70	25-30	75-120	3400	10-40 Pa*S	0.3	>1E14 Ω-cm	1.4 W/m·K	450 V/mil
AI TECHNOLOGY	MC7885-UF	236	20		7500	10 Pa*S		>1E14 Ω-cm	1 W/m·K	750 V/mil
AI TECHNOLOGY	MC7885-UFS	175	25		7500	10 Pa*S		>1E14 Ω-cm	2 W/m·K	1000 V/mil

Table 7: Underfill material properties

6.2 Underfill Study under Temperature Cycling

This section provides Temperature Cycling (TC) results of various GaN transistors under two different conditions, with and without the underfill materials listed earlier. Two temperature cycle ranges were tested: (i) –40°C to 125°C; and (ii) –55°C to 150°C. For all cases, the parts were mounted on DUT cards or coupons consisting of a 2-layer, 1.6- mm thick, FR4 board. SAC305 solder paste, and water-soluble flux was used, followed by a flux clean process prior to the underfill. Temperature Cycling data for EPC2701C and EPC2053 are provided in Tables 8 through 11 and results for EPC2206 are provided in the Weibull plot in Figure 14.

Product/DOE	EPC2001C										
Stress condition: -40°C to 125°C	Status	300 cycles	550 cycles	850 cycles	1000 cycles	1250 cycles	1550 cycles	1750 cycles	1950 cycles	2150 cycles	2450 cycles
No Underfill	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	2/32 fails	5/32 fails	8/32 fails	15/32 fails	20/32 fails	26/32 fails
	On-going	0/32 fail	0/32 fail	0/32 fail	0/32 fail						
Henkels UF1137_H	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					
Masterbond EP3UF_M	On-going	0/40 fail	0/40 fail	14/40 fails	31/40 fails						
MC7685-UFS	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	2/32 fails	2/32 fails	3/32 fails	6/32 fails	14/32 fails
MC7885-UF	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	4/32 fails
Namics 8410-406B	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
Namics U8437-2_N	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
	On-going	0/80 fail	0/80 fail	0/80 fail	0/80 fail	0/80 fail					

Table 8: –40°C to 125°C Temperature Cycling results for EPC2001C

Product/DOE	EPC2053										
Stress condition: -40°C to 125°C	Status	300 cycles	550 cycles	850 cycles	1000 cycles	1250 cycles	1550 cycles	1750 cycles	1950 cycles	2150 cycles	2450 cycles
No Underfill	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	2/32 fails	3/32 fails	3/32 fails	3/32 fails
Henkels UF1137_H	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					
Masterbond EP3UF_M	On-going	1/40 fails	7/40 fails	15/40 fails	25/40 fails	39/40 fails					
MC7685-UFS	Completed	0/32 fail	0/32 fail	0/32 fail	1/32 fails	17/32 fails	32/32 fails	32/32 fails			
MC7885-UF	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	1/32 fails	1/32 fails
Namics 8410-406B	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
Namics U8437-2_N	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					

Table 9: –40°C to 125°C Temperature Cycling results for EPC2053.

Product/DOE	EPC2001C					
Stress condition: -55°C to 150°C	Status	300 cycles	600 cycles	900 cycles	1100 cycles	1300 cycles
No Underfill	Completed	0/16 fail	0/16 fail	1/16 fails	1/16 fails	2/16 fails
Henkels UF1137_H	On-going	0/20 fail	0/20 fail	0/20 fail	1/20 fails	
Masterbond EP3UF_M	On-going	0/20 fail	0/20 fail	4/20 fails	6/20 fails	
MC7685-UFS	Completed	0/16 fail	0/16 fail	0/16 fail	1/16 fails	1/16 fails
MC7885-UF	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics 8410-406B	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics U8437-2_N	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
	On-going	0/20 fail	0/20 fail	0/20 fail	0/20 fail	

Table 10: –55°C to 150°C Temperature Cycling results for EPC2001C

Product/DOE	EPC2053					
Stress condition: -55°C to 150°C	Status	300 cycles	600 cycles	900 cycles	1100 cycles	1300 cycles
No Underfill	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	1/16 fails
Henkels UF1137_H	On-going	0/20 fail	0/20 fail	0/20 fail	0/20 fail	
Masterbond EP3UF_M	On-going	5/20 fails	15/20 fails			
MC7685-UFS	Completed	1/16 fails	9/16 fails	13/16 fails		
MC7885-UF	Completed	2/16 fails	1/16 fails	7/16 fails		
Namics 8410-406B	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail
Namics U8437-2_N	Completed	0/16 fail	0/16 fail	0/16 fail	0/16 fail	0/16 fail

Table 11: –55°C to 150°C Temperature Cycling results for EPC2053

For both temperature ranges, the Namics underfills (U8437-2_N and 8410-406B) provide a large lifetime advantage compared to no underfill. The same applies to the Henkels (UF1137_H). On the other hand, Masterbond EP3UF was found to degrade the reliability. This was primarily the result of the low Tg, which meant that the underfill was exercised well beyond its glass transition temperature in all our studies. However, based on material properties, it is suspected that Masterbond EP3UF may be a suitable candidate for applications staying below 70°C.

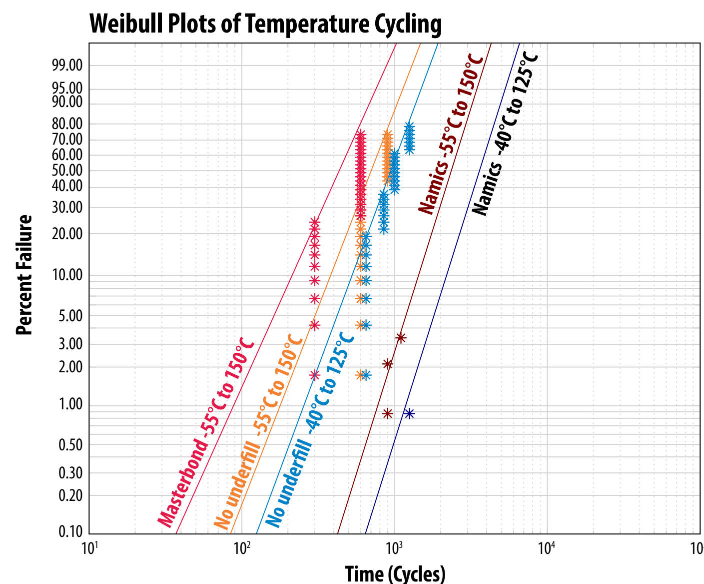


Figure 14: Weibull plots of Temperature Cycling results of EPC2206

6.3 Intermittent Operating Life Study

In Temperature Cycling, both the device and PCB are placed inside a chamber that cycles the ambient temperature, leading to an isothermal temperature change across the assembly. In Intermittent Operating Life (IOL), temperature rise is realized by dissipating power inside the device. Therefore, in IOL only the device and the PCB in the vicinity of the die change in temperature. As a result, the stresses on the solder joints resulting from the CTE mismatch between the GaN transistors and PCB are not as high as in Temperature Cycling. However, the time to complete a full cycle is much faster than in TC (Note that IOL may also be known as Power Temperature Cycling).

Figure 15 shows the results of a group of 32 samples of EPC2206 tested to failure under two different conditions. In all cases, each cycle consisted of a heating period of 30 seconds, followed by a cooling period of another 30 seconds. In Figure 16, information in blue shows the devices that were cycled between 40°C and 100°C, and in orange, the devices cycled between 40°C and 150°C. In both cases, solder fatigue is the only failure mechanism, so the slopes of the Weibull fits are almost the same. However, the Mean Time to Failure was strongly accelerated by the ΔT and T_{max} reached during each cycle.

In addition, a third cohort of parts using underfill Namics U8437-2 was started cycling between 40°C and 150°C. After 53,000 cycles no failures were observed. The green line in Figure 16 assumes one failure after 53,001 cycles, and therefore can be viewed as a lower bound on the performance of this underfill. Clearly, as was found in the TC studies, the Namics underfill was found to deliver a significant improvement (> 100x) in lifetime under cyclic temperature stress.

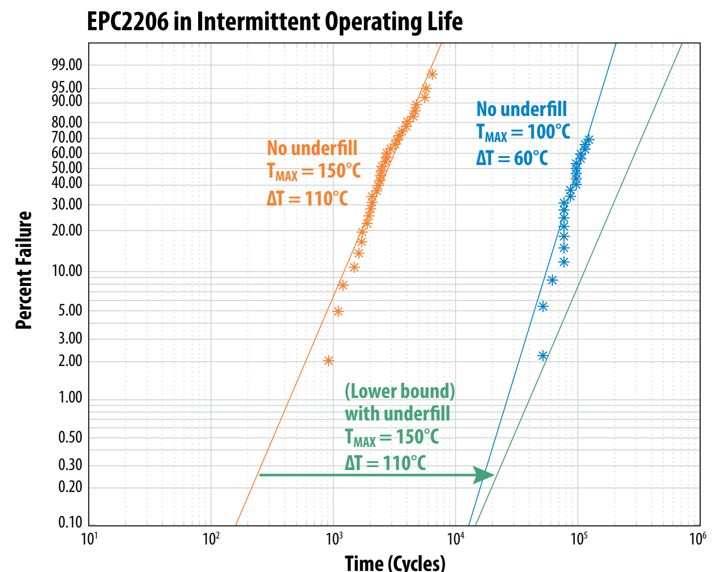


Figure 15: Weibull plots of Intermittent Operating Life results for EPC2206.

6.4 Guidelines for Choosing Underfill

The main guidelines for choosing an underfill for use with eGaN FETs are listed below:

- Underfill CTE should be in the range of 16 to 32 ppm/°C, centered around the CTE of the solder joint (24 ppm/°C). Lower values within this range are preferred because they provide better matching to the die and PCB.
- Glass transition temperature (Tg) should be comfortably above the maximum operating temperature. When operated above Tg, the underfill loses its stiffness and ceases to protect the solder joint.
- Young's (or Storage) modulus in the range of 6–13 GPa. If the modulus is too low, the underfill is compliant and does not relieve stress from the solder joints. If it is too high, the high stresses begin to concentrate at the die edges.

From the experimental results in this study, Henkels UF1137_H and Namics 8410-406B and U8437-2_N underfills provide excellent boost in thermo-mechanical reliability when used with eGaN FETs.

SECTION 7: RELIABILITY TEST RESULTS FOR GaN-ON-Si LASER DRIVERS

7.1 Long-Term Stability Under High Current Pulses

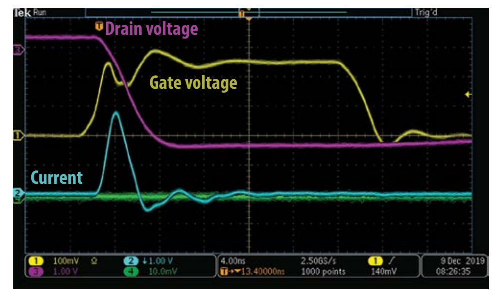
The concept of this test method is to stress parts in an actual lidar circuit for a total number of pulses well beyond their ultimate mission profile. The mission profiles for automotive lidar vary from customer to customer. A typical automotive profile would call for a 15-year life, with two hours of operation per day, at 100 kHz pulse repetition frequency (PRF). This corresponds to approximately four trillion total lidar pulses. Some worst-case (heavy use) scenarios might call for as many as 10–12 trillion pulses in service life.

By testing a population of devices well beyond the end of their full mission profile while verifying the stability of the system performance and the device characteristics, this test method directly demonstrates the lifetime of eGaN devices in a lidar mission.

To achieve the large number of pulses, parts are stressed continuously at a pulse repetition frequency (PRF) much higher than in typical lidar circuits.

For this study, two popular AEC grade parts were put under test: EPC2202 (80 V) and EPC2212 (100 V). Four parts of each type were tested simultaneously. During the stress, two key parameters were continuously monitored on every device: (1) peak pulse current and (2) pulse width. These parameters are both critical to the range and resolution of a lidar system.

Figures 16 and 17 show the results of this test over the first 13 trillion pulses. The cumulative number of pulses well exceeds a typical automotive lifetime and covers worst-case use conditions. Note that there is no observed degradation or drift in either the pulse width or height. While this is an indirect monitor of the health of the GaN device, it indicates that no degradation mechanisms have occurred that would adversely impact lidar performance.



AEC-Q101 series of discrete FETs

- 8 samples (>7000h)
- 0 failures and perfect pulse stability

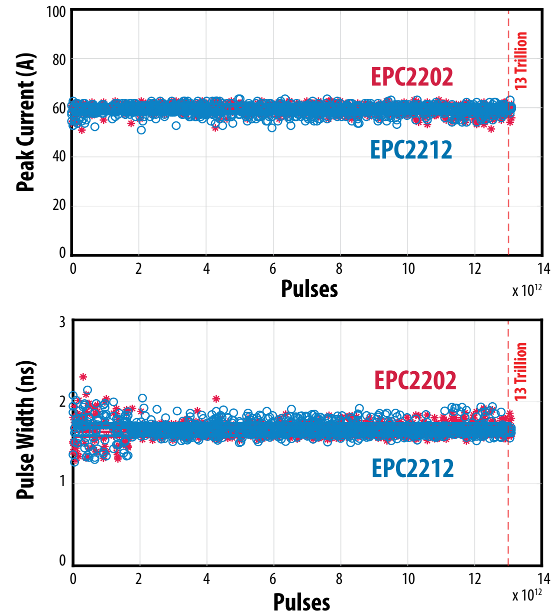
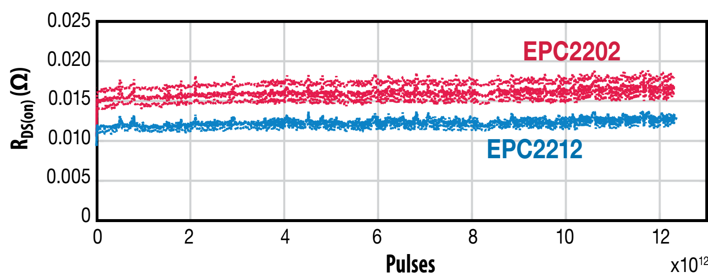


Figure 16: Long-term stability of pulse width (bottom and pulse height (middle) over 13-trillion lidar pulses. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots.

Note the excellent stability of these key parameters over a total number of pulses corresponding to an automotive lifetime in heavy-use conditions.



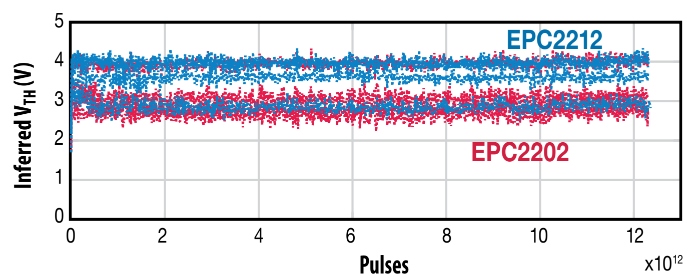


Figure 17: Long-term stability of $R_{DS(on)}$ and V_{TH} during lidar reliability testing. These parameters are measured at six-hour intervals on every part by briefly interrupting the lidar stress. Note that V_{TH} is inferred by measuring $R_{DS(on)}$ at a series of gate voltages. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots. Note the excellent stability of these key parameters over 13 trillion pulses, corresponding to an automotive lifetime under heavy-use conditions.

7.2 Monolithic GaN-on-Si laser driver ICs

The multiple-chip discrete solutions using eGaN transistors are widely implemented in time of flight (ToF) light detection & ranging (lidar) systems due to the benefits of small footprint and superior switching performance. EPC recently introduced a new family of GaN laser drive IC products that integrates a high-speed GaN driver with the discrete GaN transistor (see Figure 18). This integrated monolithic lidar solution offers even higher performance, smaller form factor, and lower cost than the existing discrete solutions. As a result, it enables a wider range of lidar applications including robotics, surveillance systems, drones, autonomous cars, vacuum cleaners, and many more.

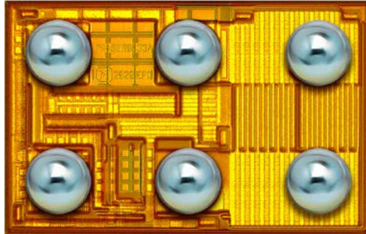


Figure 18: The EPC21601 eToF™ integrated circuit includes a driver and a power FET.

The first two offerings of the integrated GaN laser drive IC products (EPC21601 and EPC21701) are in production. Table 12 summarizes the main specifications of the first two qualified IC products.

Part Number	Die Size (mm x mm)	Main Specifications
EPC21601	S (1.5 X 1)	40 V, 15 A, 3.3 V logic, eToF laser driver IC
EPC21701	S (1.7 X 1)	80 V, 15 A, 3.3 V logic, eToF laser driver IC

Table 12: Initial EPC Laser Driver IC Product Family

7.2.1 Qualification Test Overview

EPC21601 and EPC21701 were subjected to a wide variety of stress tests according to JEDEC standard JESD47K. The stress tests include the following:

- High Temperature Operating Life (HTOL): Parts are subjected to the maximum recommended operating conditions at T_J = 125°C for 1000 hours.
- Temperature Humidity Bias (THB): Parts are tested at the maximum recommended operating conditions while exposed to ambient temperature of 85°C and 85% relative humidity (RH) for 1000 hours.
- High Temperature Storage Life (HTSL): Parts are subjected to a bake at 150°C for 1000 hours.
- Preconditioning (PC): Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1) conditions (see MSL1 details below); (3) three times reflow.
- Unbiased highly accelerated test (uHAST): Parts are stressed in a non-condensing humid environment for 96 hours at 130°C, 85% RH, and at a vapor pressure of 33.3 psia.
- Temperature cycling (TC): Parts are subjected to alternating low and high temperature extremes from -40°C to +125°C for a total of 850 cycles.
- MSL1: Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.

All devices tested in this qualification underwent external visual inspection. Chips were inspected using an optical microscope to check for signs of physical damage to the chip-scale package, e.g., edge chipping or cracks, resulting from assembly, transit, or inadequate handling. Damaged parts were removed from the test population.

Parametric measurements were performed at 25 °C on all the samples before and after the stress to verify compliance with the specifications listed on the product datasheet. The parameters measured include quiescent and operating currents of the driver (V_{DD} pin), DC static parameters of the output transistor such as threshold voltage and drain-source leakage current, input threshold voltages and hysteresis for the logic input signal (V_{IN}).

For all the qualification tests, parts were mounted onto high Tg FR-4 adaptor cards with four layers and 1.6-mm thick. Type-4 SAC305 solder paste with water-soluble (W/S) flux was used for mounting the parts onto the adaptor cards. After assembly, flux residue was cleaned using deionized (DI) water.

7.2.1.1 High Temperature Operating Life (HTOL)

Parts were subjected to the maximum recommended operating voltages at the maximum recommended operating temperature for a stress period of 1000 hours. As shown in Table 13, three lots and 77 samples per lot were tested for EPC21601 and EPC21701, respectively. The test was conducted in accordance with JESD22-A108.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	**EPC21601**	S (1.5 x 1)	T_J = 125°C, V_{DD} = 5.5 V, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3$V_{P\text{-}P,}$ (10-pulse burst; burst frequency = 1 kHz; pulse frequency = 25-30 MHz)	0	77 x 3	1000
HTOL	**EPC21701**	S (1.7 x 1)	T_J = 125°C, V_{DD} = 5.5 V, V_{D_DC} = 60 V, R_{LOAD} = 4 Ω V_{IN} = 3.3$V_{P\text{-}P,}$ (10-pulse burst; burst frequency = 1 kHz; pulse frequency = 25-30 MHz)	0	77 x 3	1000

Table 13: High Temperature Operating Life Test

7.2.1.2 Temperature Humidity Bias (THB)

Parts were subjected to maximum recommended operating voltages (V_{D_DC} = 30 V for EPC21601 and V_{D_DC} = 60 V for EPC21701 and V_{DD} = 5.5 V) and 85°C and 85% relative humidity for a stress period of 1000 hours. The results are shown in Table 14 below, three lots and 25 samples per lot were tested. Stress testing was conducted in accordance with JESD22-A101.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
THB	**EPC21601**	S (1.5 x 1)	T_A = 85°C, R_H = 85%, V_{DD} = 5.5 V, V_{D_DC} = 30 V, V_{IN} = 0 V	0	25 x 3	1000
THB	**EPC21701**	S (1.7 x 1)	T_A = 85°C, R_H = 85%, V_{DD} = 5.5 V, V_{D_DC} = 60 V, V_{IN} = 0 V	0	25 x 3	1000

Table 14: Temperature Humidity Bias Test

7.2.1.3 High Temperature Storage Life (HTSL)

Three lots of EPC21601 and one lot of EPC21701 (25 parts per lot) were subjected to an ambient temperature of 150°C for a total of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTS	**EPC21601**	S (1.5 x 1)	T_A = 150°C Air, Unbiased	0	25 x 3	1000
HTS	**EPC21701**	S (1.7 x 1)		0	25 x 1	1000

Table 15: Temperature Humidity Bias Test

7.2.1.4 Unbiased Highly Accelerated Test (uHAST)

Three lots of EPC21601 and one lot of EPC21701 (25 parts per lot) were subjected to 96 hours at a temperature of 130°C, relative humidity of 85%, and a vapor pressure of 33.3 psia, as summarized in Table 16 below.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
uHAST	**EPC21601**	S (1.5 x 1)	T_A = 130°C, RH = 85% VP = 33.3 psia, Unbiased	0	25 x 3	96
uHAST	**EPC21701**	S (1.7 x 1)		0	25 x 1	96

Table 16: Unbiased Highly Accelerated Test

7.2.1.5 Temperature Cycling (TC)

Three lots of EPC21601 and three lots of EPC21701 (25 parts per lot) were subjected to temperature cycling between –40°C and 125°C for a total of 850 cycles. In accordance with JEDEC Standard JESD22-A104. The minimum dwell time was five minutes, and heating/cooling rates were approximately 15°C per minute.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
TC	**EPC21601**	S (1.5 x 1)	T_A = -40°C to +125°C, Unbiased	0	25 x 3	850
TC	**EPC21701**	S (1.7 x 1)		0	25 x 3	850

Table 17: Unbiased Highly Accelerated Test

7.2.1.6 Moisture Sensitivity Level 1 (MSL1)

Parts were subjected to MSL1 conditions in accordance with the IPC/JEDEC joint Standard J-STD-020 for Pb-free solder.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	**EPC21601**	S (1.5 x 1)	T_A = 85°C, R_H = 85%, 3x relfow	0	25 x 3	168
MSL1	**EPC21701**	S (1.7 x 1)		0	25 x 3	168

Table 18: Moisture Sensitivity Level Test

7.2.1.7 Electrostatic Discharge (ESD) Sensitivity

One lot of EPC21601 and one lot of EPC21701 were subjected to ESD sensitivity test using the human body model (HBM). Testing was conducted according to JS-001-2017 JEDEC standard. Device parameters were measured before and after ESD testing. Results are shown in Table 19 below. EPC21701 passed HBM with a rating of 500 V and EPC21601 passed HBM with a rating of 250 V.

The charged device model (CDM) rating is highly dependent on the total package size of the device, where a smaller part is less susceptible to the CDM damage at a given voltage as compared to a larger one [16]. EPC21601 and EPC21701 are both chip scale package (CSP) products that do not have a package. In addition, the active die areas of both devices are very small, which are measured at 1.87 mm^2 and 1.65 mm^2, respectively. CDM testing was previously conducted on a large quantity of CSP products by EPC that have significantly larger die size than EPC21601 and EPC21701, where 1 kV CDM rating was tested consistently. Therefore, both EPC21601 and EPC21701 shall be capable of a CDM rating of 1 kV by matrix.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	EPC21601	S (1.5 x 1)	250 V	0	3 x 1
ESD-HBM	EPC21701	S (1.7 x 1)	500 V	0	3 x 1

Table 19: Electrostatic Discharge (ESD) Sensitivity

7.2.2 Test-to-Fail Methodology

The goal of standard qualification testing is to have zero failures out of a relatively large group of parts tested for an extended period, or for a certain number of cycles. The challenge of this test-to-pass approach is the difficulty of applying the qualification testing results to different mission profiles or using them to accurately predict the lifetimes at a given operating condition.

Therefore, testing devices to the point of failure is warranted as it enables the development of an understanding of the amount of the margin between data sheet limits and a given mission profile. Next, conducting failure analysis to understand the intrinsic underlying failure mechanisms is equally critical. By developing an understanding of the fundamental root causes, the safe operating life of a product can be determined over a more general set of operating conditions.

7.2.3 Key Stressors of eToF Laser Driver IC for Lidar Application

The integration of the GaN gate driver and eGaN power transistor into a chip-scale package greatly reduces the parasitic inductances and further improves the speed, minimum pulse width and power dissipation. It also introduces challenges to isolate the key stressors because many of the devices are integrated and cannot be accessed directly. The first step of the study is to identify the key stressors that are encountered by the IC device at corner operation conditions in lidar applications.

Both EPC21601 and EPC21701 are selling in a chip-scale BGA form factor that measure at 1.5 x 1.0 mm and 1.7 x 1.0 mm, respectively. The package technology of the laser driver ICs has been used in EPC's discrete power transistors for many years, and therefore the package related reliability of the IC products was covered by previous phase reliability testing reports and related publications [2,6,17–22].

In this Phase 15 report, the focus of testing and failure analysis is on the IC device level. High temperature Operating Life (HTOL) best emulates the lidar operating conditions (see Figure 19a), thus HTOL is chosen as the test used to investigate the impact of different accelerated bias conditions and temperatures over an extended period of time.

EPC21601 is selected as the test vehicle for this test-to-fail study as it was released a few months earlier than EPC21701. The laser driver circuit design of the two products is identical. The main difference between them is the drain voltage rating of the output GaN transistor, where EPC21601 has an absolute V_D max rating of 40 V and EPC2701 is 80 V.

As with EPC21601 laser driver ICs, three key stressors are identified and summarized below:

- V_{DD} is the logic supply voltage that supplies the drive voltage to the low voltage (LV) GaN FETs in laser driver circuit as well as high voltage (HV) GaN FET for the output transistor.
- V_D is the laser drive voltage that is predominantly applied to the drain terminal of the HV output GaN transistor.
- Operating frequency is another stressor that is consequential to the lidar operation.

7.2.4 V_{DD}, Logic Supply Voltage

When EPC21601 is under operation by generating a burst of short pulses, the logic supply voltage (V_{DD}) is applied to the gate terminals of the LV GaN FETs in the laser driver circuits and the gate of the HV GaN power transistor. It is equivalent of performing a dynamic gate test for all GaN FETs with a burst frequency of 1 kHz and very low duty cycle (~0.02%) and high operating frequency. When not being pulsed, the part is in the OFF state and the gate bias is nearly zero (see Figure 19b).

In the qualification HTOL test, V_{DD} was biased at the absolute maximum rating of 5.5 V, and no issue was found after 1000 hours of testing at 125°C junction temperature. To test the device's robustness, the V_{DD} voltage was increased to a high value at 7 V, which is more than 125% of the absolute maximum rating. This stress condition addresses the worst overvoltage ringing issue on the V_{DD} pin during normal operation by customers. Table 20 summarizes the test result where 16 devices were tested up to 1049 hours at 7 V V_{DD} and 125°C junction temperature. No failures occurred. This indicates a significant margin exists in the laser drive IC products.

As there were zero failures, this result does not determine how much margin was designed into the product or to accurately predict the lifetime at a given mission profile for the V_{DD} stressor. Therefore, more stringent stress conditions must be applied to test the devices to failure, where the goal is to fail the parts quickly and conduct failure analysis to understand the underlying failure modes and mechanisms.

To determine the voltage acceleration of the V_{DD} stress, a matrix of tests was conducted from 8.5 V to 9.5 V at 25°C, as shown in Table 21. At 8.5 V V_{DD}, a total of three failures were found after more than 1000 hours of testing whereas almost all parts failed within 305 hours at 9.5 V, indicating a significant voltage acceleration.

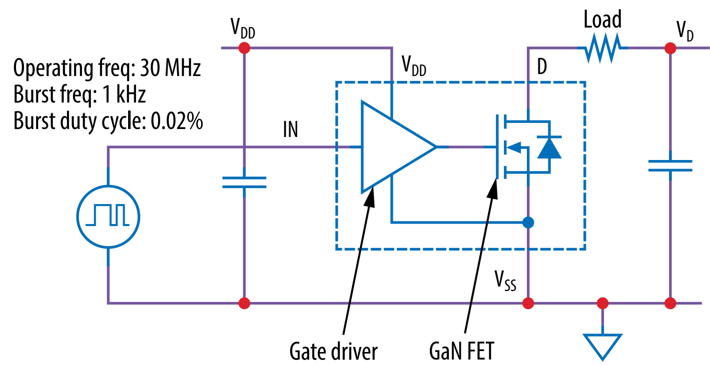


Figure 19a: Block diagram of EPC21601 and EPC21701 laser drive integrated circuits

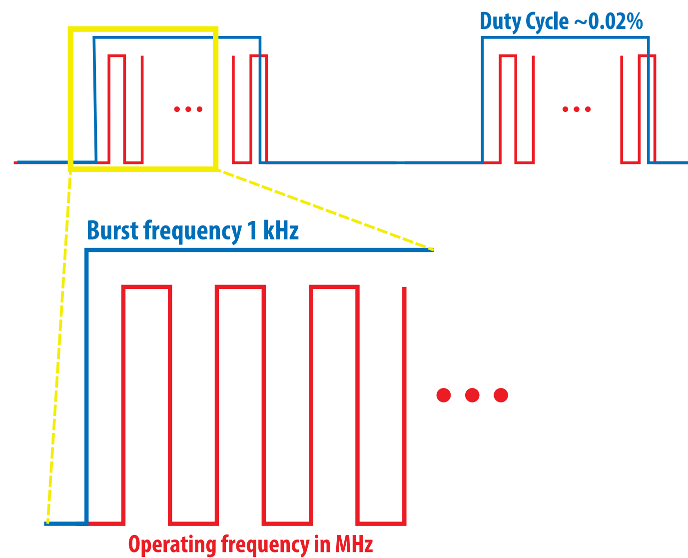


Figure 19b: Diagram of operating conditions with burst frequency (Blue) 1 kHz with a duty cycle of ~0.02% andoperating frequency in MHz

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	**EPC21601**	**V_{DD} = 7 V, T_J = 125°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; operating frequency = 30 MHz	0	16	1049

Table 20: HTOL test result of EPC21601 with V_{DD} = 7 V and T_J = 125°C

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	**EPC21601**	**V_{DD} = 8.5 V, T_J = 125°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; = 30 MHz	3	16	1049
HTOL	**EPC21601**	**V_{DD} = 9.5 V, T_J = 125°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; = 30 MHz	15	16	305

Table 21: HTOL test result of EPC21601 with V_{DD} = 8.5 V and V_{DD} = 9.5 V, T_J = 25°C

The effect of temperature acceleration was also studied at two different temperatures, 25°C and 125°C, while the V_{DD} was fixed at 8.5 V. The results are summarized in Table 22 where it shows a significant temperature acceleration.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	EPC21601	**V_{DD} = 8.5 V, T_J = 25°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; operating frequency = 30 MHz	3	16	1049
HTOL	EPC21601	**V_{DD} = 8.5 V, T_J = 125°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; operating frequency = 30 MHz	15	16	718

Table 22: HTOL test result of EPC21601 with T_J = 25°C and , T_J = 125°C, V_{DD} = 8.5 V

Failure analysis determined that they were all soft parameter failures due to the quiescent current exceeding the 20 mA maximum datasheet limit [23]. Under closer examination, the quiescent current only exceeded datasheet limits when the failures were tested under the specified lidar operation, where the V_D = 20 V, V_{IN} = 3.3 V, and V_{DD} = 5 V during OFF state. A simple normal DC characterization of only the V_{DD} pin did not reveal the failure mode.

When the quiescent current soft failures were subjected to lidar operation with a V_D of 15 V, the integrity of their pulses was uncompromised. Figure 20 shows the waveforms of the input signal (blue) of V_{IN} (the logic input to EC21601) and the corresponding output signals from V_D of the quiescent current failures (green and yellow), where no pulse distortion or missing pulses were observed. This suggests even when the device was damaged by extremely high V_{DD} stress, it still was functional, and the performance of the laser pulses was not adversely impacted.

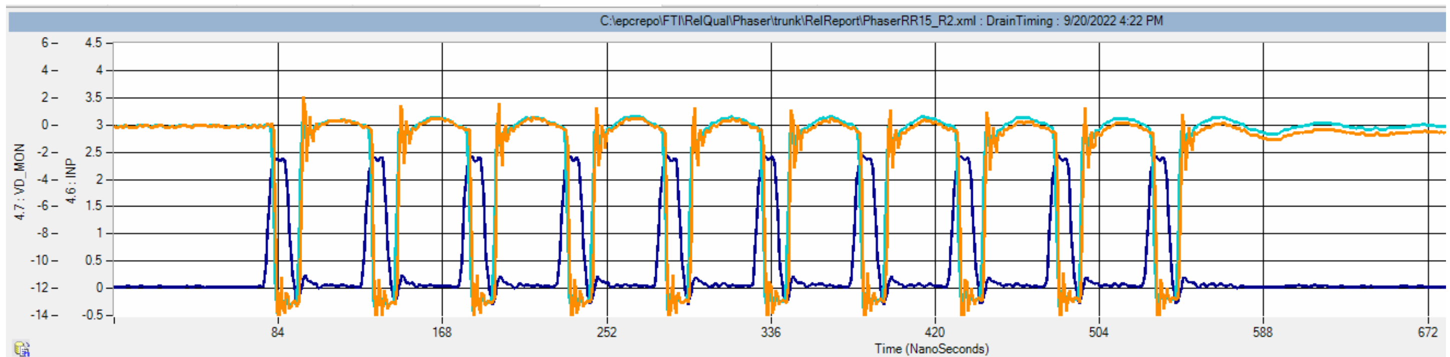


Figure 20: The input (blue) waveform and the corresponding output waveforms of the quiescent current failures (green and yellow)

Since all failures at different voltages and temperatures showed similar "soft" electrical failures, physical failure analysis was conducted to determine the underlying root cause. Gate rupture primarily of the LV GaN FETs in the driver circuit was found to be the single failure mechanism for all failures regardless of stress voltages and temperatures. This result is expected based on the circuit analysis because the V_{DD} voltage is essentially applied to the gates of the LV and HV GaN FETs when the pulses are generated.

Figure 21 shows time-to-failure data of two different V_{DD} voltages at room temperature. The data was analyzed using a two-parameter Weibull distribution for each voltage leg using maximum likelihood estimation (MLE). The fits are indicated by solid lines in the graphs. The Weibull shape (or slope) parameter was constrained to be the same for all voltage legs because a single failure mode was found through failure analysis.

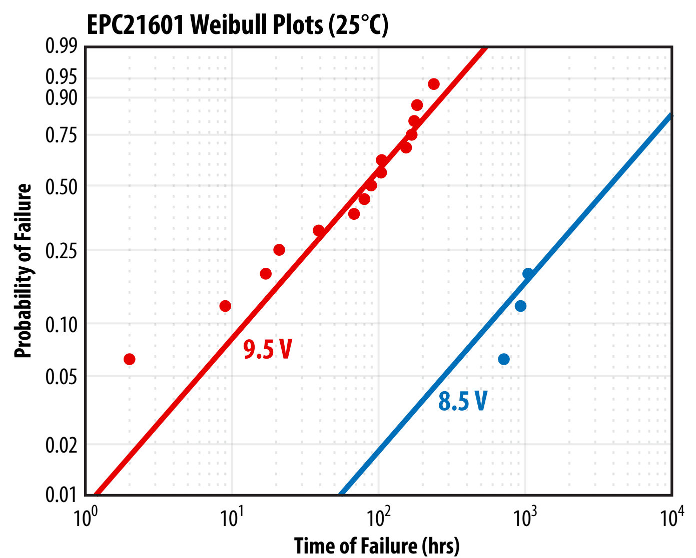


Figure 21: Weibull plots showing the failures of EPC21601 at 8.5 V (blue) and 9.5 V (red) V_{DD}, respectively and T_J = 25°C

The calculated mean-time-to-failure (MTTF) of the 9.5 V V_{DD} leg is approximately 117 hours, which equals to 4.2 X 10^5 seconds. In Figures 1 and 2 of the Phase 14 Reliability Report [2], the MTTF of the 9.5 V V_{GS} DC test of EPC2212 at 25°C is approximately 150 seconds, which is 7.5 x 10^5 seconds when scaling with the 0.02% burst duty cycle that was used in the HTOL test. EPC21601 and EPC2212 share the same gate construction and use identical gate fabrication processes. This converted result from a static DC V_{GS} testing on EPC2212 is close to the measured MTTF of EPC21601 that was essentially subjected to a dynamic accelerated gate testing for hundreds of GaN FETs.

It is understandable that the two MTTF values do not match exactly due to the difference in testing setup and implementation. For instance, the gates of all the LV FETs were stressed through the same V_{DD} pin concurrently during an extremely short pulse, where some slight ringing on the gates might be expected. This could explain the slightly worse MTTF for EPC21601 as compared to the DC accelerated gate testing result for EPC2212.

The commensurate MTTF results between EPC21601 and EPC2212 also corroborate the validity of the physics-based model EPC developed for the gate reliability in the Phase 14 Reliability Report [2]. The same lifetime equation (Equation 1) with respect to the voltage acceleration is plotted against the measured data for V_{DD} at two different biases.

Figure 22 shows the lifetime projection against the measured acceleration data for EPC21601 at 25°C. The fit projected greater than 25 years of lifetime with less than 1 ppm failure rate at the 5.5 V maximum V_{DD} voltage rating at 25°C. This result also agrees well with the extrapolated lifetime for gate at 5.5 V under static DC gate bias.

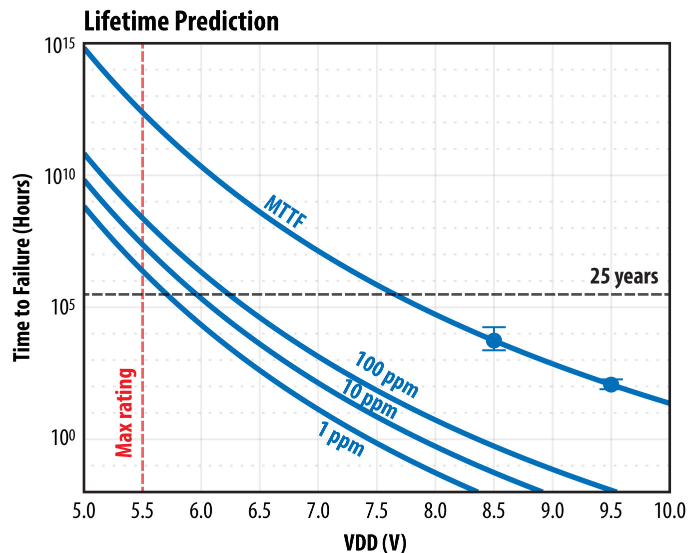


Figure 22: EPC21601 MTTF data at two different voltages with error bars are plotted against V_{DD} at 25 °C. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

Figure 23 shows time-to-failure data at two different temperatures (25°C and 125°C) while the V_{DD} was fixed at 8.5 V. The data was also analyzed using a two-parameter Weibull distribution for each temperature leg using maximum likelihood estimation (MLE). The Weibull shape (or slope) parameter was constrained to be the same for both temperature legs because a single failure mode was identified through failure analysis. The time-to-fail of each device was recorded by conducting a complete ATE post screening after the parts were removed from the oven (125°C leg) and the motherboards. Multiple "soft" quiescent current failures were found at the same first read point at 72 hours in the 125°C leg, where a cluster of vertical failure data points were shown on the Weibull plot. The last failure was found at 718 hours for the 125°C leg, whereas only a total of three soft failures were measured after more than 1000 hours of testing in the 25°C leg, as shown in Table 22.

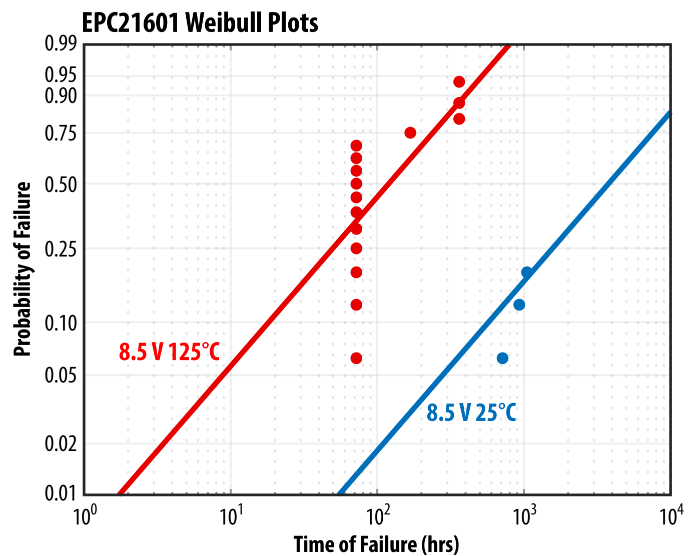


Figure 23: Weibull plots showing the failures of EPC21601 at 25°C (blue) and 125°C (red) junction temperature, V_{DD} = 8.5 V

Figure 24 shows the Arrhenius plot for the MTTF data at 25°C and 125°C with V_{DD} = 8.5 V, where an activation energy of 0.35 eV was calculated by using the Arrhenius equation [24–26]. This result is different from what was observed when conducting static HTGB testing for discrete GaN products. Initial failure analysis showed identical gate rupture as the underlying failure mode for all soft quiescent current failures regardless of 25°C or 125°C testing temperature.

Though the failure mechanism responsible for the temperature acceleration warrants further investigation, the laser driver IC under the V_{DD} stressor is proven to be extraordinarily robust.

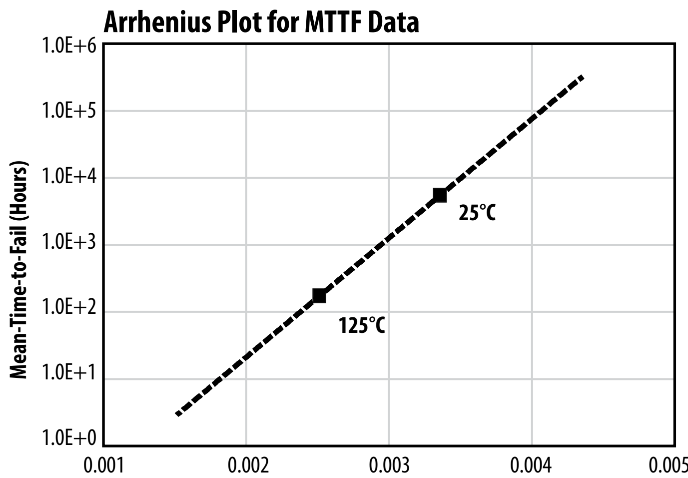


Figure 24: EPC21601 MTTF data at two different temperatures are plotted against T^{-1} (K^{-1}) with V_{DD} at 8.5 V. The solid line corresponds to the Arrhenius equation, where an activation energy of 0.35 eV was found.

7.2.5 V_D, Laser Drive Voltage

By examining the circuits that connect the V_D pin in detail, the accelerated V_D HTOL can cause two potential failure modes in EPC21601.

1. V_D primarily goes to the drain terminal of the HV GaN FET. Due to the nature of lidar operation, the HV output FET is under reverse drain bias most of the time. When the laser pulses are generated, the HV FET turns on and conducts current. Accelerated V_D HTOL test in essence is conducting a dynamic HTRB test with a high duty cycle. Therefore, the intrinsic failure modes due to accelerated drain bias test for a discrete GaN transistor apply.
2. Besides connecting to the drain node of the HV FET, the V_D pin associates with only one of the laser driver circuits, but it determines the number of pulses generated by the device. If that path was compromised by the accelerated V_D stress, it could lead to missing pulses, which is another crucial failure mode for lidar application.

The HTOL qualification test was conducted at 30 V V_D, the maximum recommended voltage specified by the datasheet [23]. A matrix of accelerated V_D HTOL tests were conducted and summarized in Table 23. 60 V V_D was selected because it is two times of the maximum recommended voltage rating, which is an extremely accelerated condition. However, this voltage is not too high to cause some other known intrinsic failure modes for the HV output FET. 60 V is an aggressive test-to-fail condition against the driver design. Table 23 shows that no failures were found after more than 1000 hours of testing. All parts passed the post ATE screening against the product datasheet.

When parts pass all the datasheet limits it suggests there is no catastrophic failure mode within these limits. It is still possible the parts could suffer from distorted or missing pulses as mentioned in the second potential failure mode described above. To further validate the pulse waveforms of the ATE passing devices, the parts from the V_D = 60 V and TJ = 125°C leg were mounted back onto the test setup at 60 V and 125°C, the input and output pulse waveforms were captured and shown in Figure 25.

Figure 25 shows that no degradation in pulse waveforms was observed after more than 1000 hours of HTOL testing. It is also important to note that the HV output transistor experienced more than 25 V overshoot at the end of each pulse during HTOL resulting from the short pulses. It suggests that the device saw repetitive > 85 V transient overvoltage stress (> two times the absolute maximum rating = 40 V) on V_D in addition to the 60 V nominal stress that is another two times the maximum recommended bias. This also demonstrates good robustness of the device under V_D stress.

At this point, the most rigorous testing corner is covered by the testing matrix at the 60 V V_D leg at 125°C. Further increasing the drain bias might introduce a different intrinsic failure mechanism for the HV GaN transistor that is not applicable to the lidar application or the reliability robustness of laser drive IC. In short, no failure mode was found in the laser supply voltage (V_D) testing leg.

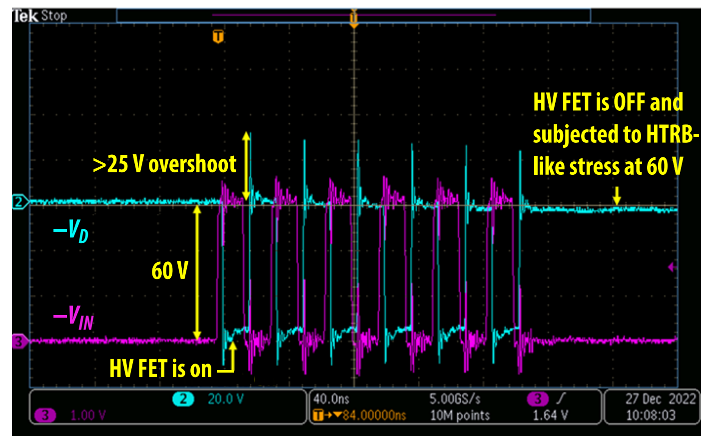


Figure 25: Output waveforms (blue) of a representative passing part after it was subjected to 1005 hours of HTOL testing at 60 V V_D and 125°C. The purple waveform is the corresponding input signal from V_{IN}. Please note that a 25 V of overshoot was seen at the end of each pulse during HTOL testing.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	**EPC21601**	**V_{DD} = 60 V, T_J = 25°C**, V_{D_DC} = 5.5 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; operating frequency = 30 MHz	0	16	1005
HTOL	**EPC21601**	**V_{DD} = 60 V, T_J = 125°C**, V_{D_DC} = 5.5 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; operating frequency = 30 MHz	0	16	1005

Table 23: HTOL test result of EPC21601 with V_D = 60 V, T_J = 25°C and T_J = 125°C, respectively

7.2.6 Operating Frequency

Small sample size preliminary device characterization found that the pulse waveforms could be distorted when testing at extremely high operating frequency. It is therefore useful to study at what frequency or duration of the HTOL testing the pulse waveform starts showing significant distortion or missing pulses.

A testing matrix at two high operating frequencies were carried out as show in Table 24. 48 MHz and 96 MHz are 160% and 320% more than the 30 MHz maximum recommended operating frequency used in qualification. No failure occurred after more than 1400 hours of testing. All parts passed post ATE screening where all parameters were within datasheet limits.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTOL	**EPC21601**	**Operating frequency = 48 MHz** V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; V_{D_DC} = 30 V, T_J = 25°C, V_{D_DC} = 5.5 V, R_{LOAD} = 2 Ω	0	16	1413
HTOL	**EPC21601**	**Operating frequency = 96 MHz** V_{IN} = 3.3V_{P-P}, burst frequency = 1 kHz; V_{D_DC} = 30 V, T_J = 25°C, V_{D_DC} = 5.5 V, R_{LOAD} = 2 Ω	0	16	1413

Table 24: HTOL test result of EPC21601 with operating frequency of 48 MHz and 96 MHz with V_D = 30 V and T_J = 25°C

Figure 26 shows representative input (purple) and output (blue) waveforms of a passing device post 1413 hours of 48 MHz HTOL testing. No waveform distortion or missing pulses were found. Figure 27 shows another set of representative input (purple) and output (blue) waveforms of a passing device post 1413 hours of 96 MHz HTOL testing. No waveform distortion or missing pulses were found.

So far, no failure mode has been identified at nearly 100 MHz HTOL testing for an extended period, which further demonstrates the robustness of the laser driver IC products.

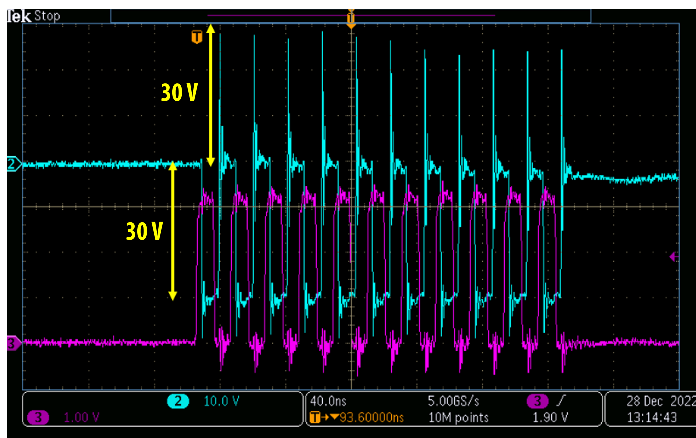


*Figure 26: Representative input (purple) and output (blue) waveforms of a passing device after 1413 hours of HTOL testing at **48 MHz** operating frequency. Please note that a 30 V of overshoot was seen at the end of each pulse during HTOL testing.*

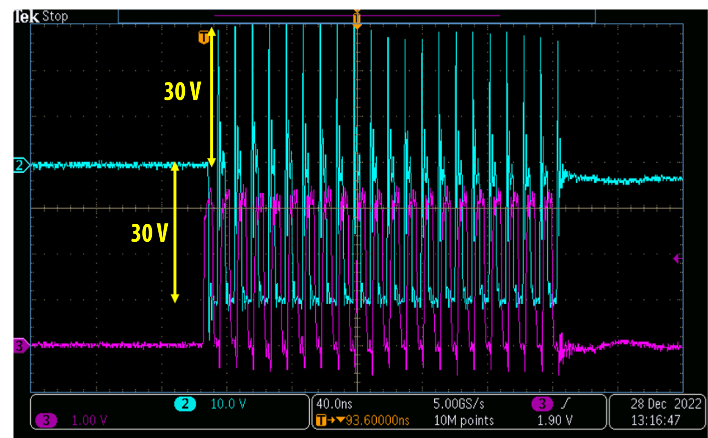


*Figure 27: Representative input (purple) and output (blue) waveforms of a passing device after 1413 hours of HTOL testing at **96 MHz** operating frequency. Please note that a 30 V of overshoot was seen at the end of each pulse during HTOL testing.*

SECTION 8: USING TEST-TO-FAIL METHODOLOGY TO ACCURATELY PREDICT HOW eGaN DEVICES CAN LAST MORE THAN 25 YEARS IN SOLAR APPLICATIONS

Modern solar panels are demanding increasingly higher power density and longer operating lifetimes. Solar applications including power optimizers and panels with built-in microinverter are becoming the prevailing trend for an increasing number of solar customers, where low voltage GaN power devices (V_{DSMax} < 200 V) are extensively used. Integration of high-power density into the same form factor and longer lifespan are becoming key challenges for market adoption. GaN power transistors and integrated circuits offer solutions that can make the solar power systems smaller, cooler, more efficient, and more reliable.

Greater than 25 years of reliable operation is a typical requirement for solar installations. The test-to-fail methodology stresses devices under extremely accelerated test conditions. The goal is to fail the devices quickly and conduct failure analysis to determine the underlying failure modes. Using this approach enables an understanding of the intrinsic failure mechanisms and the development of physics-based mathematical models that accurately predict the lifetime under all mission profiles. In references [2,19–22], various lifetime predictions involving gate, drain, and thermo-mechanical stress have been quantified. In this report, we use these physical insights and apply them to the unique demands of solar applications.

8.1 Gate Stress

The representative discrete GaN device (EPC2212) used in this study showed excellent long term gate reliability, where the test-to-fail approach at accelerated gate bias conditions was applied. Failure analysis was conducted on multiple failures from the study, and a consistent failure mode was found between the gate metal and the metal field plate. The silicon nitride dielectric sandwiched between is responsible for the gate failures in this study, as highlighted in Figure 3 from the Phase 14 Reliability Report [2].

Based on the intrinsic failure mechanism found in the failure analysis, A first-principles mathematical model was developed to explain all observations. This model can be used to predict the lifetime under different gate biases, temperatures, and duty cycles. The physics-based lifetime equation is plotted against the measured accelerated data for EPC2212 in Figure 28. Figure 28 shows that EPC2212 has less than 1 ppm failure rate projected over more than 35 years of lifetime under continuous DC gate bias at the maximum rated gate voltage (V_{GS} = 6 V).

When keeping the gate bias below the maximum rated voltage the data shows that eGaN devices should have an extremely low failure rate for more than 25 years of lifetime. This projected result is also consistent with EPC's field experience for gate failures.

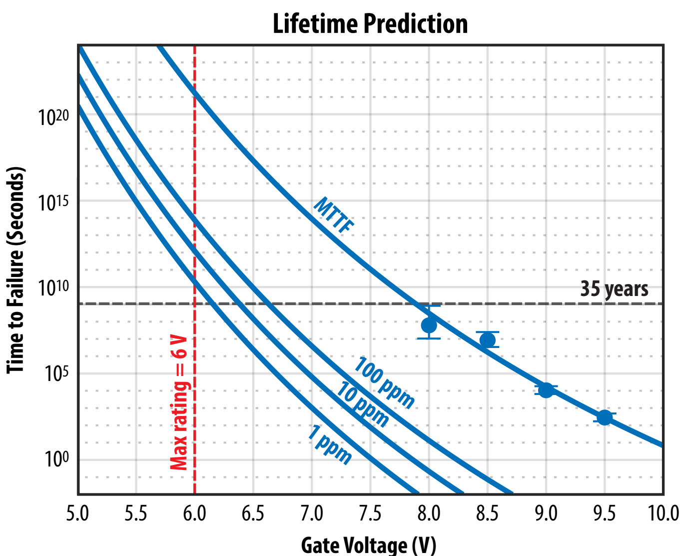


Figure 28: EPC2212 time to failure vs. V_{GS} at 25°C MTTF (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model described in [6].

8.2 Drain Stress

The low $R_{DS(on)}$ and small die size of GaN devices significantly increases the efficiency and reduces the power losses of a solar panel. One common concern for GaN is dynamic on-resistance. This is a condition whereby the on-resistance of a transistor increases when the device is exposed to high drain-source voltage (V_{DS}). The dominant intrinsic failure mechanism responsible for the rise in the on-resistance is the trapping of electrons in trap-states near the channel [5]. As the trapped charges accumulate, it depletes electrons from the two-dimensional electron gas (2DEG) in the ON state, resulting in an increase in $R_{DS(on)}$.

By understanding hot electrons trapping mechanism a resistive hard switching topology circuit was developed and implemented to accelerate this failure mechanism by providing more hot electrons at maximum rated V_{DS} [2,6,21,22] and beyond. Using the characterization test results from this development, a first-principles model was developed to describe the dynamic $R_{DS(on)}$ effects in eGaN FETs under all bias and temperature stress conditions.

Flyback is one of the most used topologies for the microinverters in solar application. When selecting transistors for the primary side, the drain voltage experienced is primarily comprised of three sources, (1) the bus voltage, (2) the flyback voltage, and (3) the spark noise due to the inductance from the design. The typical bus voltage for a microinverter is 60 V in a solar application. The flyback voltage is determined by the product of the system's output voltage and the turn ratio of the transformer, which is usually less than the bus voltage. By adding some margins for the spark noise and derating, 170 V maximum V_{DS} rating is frequently desired by the solar customers using in such applications.

EPC2059 is a 170 V maximum V_{DS} rated product that meets the general requirements for the microinverter in solar applications. Figure 29 shows an EPC2059 device that was operated under continuous hard switching at 136 V (80% of the max rated drain bias of 170 V) while the case temperature was modulated at 80°C, where 80°C is considered a nominal operation temperature for solar application. As shown in Figure 29, the measured data and the corresponding model predict the $R_{DS(on)}$ increase due to continuous hard switching in 35 years is expected to be approximately 10%. The extrapolation is based on the log(time) growth characteristic as described in detail in the prior publications [2,6,21, 22].

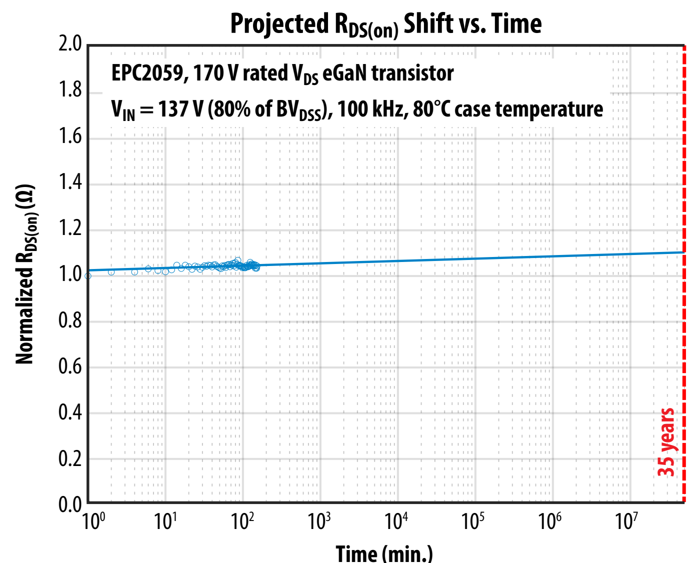


Figure 29: Projected $R_{DS(on)}$ shift of EPC2059, a 170 V rated device in 35 years of continuous hard-switching operation is expected to be approximately 10%.

Another popular option for solar is to use a DC-DC converter in the primary stage (typically a full bridge) of a microinverter. This topology is frequently used in a power optimizer, which has been increasingly adopted by solar providers due to its superior efficiency. GaN devices such as 100 V-rated EPC2218, EPC2053, and EPC2302, among others, are a good fit for this application.

Figure 30 shows that multiple EPC2218 eGaN transistors were tested for over 1000 hours under continuous resistive hard-switching operation at a bias of 100 V, the max rated voltage at 25°C ambient temperature.

Two conclusions are:

1. The projected $R_{DS(on)}$ increase of EPC2218 due to continuous hard switching over 35 years is expected to be approximately 10%.
2. The 1150-hour tests agree with the short duration tests (5 hours) within 10% on the projected $R_{DS(on)}$ after 35 years. The variation of the lifetime projection is resulted from the small (and random) temperature fluctuation in the ambience. This result gives credence to the idea that short-term data can be used for accurately predicting the long-term lifetime of the $R_{DS(on)}$ behavior.

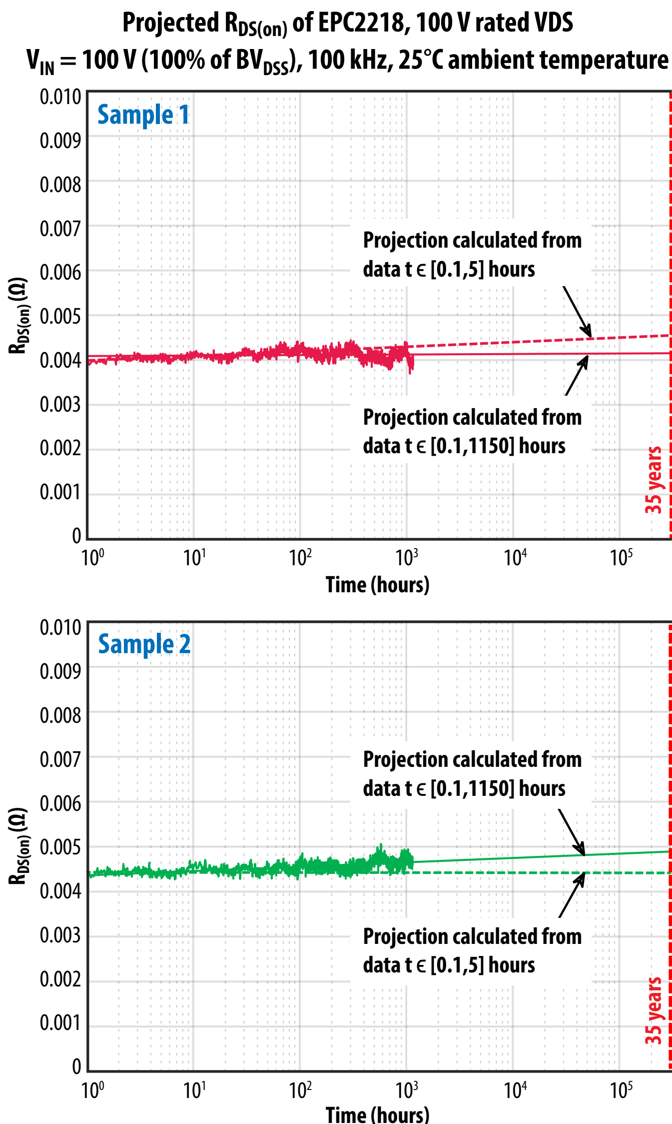


Figure 30: Long-term dynamic $R_{DS(on)}$ for two samples of EPC2218 eGaN FETs under continuous resistive hard-switching operation for over 1000 hours at ambient temperature and a bias of 100 V. Note that the short-term fit has a similar projection to the long-term fit, with small random differences of ±10% on the 35-year projection.

Therefore, eGaN devices demonstrate good robustness in dynamic on-resistance with more than 25 years of lifetime and beyond.

8.3 Thermo-Mechanical Stress

Thermo-mechanical reliability is another critical area of particular interest in solar applications. Solar panels are placed outside and experience significant ambient temperature change during each day. Therefore, devices mounted on the PCBs in the solar panels must be capable of surviving 25 years of continuous ambient temperature change. A similar test-to-fail approach was used to study the board level thermo-mechanical reliability of EPC2218A, the automotive grade of EPC2218. As described above, EPC2218A or equivalent commercial grade 100 V rated devices are ideal candidates for use in power optimizers for solar applications.

Three different combinations of temperature cycling stress conditions, with or without the underfill material were studied. Two temperature cycling ranges were tested: temperature cycle 1 (TC1): –40°C to 125°C and temperature cycle 2 (TC2): –40°C to 105°C. Under the temperature range of –40°C to 125°C (TC1), two cases with and without underfill material were compared. The underfill material selected was from HENKELS LOCTITE (part number: ECCOBOND-UF 1173) that showed good performance in previous studies [5]. The detailed selection guideline for searching proper underfill materials was discussed in [6]. For all cases, the parts were mounted on DUT cards or coupons consisting of a 2-layer, 1.6-mm thick, FR4 board using SAC305 solder paste, and water-soluble flux. All underfilled devices were subjected to a plasma clean process prior to the underfill application.

Industry standard (JESD22-A108F [27]) and other customers' specifications were followed for this study. A group of 88 devices of EPC2218A were tested for each leg, and all three test legs used similar ramp rate and dwell time at the two temperature extremes. After every temperature cycling interval, electrical screening was performed, where exceeding datasheet limits were used to determine failures. The main electrical failure characteristic is an increase in $R_{DS(on)}$, but the devices are still functional as normal transistors. Physical cross-sectioning and SEM inspection were followed to further examine the electrical test failures. Solder joint cracking was found to be the single failure mode throughout all failures analyzed.

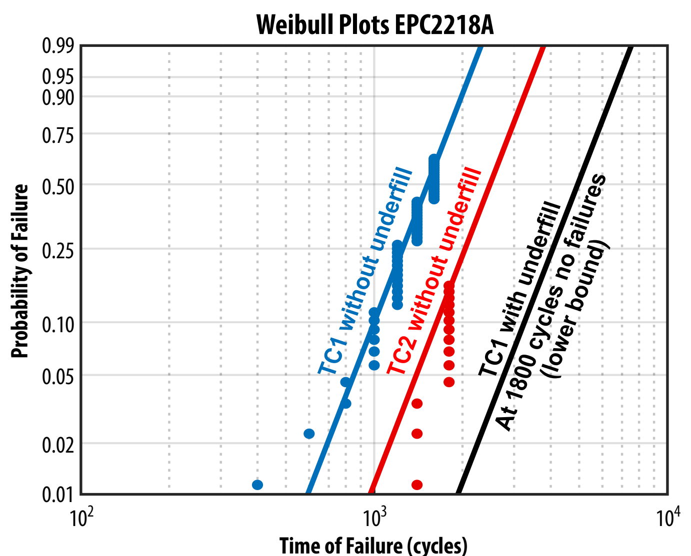


Figure 31: Weibull plots of temperature cycling results for EPC2218A

Figure 31 shows Weibull failure distribution of the temperature cycling results. The failure distribution was analyzed using a two-parameter Weibull distribution for each temperature cycling leg using maximum likelihood estimation (MLE) [28]. The fits are indicated by solid lines in the graph.

TC1 (–40°C to 125°C) without underfill material reached more than 50% cumulative failure rate at 1600 cycles, where physical failure analysis found that solder joint cracking was the single failure mode for all failures at various read points.

TC2 (–40°C to 105°C) without underfill material leg showed approximately 60% failure rate at the end of 2400 cycles as shown in Figure 31. A strong acceleration was found from TC2 to TC1 test conditions, where devices from both cases did not use underfill material.

Two primary failure mechanisms could be responsible for the significant acceleration. First, the difference in ΔT of two testing conditions leads to the acceleration of the solder fatigue failure mechanism, which is well described by the Coffin-Manson relation and is widely adopted by JEDEC [29] and AEC [30] standards. However, this failure mechanism alone is insufficient to explain the acceleration observed. A second mechanism, creep solder joint failure mechanism, is introduced here. Creep is believed to be the main effect during the dwell period at the hot temperature extreme [31–35]. This creep mechanism is governed by an activation energy that will be discussed in the following lifetime model development.

After 1800 cycles of TC1 (–40°C to 125°C) with HENKEL underfill, no outlier devices were found in the absolute $R_{DS(on)}$ value nor in the $R_{DS(on)}$ shift post electrical testing. All parameters examined showed very tight distributions throughout all temperature cycling intervals. Physical cross-sectioning was conducted on a randomly selected part from the 1800 cycles passing devices, where no solder joint cracking was observed. This shows that applying proper underfill material can significantly improve the thermo-mechanical capability of the chip-scale package devices. Therefore, the Weibull fit line for the TC1 with the underfill leg is merely the lower bound confidence level based on the current test results. The test is continuing, and the plot will be updated when failures are identified.

By investigating and understanding the main failure mechanisms involved in board level temperature cycling, a more general lifetime model was developed by using Norris-Landzberg model [31].

$$N = A \cdot f^{-\alpha} \cdot \Delta T^{-\beta} \cdot \exp\left(\frac{E_a}{kT_{Max}}\right) \quad \text{Eq. 6}$$

Where N is the number of cycles to fail, f is the cycling frequency and α is the cycling frequency exponent, this frequency term is to describe the frequency of usage. In this study, the cycling frequency was determined by counting the total number of cycling per day and the cycling frequency exponent α is widely used –1/3 [32–36]. ΔT is the range of temperature change in one cycle and β is the temperature range exponent. This term is the well-known Coffin-Manson relation mentioned above [29–31] used to determine the effect of the ΔT. The temperature range exponent is typically around two. Since SAC305 solder is used in this study, the exponent β is 2.3 for the lifetime modeling [28–34]. The last variable is an Arrhenius term that focuses on the creep failure mechanism at the maximum temperature, T_{Max} in each cycle, where E_a is the activation energy, k is the Boltzmann constant, and T_{Max} is the maximum temperature of the high-temperature dwell stage in Kelvin units (°K).

Finding the activation energy is critical and the last step towards developing the lifetime model. By comparing the mean-time-to-fail (MTTF) between TC1 and TC2 without underfill material as listed in Table 25, the acceleration factor was determined. Based on the acceleration factor, the activation energy (E_a) at T_{Max} was calculated to be 0.2 eV.

The predicted lifetime curves using Norris-Landzberg model are plotted in Figure 32 assuming the T_{Max} is 125°C, which is possibly the worst-case scenario for creep failure mechanism. The horizontal, black dashed line at 9,125 cycles represents a duration of 25 years of continuous operation assuming one thermal cycle per day. Figure 32 shows that after 25 years of continuous operation under a constant temperature swing of 60°C from hot to cold or vice versa, only 0.1% of EPC2218A devices with underfill material would fail the datasheet limit due to increase in $R_{DS(on)}$ value. At 1% of failure rate, 99% of the devices should be capable of surviving 25 years of continuous operation when subjected to a constant ΔT of 76°C. Even without underfill material, 99% of the parts should survive a fixed ΔT of approximately 50°C over 25 years of continuous operation.

TC Condition	T_{min} (°C)	T_{max} (°C)	ΔT (°C)	Frequency (cycles per day)	Slope Parameter	Characteristic Weibull Life	MTTF (cycles)
TC1 without underfill	-40	125	165	36	4.5	1649	1505
TC1 without underfill	-40	105	145	48	4.5	2663	2430
TC1 with underfill	-40	125	165	36	4.5	5410	4937 (no failures at 1800 cycles, a lower bound confidence level)

Table 25: Temperature cycling profile and key parameters determined by Weibull plots

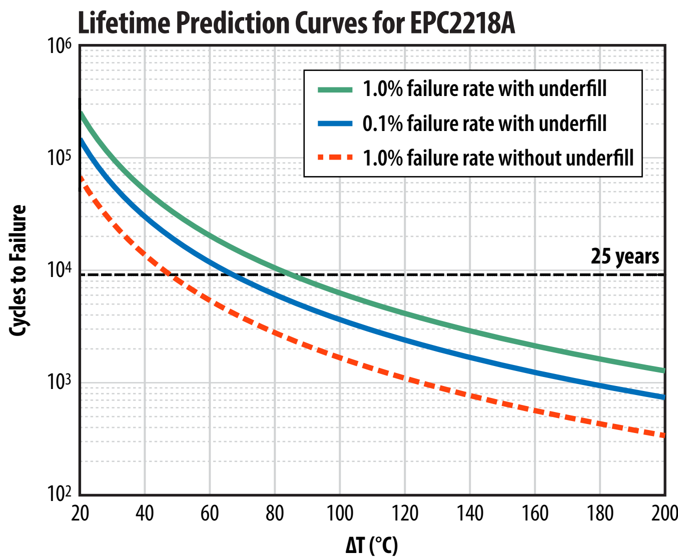


Figure 32: Lifetime prediction curves for EPC2218A with respect to ΔT using the Norris-Landzberg model

In real-world applications, solar panels experience varying ambient temperatures, and the amount of temperature changes varies significantly depending on the season and location. As a result, a more general lifetime model for thermo-mechanical stress is warranted to account for various mission profiles over the 25 years of lifetime. An empirical mathematical model is developed below to account for different ΔT at different seasons of the year, as shown in Equation 7.

$$\frac{1}{N_{Total}} = \frac{a}{N_{\Delta T_a}} + \frac{b}{N_{\Delta T_b}} + \cdots + \frac{i}{N_{\Delta T_i}} \quad \text{Eq. 7}$$

Where N_{Total} is the total calculated lifetime of number of cycles, $N_{\Delta T_a}$ corresponds to cycles-to-failure for the condition of ΔT_a and a is the fraction of time the device was operational under the condition of ΔT_a, $N_{\Delta T_b}$ corresponds to cycles-to-failure for the condition of ΔT_b and b is the fraction of time the device was operational under ΔT_b, and $N_{\Delta Ti}$ corresponds to cycles-to-failure for the condition of ΔT_i and i is the fraction of time the device was operational under ΔT_i.

There are three main factors that predominantly determine the lifetime of the solder joints when developing this model. Each one is included in the model.

1. The duration of each mission profile needs to be separated. This effect is accounted by the fractional coefficient in numerator in each term in Equation 7, such as *a*, *b*, …, and *i*.
2. The temperature change (ΔT) in each mission profile; this term is addressed by the Norris-Landzberg model in Equation 6 and plotted in Figure 32. The solder joints experience the most stress during the period when the devices are subjected to the largest ΔT, which translates to the shortest cycles-to-failure. The overall lifetime of the device essentially shall be dominated by the most stressful period. This effect is addressed by putting the cycles-to-failure term ($N_{\Delta T}$) in the denominator and then sum them up collectively.
3. The hottest temperature extreme of each cycle, or the baseline temperature; for instance, the solder joints may experience different stress levels given an identical ΔT in the winter or in the summer. This effect is included in the Arrhenius term in Equation 6, which eventually goes to the cycles-to-failure term ($N_{\Delta T}$) in the denominators.

Next a real-world example was examined to estimate the lifetime using Equation 7 by applying different mission profiles throughout the lifetime of the devices, where the calculation uses the lifetime plot of 0.1% failure rate for EPC2218A with underfill.

It was assumed that the solar panels are installed in Phoenix, Arizona, where solar is well-suited for the climate that has long sun exposure, but also demands very stringent thermo-mechanical requirements due to the extreme temperature changes over time. Using the year 2023 forecast as an example [37], the average ΔT from January to April is expected to be 14.5°C (1/3 of the time), from May to August ΔT is expected to be 20°C (1/3 of the time), from September to December ΔT is expected to be 14.75°C (1/3 of the time). Device self-heating of 30°C is added in the mission profile. The corresponding cycles-to-failures are tabulated in Table 26. For the 0.1 % failure rate the total lifetime is calculated to be 15,433 cycles. Considering one cycle equivalent to one day the lifetime is estimated to be 42 years for 0.1% failure rate due to temperature cycling stress.

Cycles to 0.1% failure rate with underfill	N_{Total}	$N_{\Delta Ta}$ (ΔT_a = 44.5°C)	$N_{\Delta Tb}$ (ΔT_b = 50°C)	$N_{\Delta Tc}$ (ΔT_c = 44.75°C)
	15,433	17,742	13,570	15,086

Table 26: Number of cycles to 0.1% failure rate with underfill for each mission profile in real-world applications

Based on the discussions above, making use of EPC's 100 V-rated Generation 5 product family with underfill for real-world solar application vastly reduces thermal cycling reliability risk while giving excellent lifetimes that significantly exceed the expected 25 years.

8.4 Cosmic Rays

Because solar panels are installed outside, devices used in solar inverter applications are more likely to be subjected to energetic particles that originate from the cosmic rays from outer space. Terrestrial neutrons are found to be the most lethal particles causing catastrophic failures for power devices, including Si MOSFET and SiC devices [38-40]. Studies have shown that the failure rate found in MOSFET and SiC devices is usually constant in time, but strongly dependent on the voltage and the altitude, and weakly dependent on the temperature [38-40].

Figure 33 shows the testing results of a 100 V-rated GaN devices under neutron radiation bombardment at doses up to 4 x 10^{15} per square cm, where the average parametric value change was found to be minimal. The survival of a fluence of 4 x 10^{15} n-cm^2 significantly exceeded of the reported values for both SiC-based [41] and Si-based [42] power devices.

The primary failure mechanism for devices under neutron bombardment is displacement damage [43] because the high energy neutrons scatter off atoms in the crystal lattice and leave behind lattice defects. Therefore, the results in Figure 33 show that the impact of neutrons on the GaN crystal and the entire device structure is insignificant.

The reason for GaN's superior performance under neutron radiation is that GaN has a much higher displacement threshold energy compared with silicon. The displacement energy of a crystal is proportional to the bond strength of the crystalline elements. The bond energy between gallium and nitrogen is significantly higher than the bond energy between silicon atoms in a silicon power MOSFET as shown in Figure 34 [44].

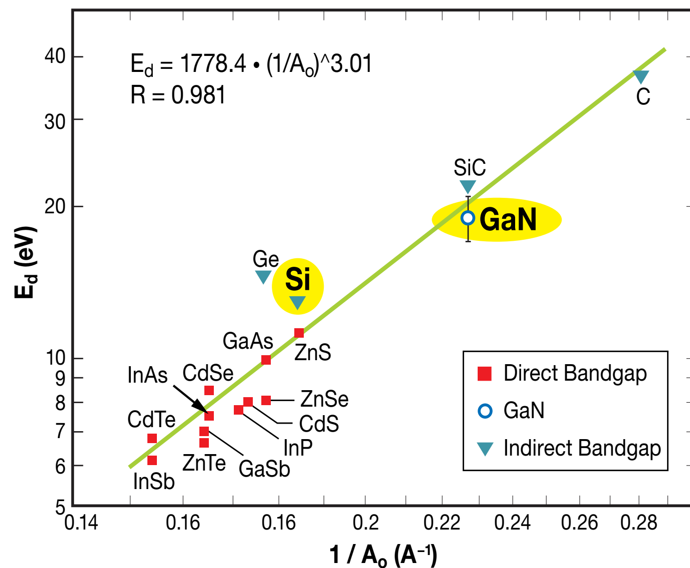


Figure 34: Graph of displacement threshold energy versus the inverse of the lattice constant for different materials taken from [44]

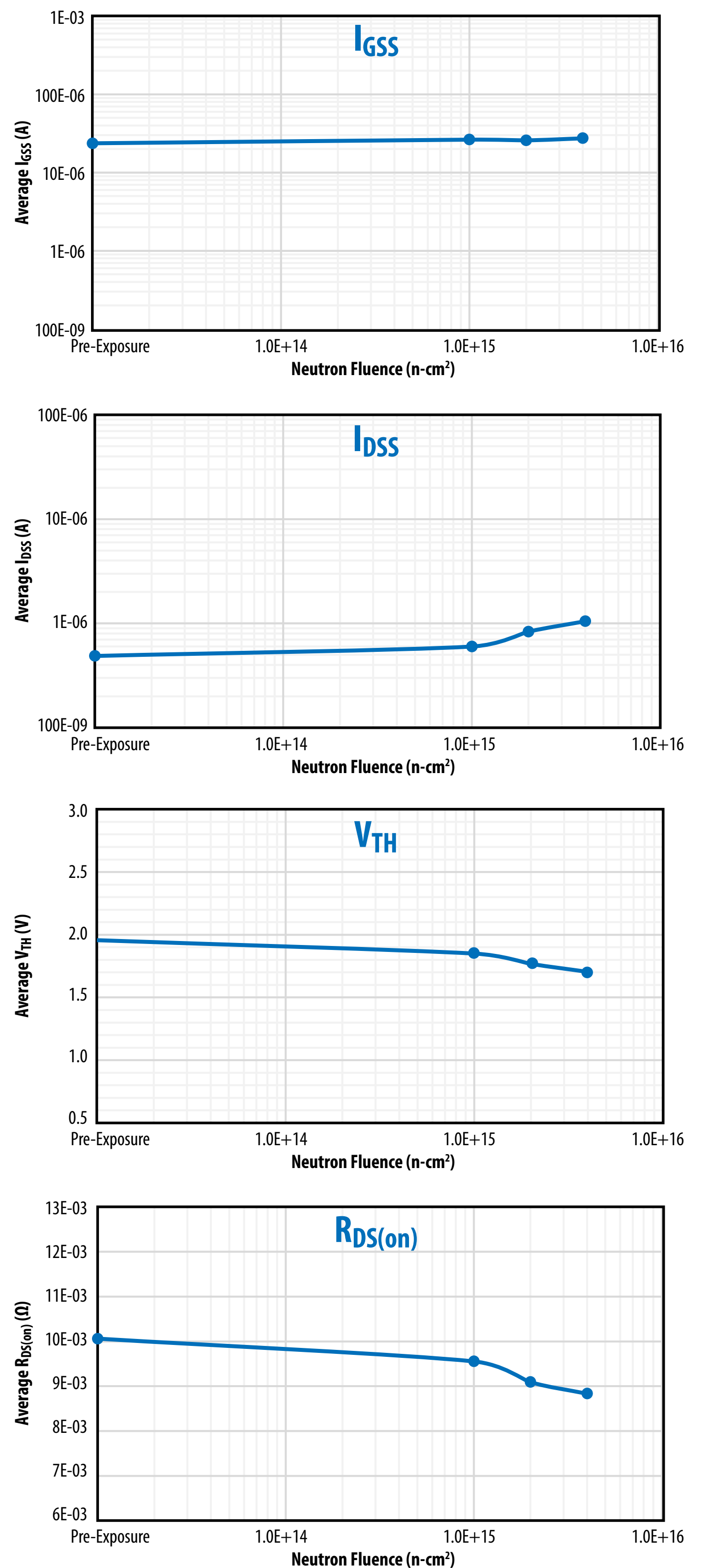


Figure 33: Impact of neutron radiation on 100 V rated eGaN devices (FBG10N30 uses a EPC2001C equivalent rad-hard version of discrete eGaN device) at doses up to 4 x 10^{15} cm^2

SECTION 9: DC-DC CONVERTERS

In this section, the dynamic $R_{DS(on)}$ model from Section 5 is applied to some common DC-DC converter use cases: (i) a synchronous rectifier and (ii) a buck converter, considering both the high-side and low-side FETs. For these calculations, a two-step simulation process was used.

In the first step, realistic SPICE models of the application circuits, including the effects of key parasitic inductances that occur in practical layouts were developed. These parasitics have a first-order effect on ringing and voltage overshoot and can therefore impact dynamic $R_{DS(on)}$ in the FET itself. Parasitic inductances were varied from typical all the way to extreme (representative of very poor PCB layout). The SPICE simulations captured the channel current and drain-source voltage inside the FET with fine time sampling throughout a single switching cycle.

In the second step, these single-cycle, current-voltage loci were imported into the hot electron trapping model (implemented in MATLAB). Using this model, we calculate the charge trapping that occurs in the very first switching cycle were calculated, and at what times (e.g., turn-on or turn-off transitions) the most charging occurs were determined. Furthermore, over trillions of identical switching cycles were integrated to determine the cumulative charge trapping that would occur over 10 years of continuous operation. Because the instantaneous trapping rate depends (non-linearly) on the cumulative trapped charge, the amount of charging per cycle is not constant, but instead rapidly self-quenches over time as the FET switches. Not only does the charging saturate in time, but the regions within a switching waveform that are most detrimental can also change as the device operates; for example, the case of the hard-switch high-side FET in a buck converter (to be discussed in detail later). Initially, charge trapping occurs predominantly during the high-current/moderate-voltage loci at the turn-on transition. However, after long-term operation, this process quenches completely, and all further charging occurs only during the low-current/high-voltage loci of the turn-off transition.

The following conclusions will be supported by these calculations:

For a 48 V–12 V LLC Synchronous rectifier:

- Under these zero-voltage switching (ZVS) conditions, dynamic $R_{DS(on)}$ ($dR_{DS(on)}$) is generally very benign.
- Users can consider using 30 V transistor in lieu of conservative 40 V transistor with a 12 V output and 24 V bus voltage.

For a Low-Side FET in Buck Converter (Soft switching) using latest-generation 100 V GaN devices:

- Benign $dR_{DS(on)}$, even with 50 V overshoot on an 80 V bus voltage for the turn on transition.
- Extreme overshoot to 170 V can lead to appreciable $dR_{DS(on)}$

For a High-Side FET in Buck Converter (Hard switching) using latest-generation 100 V GaN devices

- Under moderate overshoot of 40 V (130 V peak), charge trapping occurs predominantly during the turn-on transition, and long-term $dR_{DS(on)}$ is benign.
- Under extreme overshoot of 90 V (170 V peak), charge trapping is dominated by the high voltage ringing following the turn-off transition, and long-term $dR_{DS(on)}$ could be a concern.

9.1 Current-Dependent Hot Electron Trapping Model

To simulate dynamic-charge trapping within individual switching cycles, two simple generalizations to the basic governing differential equation discussed previously were made. For one, it was assumed that the instantaneous trapping rate is linearly proportional to the channel current (*I*). From a device physics perspective, this reasonable assumption is tantamount to saying the channel electrons act independently (non-interacting), and each has an equal probability of becoming a "lucky" electron with sufficient kinetic energy to surmount the surface barrier and become trapped. The second generalization relates to the integration in time. In previous analysis, it was assumed that the current and voltage were not changing in time. This allowed us a closed-form analytic solution for the surface charge vs. time to be obtained. For the more general cases considered here, both current and voltage to change in time throughout the loci of a switching cycle were allowed. As a result, there is no closed form solution, and must be explicitly integrated in time, leading to the general solution shown in Equation 8 below. This integration must be performed numerically, owing to the complexity of the switching waveforms.

$$Q_S(t)=B'\int_0^t I(t)\, exp\left(-\frac{\beta Q_S}{qF(t)\lambda}\right) dt \qquad \text{Eq. 8}$$

Equation 8 represents a significant development in the theoretical understanding of dynamic $R_{DS(on)}$ in GaN transistors. Researchers have long known that both the current and voltage are the key drivers of hot electron trapping in these devices. However, they have not known how to combine their effects mathematically to compute cumulative trapped charge and dynamic $R_{DS(on)}$. As seen in Equation 8, the effect of current is linear, while the effect of V_{DS} (through the electric field term *F*) is highly non-linear and depends on the trapped charge Q_S that has already accumulated. For this reason, as the FET switches over longer time scales and Q_S rises, it is only the hottest electrons, resulting from highest field *F* and highest V_{DS} loci, that can contribute to further trapping. This effect will become clearer as we analyze practical use-cases in the discussion to follow.

Real-world examples are considered in the next step. In the first example, a 48 V–12 V LLC synchronous rectifier operating at 1 MHz was used to evaluate $R_{DS(on)}$ degradation of the secondary side transistors.

9.2 48 V–12 V LLC Synchronous Rectifier

The SPICE model for this circuit is based on the EPC9149 [45] demonstration circuit. The circuit and model parameters are shown in Figure 35. To create different waveforms with more or less overshoot, the leakage inductances L1, L2, L3, and L4 at the output of each of the transformer terminals were varied together from 50 pH to 150 pH. The higher inductance values generated more ringing and overshoot as can be seen in Figure 35 (right).

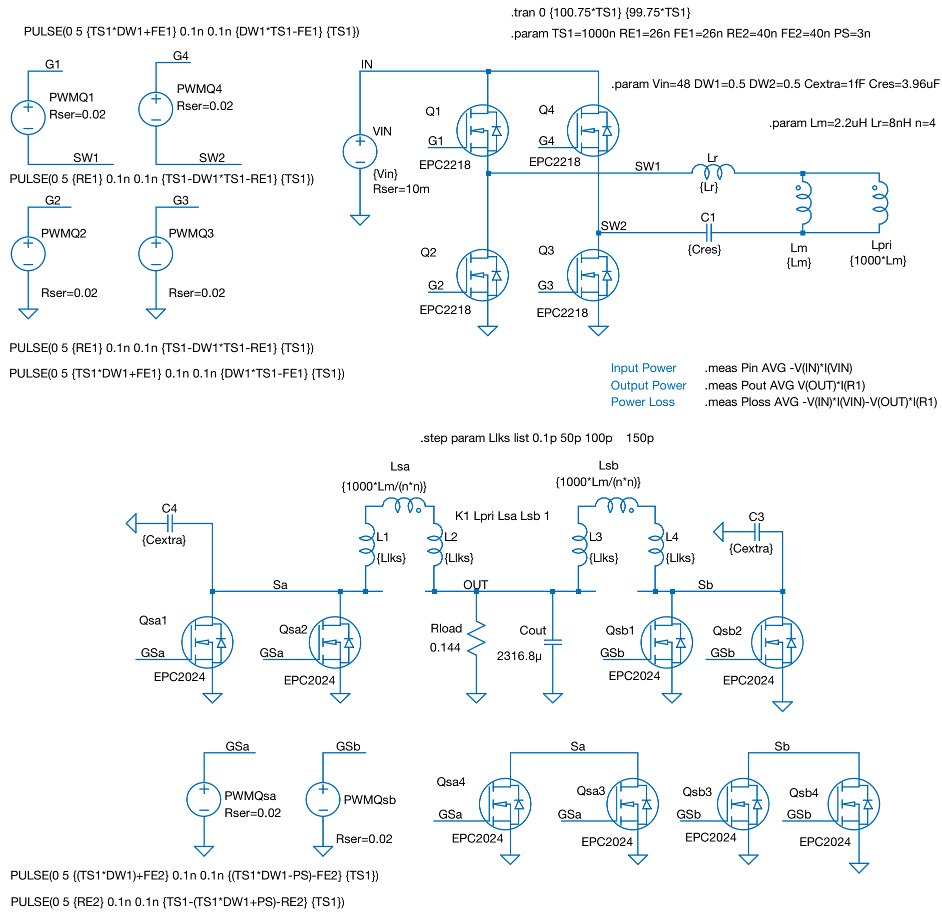


Figure 35: Circuit diagram and SPICE model parameters for a 48 V–12 V LLC synchronous rectifier operating at 1 MHz based on the EPC9149 demo board

Four different cases were studied with the variables being more and less overshoot, and 40 V (case 1 and 2) or 30 V (case 3 and 4) rated GaN devices. In all cases, the eGaN FETs experience a ZVS turn-on and a hard-switched turn-off. The calculations of voltage, current, and $dR_{DS(on)}$ for the entire sequence of switching waveforms from the first cycle to the 10 millionth cycle were made. Figure 36 shows the calculated current and voltage waveforms after 10 million cycles. Throughout each cycle, the amount of trapped charge, Q_S was calculated and summed with all previous cycles.

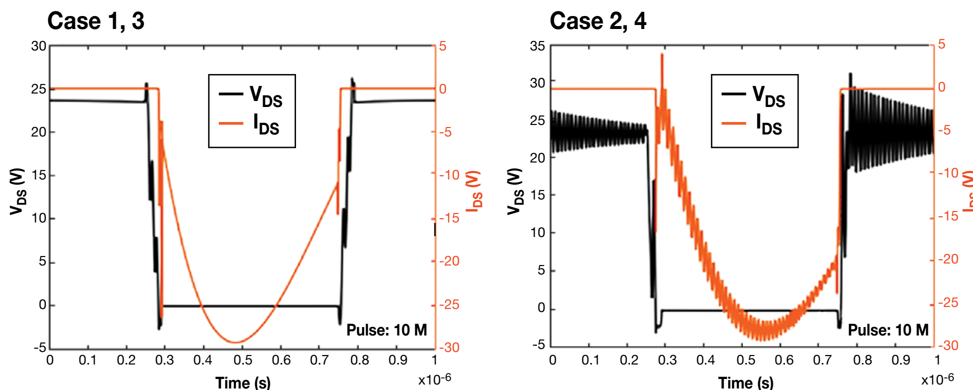


Figure 36: Overshoot was increased in cases 2 and 4 by increasing the inductance values of L1–L4 from 50 pH to 150 pH

9.2.1 40 V GaN Transistors – Cases 1 and 2

In Figure 28 is shown the results of the calculations using 40 V plotted on a log(t) scale ending at 10 years. In both cases there is no measurable accumulation of trapped charge, and therefore no measurable degradation of $R_{DS(on)}$. In the next two cases, a lower $R_{DS(on)}$ 30 V GaN FET was used. Lower voltage parts typically are more efficient than 40 V parts.

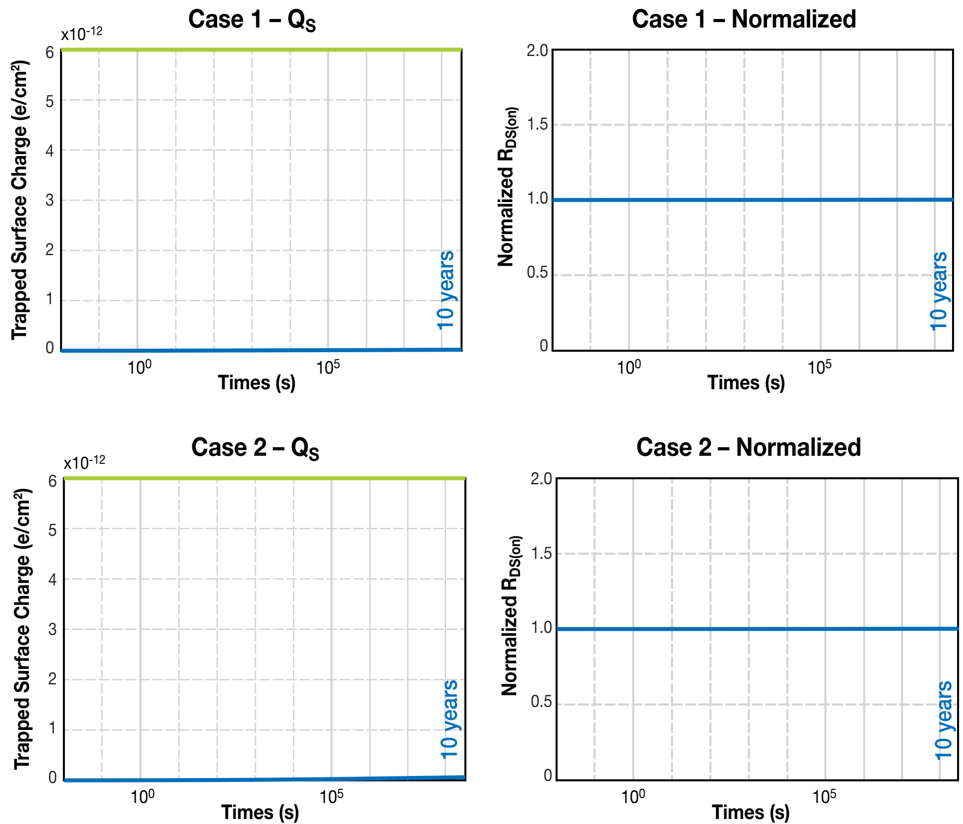


Figure 37: 40 V EPC2024 devices, (upper and lower left) Q_S trapped charge over time, (upper and lower right) normalized $R_{DS(on)}$ over time. Case 1 used L1–L4 = 50 pH, Case 2 used L1–L4 = 150 pH

9.2.2 30 V GaN Transistors – Cases 3 and 4

In Figure 38 is shown the results of the calculations plotted on a log(t) scale ending at 10 years for the same circuits as used in case 1 and 2, except 30 V EPC2024 GaN transistors were used. In the most extreme case there is about 5%, or minimal degradation of $R_{DS(on)}$. The conclusion is that 30 V devices can safely be used in this circuit, even with the more extreme overshoot.

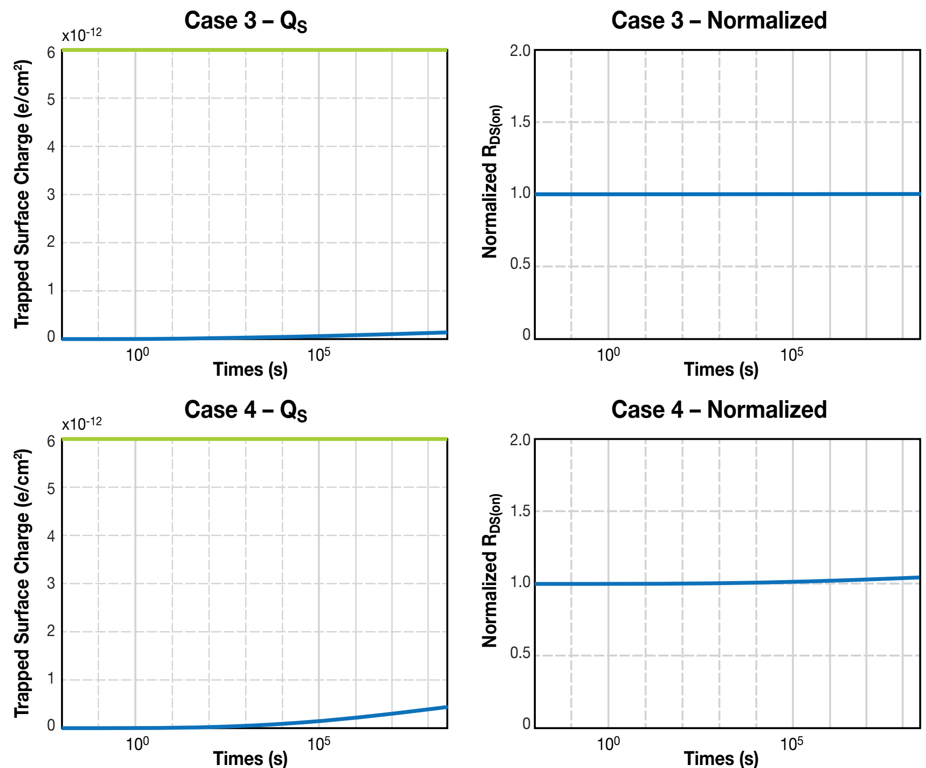


Figure 38: 30 V EPC2023 devices, (upper and lower left) Q_S trapped charge over time, (upper and lower right) normalized $R_{DS(on)}$) over time. Case 3 used L1–L4 = 50 pH, Case 2 used L1–L4 = 150 pH

9.3 48 V–12 V Buck Converter

The next example is for a 48 V–12 V buck converter operating in continuous conduction mode at 500 kHz. The SPICE model circuit schematic is shown in Figure 39. Inductor L5 was varied to modulate the amount of overshoot. The low-side rectifier FET will first be examined, followed by the high-side control FET. Both devices are EPC2045 100 V GaN transistors.

9.3.1 Low-Side GaN Transistor

Figure 40 shows the voltage and current waveforms of the low-side rectifier FET in the converter with different parasitic inductances. In both cases the low-side transistor experiences soft-switching transients, with increasing voltage overshoot at turn-off as the inductance increases. By varying L5 the overshoot above the 80 V bus went from 50 V to over 90 V peak on the low-side transistor as shown in Figure 40. It should be noted that 170 V peak overshoot is much larger than would be experienced in a well-designed system.

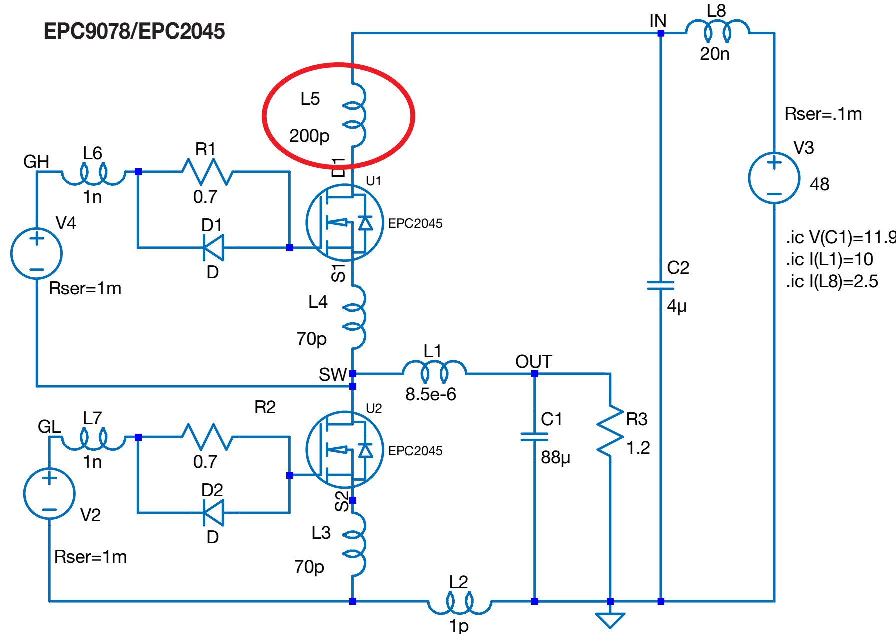


Figure 39: 48 V–12 V buck converter operating at 500 kHz based on EPC9078 demonstration board [46]. To produce different amount of overshoot, L5 was varied from 0.2 nH to 1.2 nH.

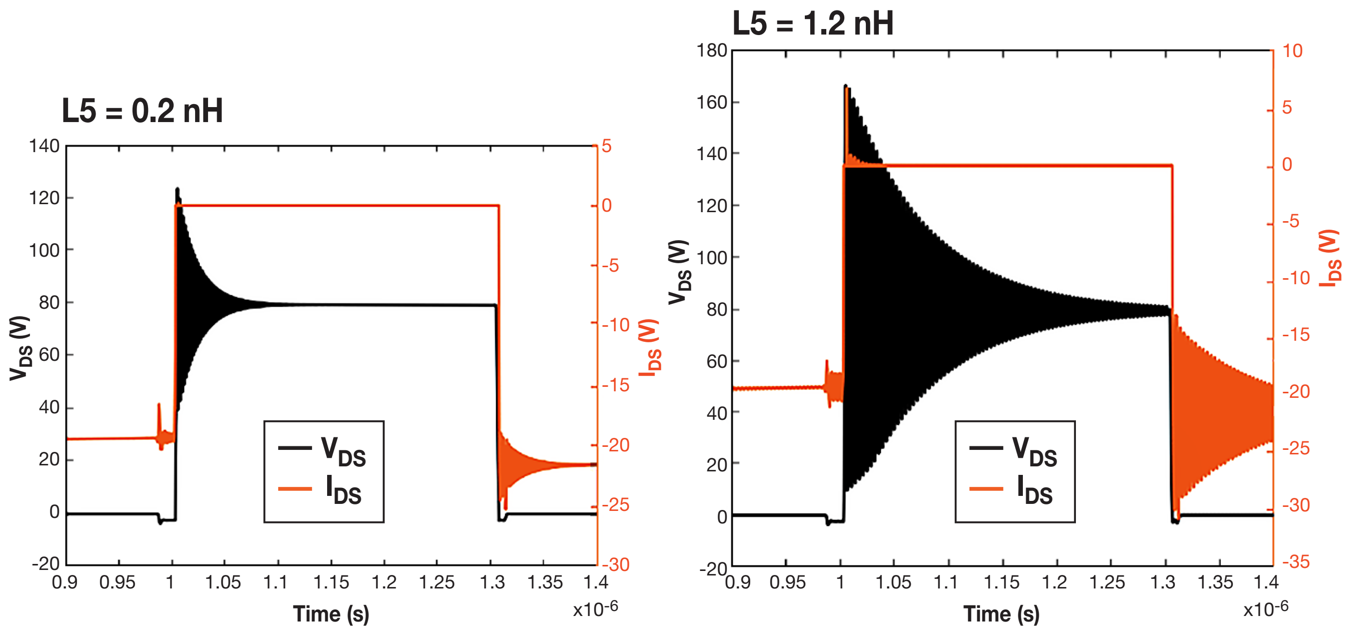


Figure 40: 48 V –12 V buck converter operating at 500 kHz. To produce different amounts of overshoot, L5 was varied from 0.2 nH to 1.2 nH. 0.2 nH resulted in a peak overshoot on the low-side device of 50 V above the 80 V DC bus (left), whereas a 1.2 nH inductor created a 90 V peak overshoot.

Figure 41 shows the amount of charge trapped in the first cycle as compared with the cumulative amount trapped in the 10-millionth cycle (Note the five orders of magnitude change in vertical axis and the high resolution of the scale). The red oval shows that, at some point from 1 to 10 million cycles, the characteristics changed. In fact, this is caused by the barrier height increasing slightly every time an electron is trapped. This makes it more difficult for all but the most energetic electrons to get trapped. This region includes some ringing, but the trapped electrons are due to the very small leakage current combined with the high V_{DS} when the device is nominally in the off state.

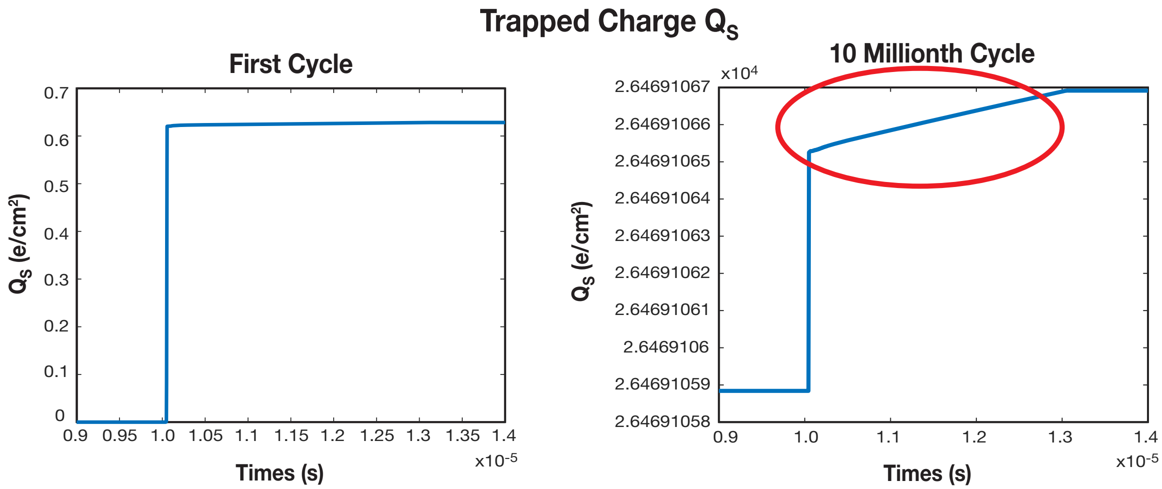


Figure 41: Amount of charge trapped Q_S in the first cycle as compared with the cumulative amount trapped in the 10-millionth cycle.

These data can be translated into the graphs in Figure 42. The upper pair show the trapped charge, Q_S, over time on the left, and the normalized $R_{DS(on)}$ on the right for the 0.2 nH inductor case. The lower graphs show the same information for the 1.2 nH case. Whereas there is a minimal increase in $R_{DS(on)}$ with ringing as high as 130 V peak, there is more significant evolution of $R_{DS(on)}$ when peak voltages go as high as 170 V.

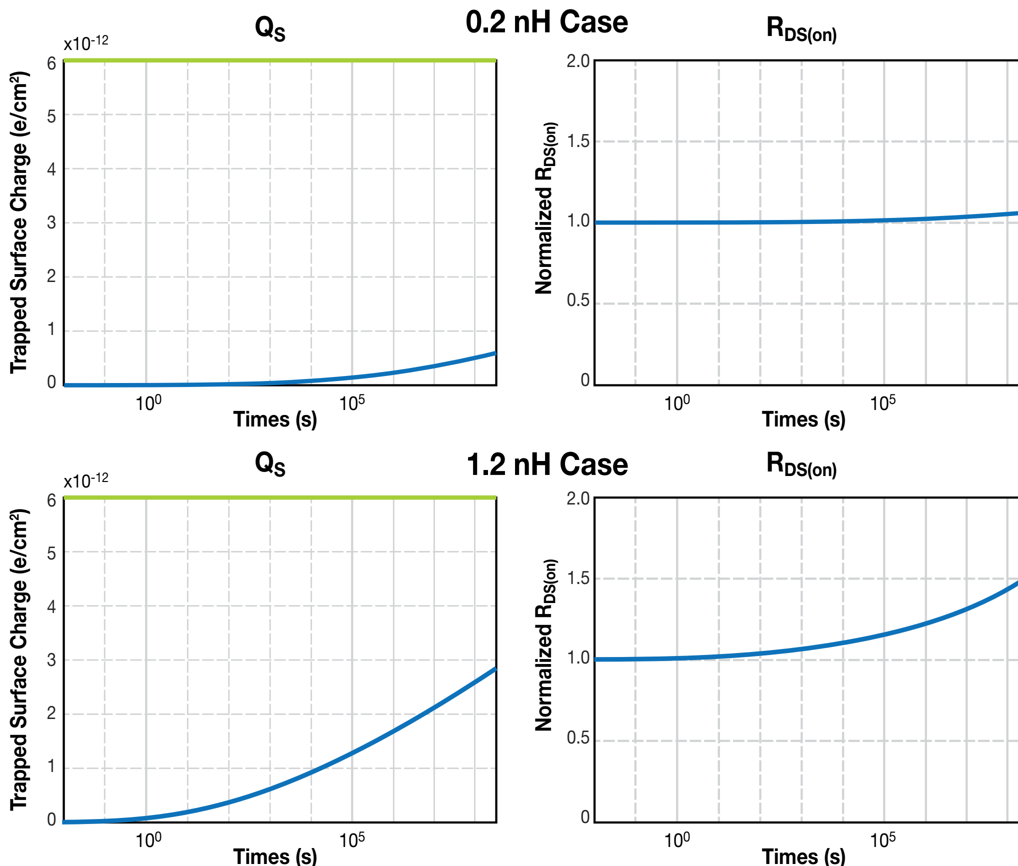


Figure 42: The upper pair of graphs show the trapped charge, Q_S, over time on the left, and the normalized, $R_{DS(on)}$, on the right for the 0.2 nH inductor case. The lower graphs show the same information for the 1.2 nH case.

9.3.2 High-Side GaN Transistor

In Figure 43 on the left are the current and voltage waveforms for the high-side control FET in the buck converter of Figure 39. This time the eGaN FET experiences hard-switching transitions at turn-on and turn-off. For the same value of L5 inductance (1.2 nH) the overshoot on the high-side device is only about 40 V, resulting in a peak overshoot voltage of 120 V. On the right are graphed the charge trapped in the first cycle (top) compared with the 10 millionth cycle (bottom). Noting the vertical scale change, as with the low-side transistor, the characteristics change as the amount of trapped charge increases in later cycles. There is a bump in charge that appears during the turn-off cycle at 1.3 µs that was not seen in the low-side device. In this part of the cycle the high-side transistor has a significant amount of current during the voltage decay in turn-off. There is therefore a significant supply of highly energetic electrons available for trapping.

As might be expected with the reduced peak overvoltage of 120 V on the high side device with 1.2 nH inductance, the minimal evolution of $dR_{DS(on)}$ is similar to that in Figure 42 for the 0.2 nH case as they both have about the same peak overshoot voltage as shown in Figure 44.

A physics-based model enables calculation of charge trapping for any given switching loci. Simulations show that current has a small impact, and voltage a much larger impact. In an LLC synchronous rectifier with a 12 V output, varying the leakage inductance from 50 pH to 150 pH on each leg of the transformer produced a different amount of overshoot, but not a significant amount of $dR_{DS(on)}$, even when using 30 V rated devices. In a buck converter, for both low-side and high-side transistors there were minimal changes in $R_{DS(on)}$ up to 130 V peak overshoot for the 100 V rated device. At 170 V peak overvoltage, $R_{DS(on)}$ of this 100 V device degraded only 50% over 10 years.

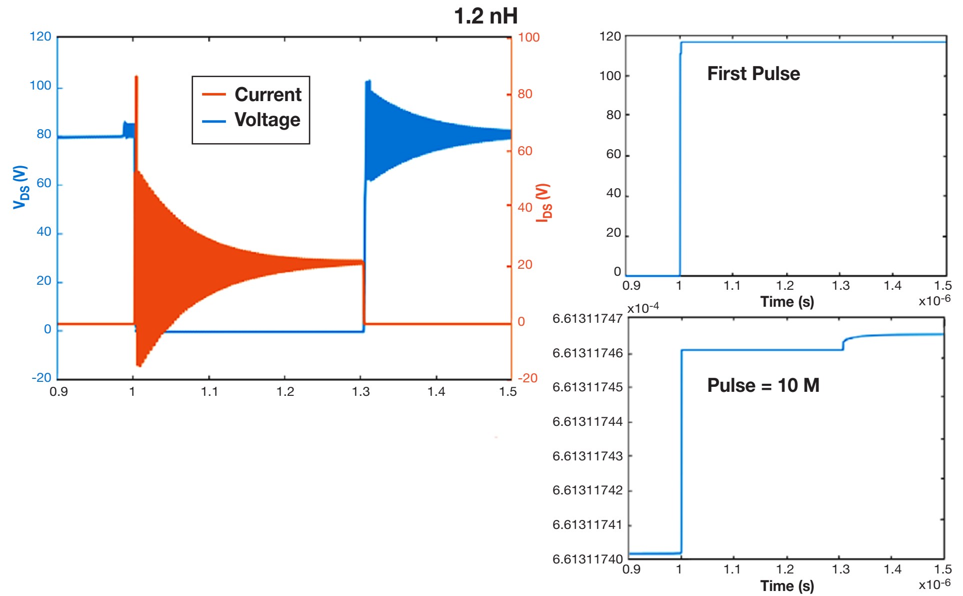


Figure 43: (left) Current and voltage waveforms for the high-side control FET in the buck converter of Figure 39. (right) Charge trapped in the first cycle (top) compared with the 10 millionth cycle (bottom).

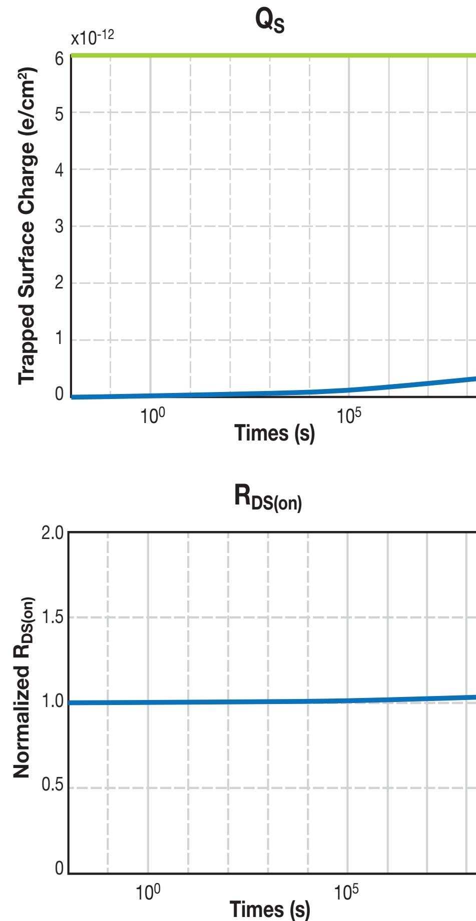


Figure 44: (Top) Trapped charge Q_S over time, and (bottom) normalized $R_{DS(on)}$. The horizontal scale ends on the right at 10 years.

9.4 Summary of Applying the Model to Important Real-World Use Cases

A physics-based model enables calculation of charge trapping for any given switching loci. Simulations show that current has a small impact, and voltage a much larger impact. In an LLC synchronous rectifier with a 12 V output, varying the leakage inductance from 50 pH to 150 pH on each leg of the transformer produced a different amount of overshoot, but not a significant amount of $R_{DS(on)}$ increase was measured, even when using 30 V rated devices.

In a buck converter, for both low-side and high-side transistors there were minimal changes in $R_{DS(on)}$ up to 130 V peak overshoot for the 100 V rated device. At 170 V peak overvoltage, $R_{DS(on)}$ of this 100 V device degraded only 50% over 10 years.

10: SUMMARY

GaN devices have been in volume production since 2010 and have demonstrated very high reliability in both laboratory testing and customer applications, such as lidar for autonomous cars, rooftop solar panels, vehicle headlamps, DC-DC converters for servers, and satellites to name just a few. Test-to-fail testing can isolate intrinsic failure mechanisms and their behavior over all stress conditions. Information gained from this testing can then be used with confidence to predict device lifetime under a wide range of actual mission profiles.

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