EPC eGaN® FETs Automotive Qualification Report EPC2212

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This report summarizes the Product Qualification results for EPC part numbers EPC2212 which meets all required AEC-Q101 requirements and is released for production.

Scope

The testing matrix in this report covers the qualification of EPC2212 in accordance with the component level AEC-Q101 Rev D1 requirements. For some of the required tests, EPC2212 is qualified by matrix with EPC2202, EPC2203, and EPC2206, also AEC qualified products. All four of these devices are compared in the table below. EPC2212 and EPC2202 share identically the same die outline, bump land pattern, and outer passivation (i.e. the same wafer level chip-scale "package"). Compared to EPC2202, EPC2212 has higher maximum gate and drain voltage ratings, lower $R_{DS(on)}$, and lower parametric shift during long term stress testing.

Part Number	Max V_{DS} (V)	Max V_{GS} (V)	Max $R_{DS(on)}$ (mΩ)	Die Size (mm x mm)	Max Operating Temperature (°C)
EPC2206	80	6	2.2	XL (6.05 x 2.3)	150
EPC2212	100	6	13.5	M (2.11 x 1.63)	150
EPC2202	80	5.75	17	M (2.11 x 1.63)	150
EPC2203	80	5.75	80	S (0.95 x 0.95)	150

EPC 80 V/100 V Automotive Product Family

Qualification Test Overview

EPC's EPC2212, EPC2202, EPC2203 and EPC2206 eGaN FETs were subjected to a wide variety of stress tests following the specifications of AEC-Q101 (Rev D1) developed for silicon-based power MOSFETs. These tests include:

- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1); (3) 3 times reflow
- Parametric Verification: Device parameters are measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet limits over the entire temperature range
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events
- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature and maximum rated voltage
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature and maximum rated gate voltage
- Unbiased highly accelerated test (uHAST): Parts are stressed in a non-condensing humid environment for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -55°C to 150°C for a total of 1000 cycles
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to 1000 hours of 85°C, 85% humidity with the drain biased at 80% of maximum rating
- Moisture sensitivity level 1 (MSL1): Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours

– Intermittent Operating Life (IOL): Parts are temperature cycled with short period and device heating through internal electrical power dissipation

- Destructive Physical Analysis: Parts are delayered and physically analyzed looking for defects resulting from stress testing

All devices put on test as part of this qualification underwent external visual inspection prior to test. This microscope inspection checks for physical damage to the chip-scale package, such as edge chipping or cracks, that may have resulted from assembly or transit. Damaged parts are removed from the test population.

For all qualification tests, the stability of the devices is verified with DC electrical tests before and after stress. In many cases, interim readouts are also performed. Electrical parameters are measured at room temperature. The parameters include: gate-source threshold voltage (V_{TH}), on-state resistance $R_{DS(on)}$, off-state drain leakage (I_{DSS}), and gate leakage (I_{GSS}). For V_{TH} and $R_{DS(on)}$, a failure is recorded when either of the following occurs: (i) the measurement exceeds the datasheet specifications; or (2) the measurement has changed by more than 20% of its initial value. For I_{DSS} and I_{GSS}, a failure is recorded if the measurement exceeds datasheet limit, or if it has increased by more than 5x during test. All testing requirements and specifications for AEC-Q101 (Rev D1) were followed.

For certain qualification tests, parts were mounted onto high Tg FR-4 (FR-5 or NP-175) or polyimide (Arlon 85NT) PCB adaptor cards. These cards simplify the process of post-screening and electrically stressing the parts. Adaptor cards (1.6 mm in thickness) with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder no clean flux was used in mounting the part onto an adaptor card. After assembly, parts were either baked or flux-cleaned.

For other qualifications tests, including MSL1 and TC, parts were not mounted to adaptor cards. Electrical tests were performed using probe needles touching the solder pads of the bare die.

While the AEC-Q101 standard was developed for silicon devices, many of the tests apply directly to EPC's eGaN FETs for the following reasons:

1) eGaN devices consist of a very thin film of GaN/AlGaN grown on a standard silicon substrate. Thermo-mechanically, they behave the same as a standard silicon die.

2) eGaN devices are processed using standard CMOS processes in a silicon foundry. This includes internal metal layers, dielectric layers, vias, passivation, and bump processes. For environmental reliability tests, eGaN devices are essentially the same as standard silicon flip-chip devices.

These arguments apply to environmental reliability type tests, including H3TRB, uHAST, TC, PC, MSL1 and IOL.

For tests such as HTRB and HTGB, the distinct physics of failure of eGaN compared to MOSFETs requires further study in order to confidently project service life based on 1000 hours of accelerated stress testing. In these cases, EPC takes a two-prong approach to help automotive customers gain confidence the needs of their mission profile will be met:

1) EPC conducts standard AEC-Q101 qualification of eGaN FETs, following all requirements and standards exactly. This establishes a reliability baseline.

2) EPC conducts additional operating life testing in test circuits that emulate the stress conditions seen in the application environment. Examples include both LIDAR and DC-DC conversion. These tests are often designed and implemented in cooperation with the end-users. The tests are designed to directly verify that the service life of the eGaN product will exceed mission requirements (typically 10 - 15 years of continuous operation). Operating life data of this type is not presented in this document, but is available upon request from EPC.

High Temperature Reverse Bias

Parts were subjected to 100% of the rated drain-source voltage at the maximum rated temperature (150°C) for a stress period of 1000 hours. As shown in Table 1 below, three separate lots of EPC2212 were stressed at 150°C for 1000 hours, satisfying AEC-Q101 requirements for a 150°C rating. HTRB results for closely related AEC products EPC2202, EPC2203, and EPC2206 are provided in Table 1 as well.

Parts were mounted on FR5 adapter cards. Testing was conducted in accordance with MIL-STD-750-1 (M1038 Method A). This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 24 hours after bias has been removed.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTRB	EPC2206	80	XL (6.05 x 2.30)	T = 150°C, V_{DS} = 80 V	0	77 x 3	1000
HTRB	EPC2212	100	M (2.11 x 1.63)	T = 150°C, V_{DS} = 100 V	0	77 x 3	1000
HTRB	EPC2202	80	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 x 3	1000
HTRB	EPC2203	80	S (0.95 x 0.95)	T = 150°C, V_{DS} = 80 V	0	77 x 3	1000

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts were subjected to maximum rated gate-source bias at the maximum rated temperature (150°C) for a stress period of 1000 hours. As shown in Table 2, three separate lots of EPC2212 were stressed at 6V and 150°C for 1000 hours. The number of lots, test duration and temperature satisfy the AEC-Q101 requirements for a 150°C rating. HTGB results for closely related AEC products EPC2202, EPC2203, and EPC2206 are provided in Table 2 as well.

Parts were mounted on FR5 adapter cards. Testing was conducted in accordance with JESD22-A108. This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 96 hours after bias has been removed.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTGB	EPC2206	80	XL (6.05 x 2.30)	T = 150°C, V_{GS} = 6.0 V	0	77 x 3	1000
HTGB	EPC2212	100	M (2.11 x 1.63)	T = 150°C, V_{GS} = 6.0 V	0	77 x 3	1000
HTGB	EPC2202	80	M (2.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	1000
HTGB	EPC2203	80	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	1000

Table 2. High Temperature Gate Bias Test

Unbiased Highly Accelerated Test

EPC2212 is qualified by matrix to EPC2202, which shares identically the same package (die outline, bump pattern, and outer passivation). Parts were subjected to 96 hours at a temperature of 130°C, relative humidity of 85%, and vapor pressure of 33.3 psia. As summarized in Table 3 below, three lots were tested for three separate in-family products: EPC2202, EPC2203, and EPC2206. All parts were mounted on FR5 adaptor boards. Per AEC requirements, all parts went through pre-conditioning before uHAST. During pre-screen and post-screen, EPC2202 parts were tested to 100 V (20 V beyond their datasheet limits), thereby qualifying the EPC2212 package over its full voltage range under uHAST.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
uHAST	EPC2206	80	XL (6.05 x 2.30)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 x 3	96
uHAST	EPC2202	80	M (2.11 x 1.63)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 x 3	96
uHAST	EPC2203	80	S (0.95 x 0.95)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 x 3	96

Note - EPC2212 is qualified by matrix.

Table 3. Unbiased Highly Accelerated Test

Temperature Cycling

EPC2212 is qualified by matrix to EPC2202, which shares identically the same package (die outline, bump pattern, and outer passivation). Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles. A ramp rate of 15°C/min and a dwell time of 5 minutes were used in accordance with the JEDEC Standard JESD22A104. All parts went through pre-conditioning prior to TC.

As seen in Table 4, three lots of EPC2202 passed the automotive requirement of 1000 cycles, with bare die (package) loaded into trays. In addition, two lots of EPC2202 passed AEC requirements with die assembled onto low CTE polyimide PCBs (Arlon 85NT). Two lots were assembled onto FR5 PCBs; these lots passed 500 cycles. During pre-screen and post-screen, EPC2202 parts were tested to 100 V (20 V beyond their datasheet limits), thereby qualifying the EPC2212 package over its full voltage range under TC.

TC results for in-family products EPC2202 and EPC2206 are shown in Table 4 as well

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cys)	Forrmat
TC	**EPC2206**	80	XL (6.05 x 2.30)	-55 to +150°C, Air	0	77 x 3	1000	Bare Die
TC	**EPC2206**	80	XL (6.05 x 2.30)	-55 to +150°C, Air	0	48 x 1	800 (on-going)	PCB (Arlon 85NT)
TC	**EPC2202**	80	M (2.11 x 1.63)	-55 to +150°C, Air	0	77 x 3	1000	Bare Die
TC	**EPC2203**	80	S (0.95 x 0.95)	-55 to +150°C, Air	0	77 x 3	1000	Bare Die
TC	**EPC2202**	80	M (2.11 x 1.63)	-55 to +150°C, Air	0	77 X 2	1000	PCB (Arlon 85NT)
TC	**EPC2202**	80	M (2.11 x 1.63)	-55 to +150°C, Air	0	77 x 2	500	PCB (FR5)
TC	**EPC2203**	80	S (0.95 x 0.95)	-55 to +150°C, Air	0	77 x 2	500	PCB (FR5)

Note - EPC2212 is qualified by matrix.

Table 4. Temperature Cycling Test

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias of 80% maximum voltage rating, 85% RH and 85°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A101, as required by AEC-Q101. All parts were mounted on FR5 adaptor boards. All parts went through pre-conditioning before H3TRB. Test results are summarized in Table 5. Three lots of EPC2212 passed 1000 hours stress at 80 V. In addition, five separate lots of EPC2202 (with the same package) all passed 1000 hours. Table 5 also shows data for EPC2203 (small) and EPC2206 (extra-large) within the same device family.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
H3TRB	**EPC2206**	80	XL (6.05 x 2.30)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 3	1000
H3TRB	**EPC2212**	100	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	77 x 3	1000
H3TRB	**EPC2202**	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 5	1000
H3TRB	**EPC2203**	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 3	1000

Table 5. High Temperature High Humidity Reverse Bias Test

Moisture Sensitivity Level 1

EPC2212 is qualified by matrix to EPC2202, which shares identically the same package (die outline, bump pattern, and outer passivation). MSL test results are summarized in Table 6. Parts were subjected to 85% RH at 85°C for a soak period of 168 hours. Within 4 hours after the soak, the parts underwent three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020. These conditions correspond to a moisture sensitivity level 1, the most stringent level of moisture sensitivity testing. For this testing, parts were loaded in trays in bare die form (not attached to PCBs). Pre-screen and post-screen were performed using probe needles to contact the solder pads of the bare die. During pre-screen and post-screen, EPC2202 parts were tested to 100 V (20 V beyond their datasheet limits), thereby qualifying the EPC2212 package over its full voltage range under MSL1.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)	Forrmat
MSL1	EPC2206	80	XL (6.05 x 2.30)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die
MSL1	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die
MSL1	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die

Note - EPC2212 is qualified by matrix.

Table 6. Moisture Sensitivity Level Test

Destructive Physical Analysis

In accordance with AEC-Q101 requirements, two EPC2212 parts were selected for physical analysis after successfully completing H3TRB testing. The physical analysis was conducted in three steps: (1) removal of die from PCB adapter card; (2) chemical removal of solder bumps/bars; (3) removal of top-layer passivation layers via dry etch. After each step, a high magnification optical microscope inspection was performed. No damage or abnormalities were observed as a result of prior stress testing.

Electrostatic Discharge (ESD) Sensitivity

EPC2212 is qualified by matrix to EPC2202, which shares the same package and terminal capacitances. EPC2202 was tested for ESD sensitivity using both the human body model (HBM) and charged device model (CDM). Testing was conducted according to AEC-Q101-001 and Q101-005 standards. Device parameters were measured before and after ESD testing. Results are shown in Table 7 below. EPC2202 passed HBM with a rating of 500 V, and CDM with a 1000 V rating.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	1000 V	1	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	750 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	1000 V	0	10 x 1

Note - EPC2212 is qualified by matrix.

Table 7. ESD HBM and CDM Tests

Parametric Verification

In accordance with AEC-Q101 requirements, device parameters were measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet specifications over the entire temperature range. Parametric verification was performed 3 lots x 25 parts, for EPC2212 and closely related EPC2202, EPC2203, and EPC2206.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
PV	EPC2206	80	XL (6.05 x 2.30)	T = –40, 25 , 150°C	0	25 x 3
PV	EPC2212	100	M (2.11 x 1.63)	T = –40, 25 , 150°C	0	25 x 3
PV	EPC2202	80	M (2.11 x 1.63)	T = –40, 25 , 150°C	0	25 x 3
PV	EPC2203	80	S (0.95 x 0.95)	T = –40, 25 , 150°C	0	25 x 3

Table 8. Parametric Verification Tests

Intermittent Operating Life

EPC2212 is qualified by matrix to EPC2202 and EPC2203. In accordance with MIL-STD-750 (Method 1037), parts are power cycled over a ΔTj = 125°C temperature range. Devices are heated through internal electrical power dissipation by biasing them in the linear mode, with combined gate and drain bias and a regulated drain current. With a 1 minute temperature ramp, and a 5 minute cool down, a minimum of 5000 cycles are required. Die were assembled onto low CTE polyimide PCBs (Arlon 85NT). As seen in Table 9, two lots of EPC2202 passed 5000 cycles, and one lot of EPC2203 passed 7500 cycles (exceeding AEC requirements).

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)	Forrmat
IOL	EPC2202	80	M (2.11 x 1.63)	ΔTj = 125°C; ton / toff = 1 min /5 min	0	77 x 2	5000	PCB (Arlon 85NT)
IOL	EPC2203	80	S (0.95 x 0.95)	ΔTj = 125°C; ton / toff = 1 min /5 min	0	77 x 1	7500	PCB (Arlon 85NT)

Note - EPC2212 is qualified by matrix.

Table 9. Intermittent Operating Life Tests