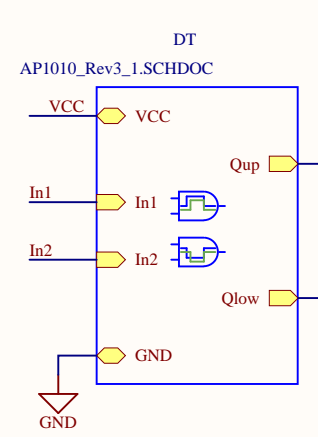
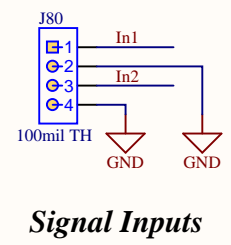
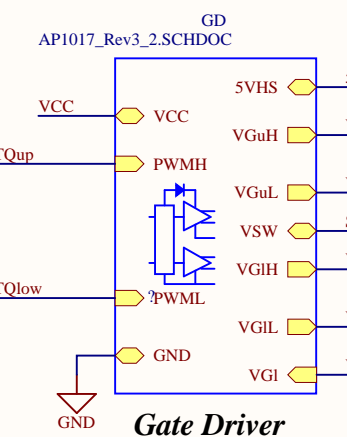


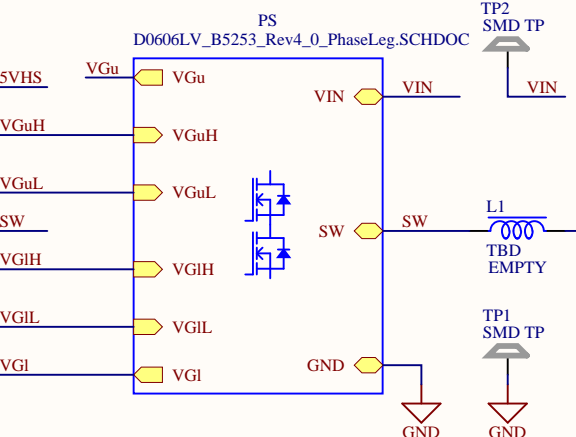
Main Supply Input



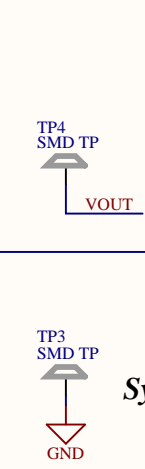
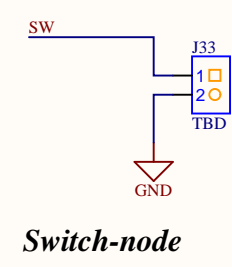
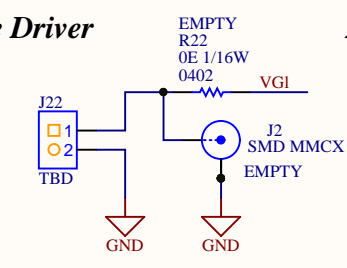
dead-time and buffers



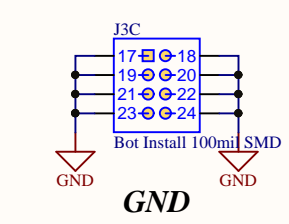
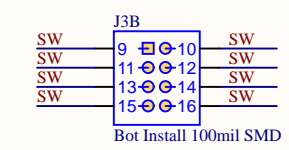
Gate Driver



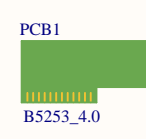
Power Stage



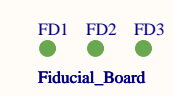
Sync Buck Output



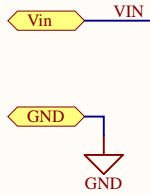
Serial# yyww-



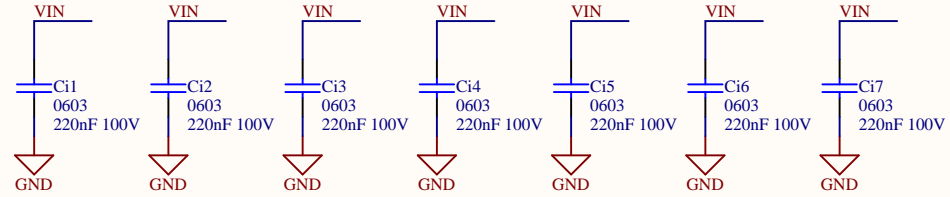
For evaluation only;
not FCC approved for resale



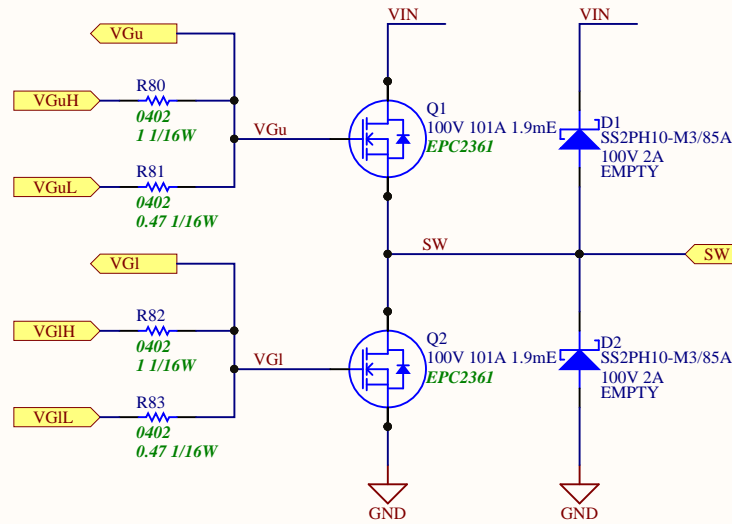
Title: Evaluation Board Main Schematic		© EPC 2024
Design #: EPC90156	PCB #: B5253	Efficient Power Conversion 909 Pacific Coast Hwy. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 4.0	Revision: 4.0	
Date: 3/7/2024	Sheet 1 of 5	
File: D0606LV_B5253_Rev4_0.SCHDOC		



DC Input
80 Vmax.



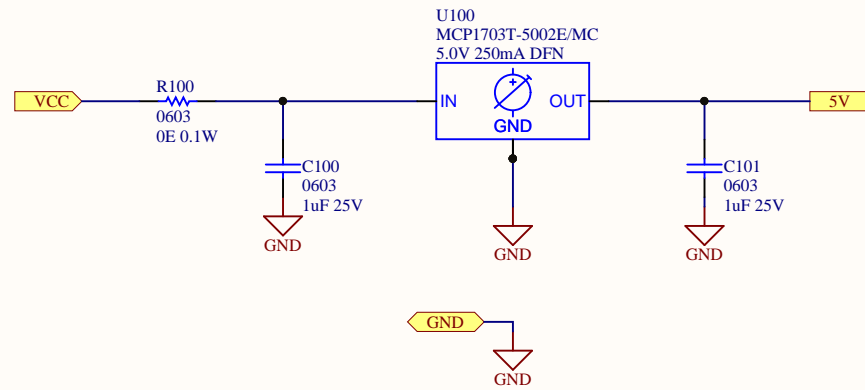
HF loop Capacitors




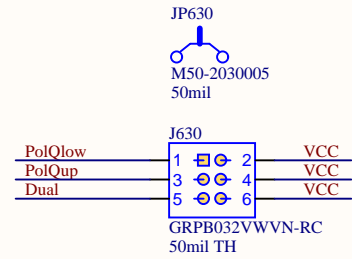
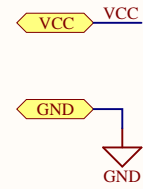
Power Stage

Optional Diodes

Title: Symmetrical Phase Leg With Synchronous Bootstrap		© EPC 2024
Design #: Half-Bridge Phase Leg		Efficient Power Conversion 909 Pacific Coast Hwy, Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1.0	P/N#: EPC2361	
Date: 3/7/2024	Sheet 2 of 5	
File: D0606LV_B5253_Rev4_0_PhaseLeg.SCHDOC		

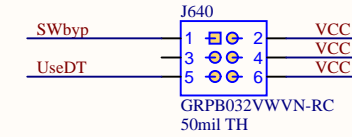


Title: 12 V to 5 V LDO power supply		© EPC 2023
Design #: AP1006		Efficient Power Conversion 909 Pacific Coast Hwy. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 2.2		
Date: 2/19/2024	Sheet 3 of 5	
File: AP1006_Rev2_2.SCHDOC		



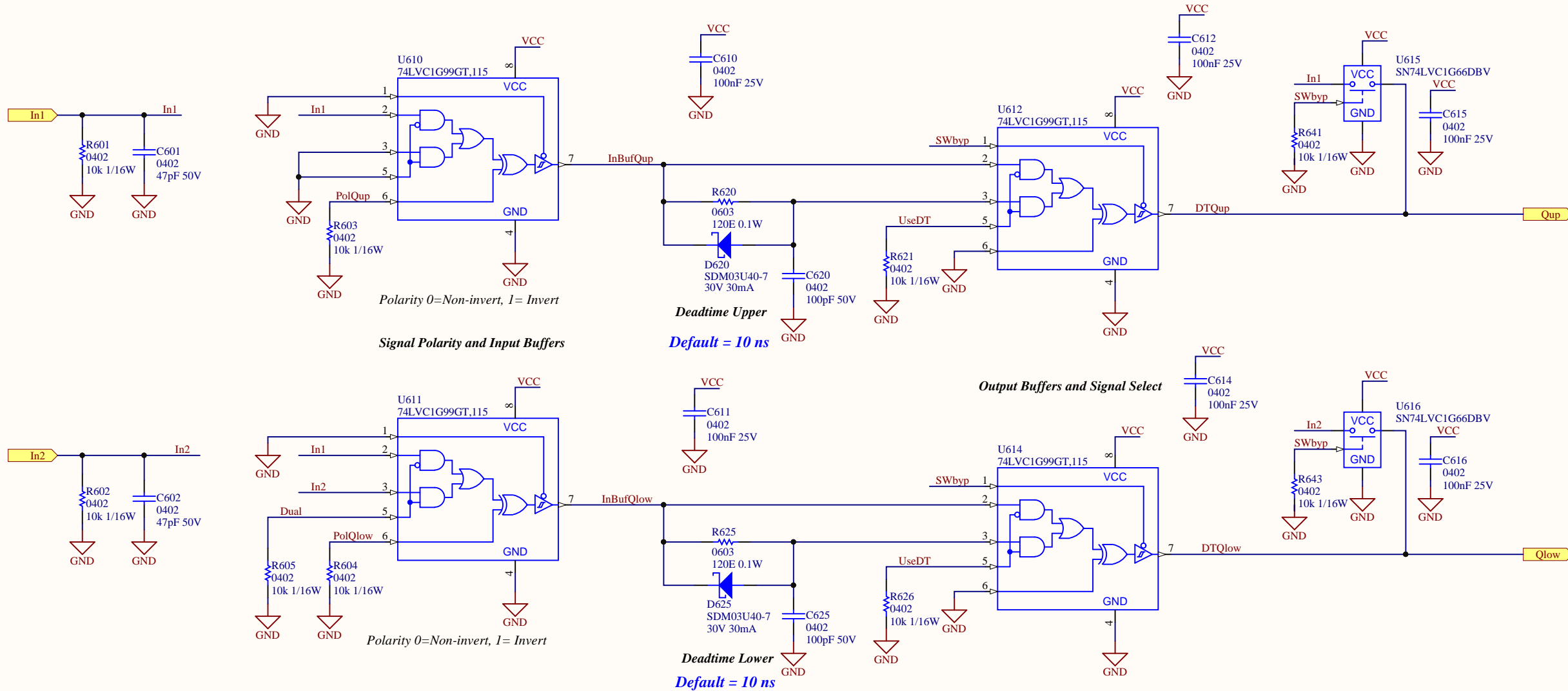
Buck Single Signal
Boost Single Signal
Dual Signal

Dual/Single PWM, Buck, and Boost Mode Selector

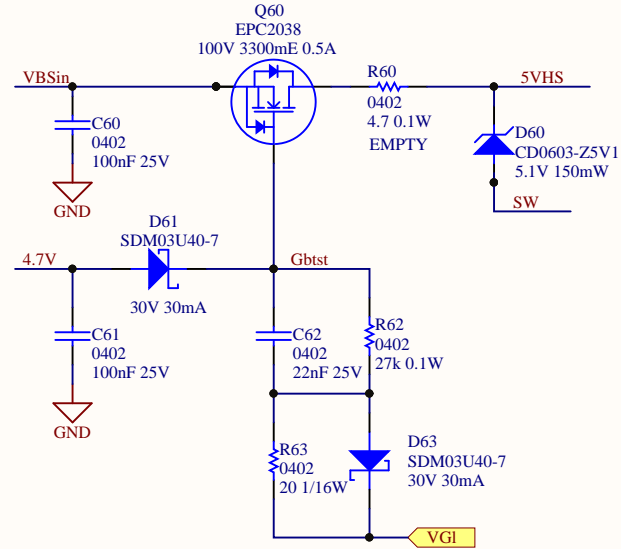
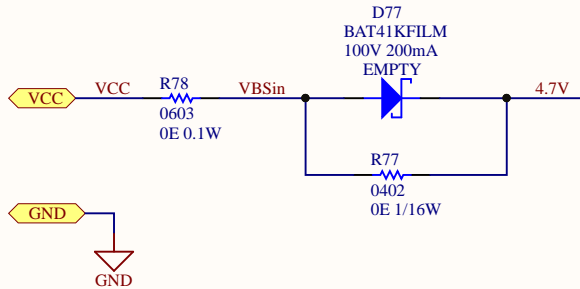


Full Bypass
DT Bypass
No Bypass

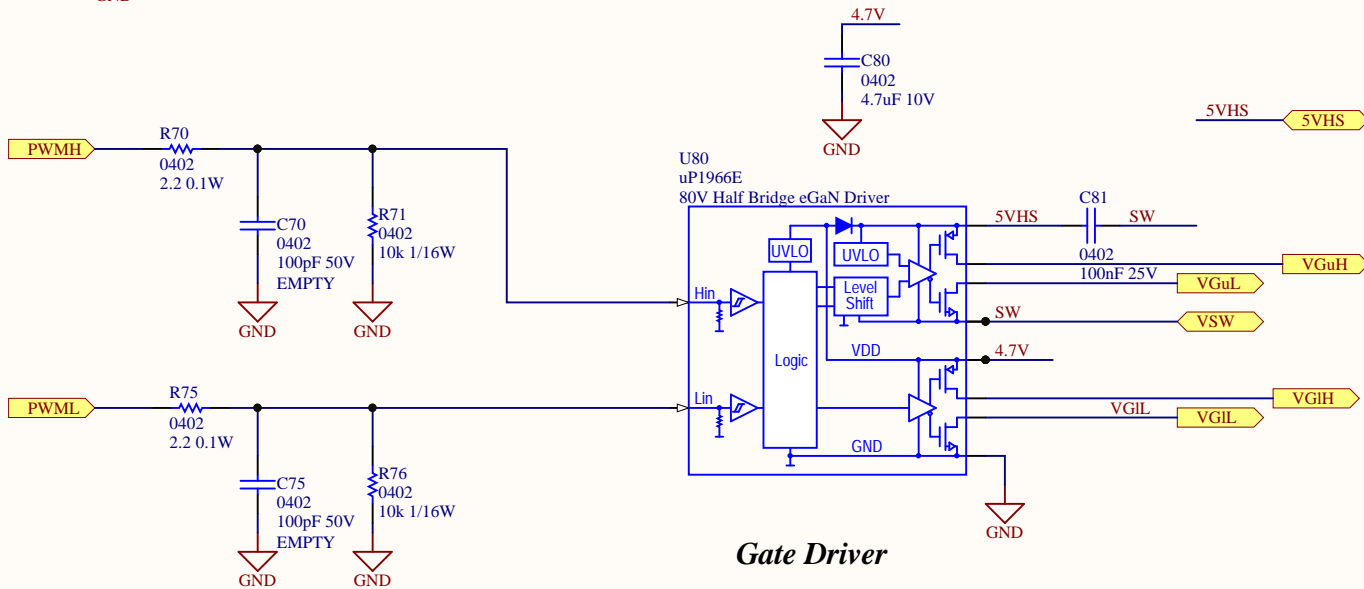
Bypass Mode Select




Sync Boot = Install R60 and D77, remove R77
 No Sync Boot = Install R77, remove R60 and D77
 Default = No Sync Boot



Synchronous Bootstrap Power Supply



Gate Driver

Title: 80 V HB Gate Driver with Synchronous Bootstrap		© EPC 2023
Design #: AP1017		Efficient Power Conversion 909 Pacific Coast Hwy. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com 
Revision 3.2		
Date: 2/19/2024	Sheet 5 of 5	
File: AP1017_Rev3_2_SCHDOC		