EPC GaN® FETs Application Readiness: Phase Five Testing

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Efficient Power Conversion Corporation's enhancement mode Gallium Nitride (eGaN®) FETs, although similar to standard power MOSFETs, deliver performance unattainable by silicon-based devices [1]. EPC eGaN FETs enable power converters to achieve higher efficiency while maintaining the simplicity of older designs [2,3,4]. Joining the first generation eGaN FETs and the second generation 40 V and 100 V product, EPC introduced its second generation 200 V product family [5] in 2011. All second generation products are lead-free, halogen free, and RoHS compliant. EPC's risk-reduction results to date include the testing of more than 1800 devices in a wide variety of stress conditions. Over 1.7 million accumulated device hours of reliability testing validate the readiness of eGaN FETs to supplant their aging silicon cousins for most commercial power switching applications. This application note focuses on the second generation 200 V device reliability test results, as well as other new tests completed since the Phase Four Report [13]. The statistical failure rate is also calculated based on the stress tests completed.

RELIABILITY TEST OVERVIEW

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts are subjected to gate-source voltages at the maximum rated temperature
- Operating Life: Parts are assembled onto power supply boards and the boards are subjected to actual switching power conversion operating conditions
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied
- Temperature cycling (TC): Parts are subjected to alternating high- and low temperature extremes
- Unbiased autoclave (AC or Pressure Cooker Test): Parts are subjected to pressure, humidity, and temperature under condensing conditions
- Moisture sensitivity level test: Parts are subjected to moisture, temperature, and three cycles of reflow

The stability is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are typically stressed for1000 hours or as applicable to meet JEDEC standards. Some tests are taken up to multiple thousands of hours to check the performance over longer periods of time.

Parts were mounted onto FR408 or FR5 adaptor cards unless otherwise stated. Adaptor cards with two copper layers or four copper layers were used. Two ounce copper was used for the two layer cards; one ounce outer layers and two ounce inner layers were used for the four layer cards. The solder paste materials used when mounting the parts were AIM lead-free no-clean NC257-2 SAC305 [6] and Senju Metal Industrial Co. (SMIC) lead-free M705-GRN360-K-V SAC305 [7]. A typical reflow profile using the Senju M705-GRN360 solder paste is shown in the previous reliability test report [13]. The underfill materials used, where applicable, were Loctite Hysol FP4549Si [8] and Shin-Etsu SMC375X7 [9].

RELIABILITY TEST RESULTS

Table 1 is a summary of the test results from the first-generation eGaN FETs, and Table 2 is a summary of the test results from the second-generation products. More than 1800 units of first and second generation devices have been stressed at their maximum rated temperatures for a total of more than 1.7 million device hours. Device electrical parameters remained stable over the stress period for all tests performed.

A complete record of eGaN FET test results and analysis can be found in the Phase One through Phase Four test reports posted on the company website [10, 11, 12, 13]. New test results obtained on the second generation 200 V products and the other results since the phase four report are discussed in the following sections.

HIGH TEMPERATURE REVERSE BIAS

During the HTRB test the devices were DC biased with a high drain-source voltage at the maximum rated operating temperature. Over 400 parts have been tested without failure.

In the most recent tests EPC2010 (200 V, 25 mΩ) and EPC2012 (200 V, 100 mΩ) FETs were subjected to 125°C with 160 V drain-source applied. Forty-five devices in each group were tested for a period of 1000 hours and all device parameters remained stable over the full stress period. The $R_{DS(on)}$ of the EPC2010 versus the stress hours on HTRB is shown in Figure 1; $V_{GS(TH)}$ is shown in Figure 2; and I_{DSS} is shown in Figure 3. The $R_{DS(on)}$ of the EPC2012 versus the stress hours on HTRB is shown in Figure 4.

Table 1. Reliability Test Results for the First-Generation eGaN® FETs

Stress Test	Part Number	Underfill	Test Condition	Results (# of Fails)	Sample Size	Duration	
HTRB	EPC1001	-	T = 125°C, V_{DS} = 100 V	0	45	1000	Hrs
HTRB	EPC1014	-	T = 125°C, V_{DS} = 40 V	0	50	1000	Hrs
HTRB	EPC1012	-	T = 125°C, V_{DS} = 200 V	0	50	1000	Hrs
HTRB	EPC1010	FP4549Si	T = 125°C, V_{DS} = 200 V	0	50	1000	Hrs
HTRB	EPC1010	-	T = 150°C, V_{DS} = 200 V	0	50	3000	Hrs
HTGB 5 V	EPC1001	-	T = 125°C, V_{GS} = 5 V	0	45	3000	Hrs
HTGB 5.4 V	EPC1001	-	T = 125°C, V_{GS} = 5.4 V	0	45	3000	Hrs
HTGB 5 V	EPC1010	-	T = 150°C, V_{GS} = 5 V	0	45	1000	Hrs
HTGB -5 V	EPC1001	-	T = 125°C, V_{GS} = -5 V	0	50	1000	Hrs
TC	EPC1001	-	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC1014	-	-40 to +125°C, Air	0	50	1000	Cys
TC	EPC1012	-	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC1012	FP4549Si	-40 to +125°C, Air	0	45	1000	Cys
H3TRB	EPC1014	-	T = 85°C, RH = 85%, V_{DS} = 40 V	0	45	1000	Hrs
H3TRB	EPC1015	-	T = 85°C, RH = 85%, V_{DS} = 40 V	0	45	1000	Hrs
H3TRB	EPC1010	-	T = 85°C, RH = 85%, V_{DS} = 100 V	0	25	1000	Hrs
H3TRB	EPC1010	FP4549Si	T = 85°C, RH = 85%, V_{DS} = 100 V	0	25	1000	Hrs
MSL1	EPC1001	-	85°C/85 RH, 168 HR, 3 Reflow	0	50	168	Hrs
AC	EPC1001	-	121°C/100% RH, 29.7 psia, 96 HR	0	80	96	Hrs
AC	EPC1015	-	121°C/100% RH, 29.7 psia, 96 HR	0	80	96	Hrs
RTOL	EPC1001	-	10 A, 250 kHz, 30°C	0	10	1200	Hrs
HTOL	EPC9001	-	10 A, 750 kHz, 85°C T_J	0	5	2920	Hrs
HTOL	EPC9002	-	9 A, 200 kHz, 85°C T_J	0	3	2920	Hrs

Table2. Reliability Test Results for the Second-Generation Lead-Free eGaN® FETs

Stress Test	Part Number	Underfill	Test Condition	Results (# of Fails)	Sample Size	Duration	
HTRB	EPC2015	-	T = 150°C, V_{DS} = 40 V	0	45	1000	Hrs
HTRB	EPC2001	-	T = 125°C, V_{DS} = 100 V	0	45	1000	Hrs
HTRB	EPC2010	-	T = 125°C, V_{DS} = 160 V	0	45	1000	Hrs
HTRB	EPC2012	-	T = 125°C, V_{DS} = 160 V	0	45	1000	Hrs
HTGB 5 V	EPC2015	-	T = 150°C, V_{GS} = 5 V	0	50	1000	Hrs
HTGB 5 V	EPC2001	-	T = 150°C, V_{GS} = 5 V	0	45	1000	Hrs
TC	EPC2001	-	0 to +105°C, Air	0	95	3000	Cys
TC	EPC2001	SMC375X7	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC2012	-	-40 to +125°C, Air	0	45	850	Cys
H3TRB	EPC2015	SMC375X7	T = 85°C, RH = 85%, V_{DS} = 40 V	0	145	1000	Hrs
H3TRB	EPC2015	-	T = 85°C, RH = 85%, V_{DS} = 40 V	0	50	1000	Hrs
H3TRB	EPC2010	-	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50	1000	Hrs
H3TRB	EPC2012	-	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50	1000	Hrs
HTOL	EPC9002	-	9 A, 200 kHz, 105°C T_J	0	5	1000	Hrs
MSL1	EPC2015	-	85°C/85 RH, 168 HR, 3 Reflow	0	25	168	Hrs
MSL1	EPC2001	-	85°C/85 RH, 168 HR, 3 Reflow	0	25	168	Hrs

HIGH TEMPERATURE GATE BIAS

In HTGB test devices were biased with a gate-source voltage at the maximum rated temperature. A total of 280 parts have been tested without failure at temperatures ranging from 125°C to 150°C and V_{GS} ranging from 5 V to 5.4 V.

In the most recent tests EPC2015 devices were subjected to 150°C with 5 V applied from gate to source. Fifty devices were tested and all passed 1000 hours with all electrical parameters remaining stable over the stress period. The gate leakage over stress time is shown in Figure 5 as an example.

HIGH TEMPERATURE HIGH HUMIDITY REVERSE BIAS

In H3TRB testing devices were subjected to 85% relative humidity at 85°C with a high drain-source bias applied. Over 400 FETs have been H3TRB stress tested without failure.

In most recent tests EPC2010 and EPC2012 devices were stressed with 100 V applied from drain to source. Fifty devices in each group were tested and all passed 1000 hours. The drain leakage (I_{DSS}) and the on-state resistance ($R_{DS(on)}$) of the EPC2010 are shown in Figure 6 and 7, respectively. The I_{DSS} and the $R_{DS(on)}$ of the EPC2012 are shown in Figure 8 and 9, respectively.

TEMPERATURE CYCLING

Temperature cycling tests the ability of components and solder interconnects to withstand thermal-mechanically induced stresses. The solder interconnect stability is dependent on solder material, PCB pad design, and the soldering process. At this point six lots, with forty-five or more samples in each lot, have passed 850 temperature cycles between -40°C to 125°C.

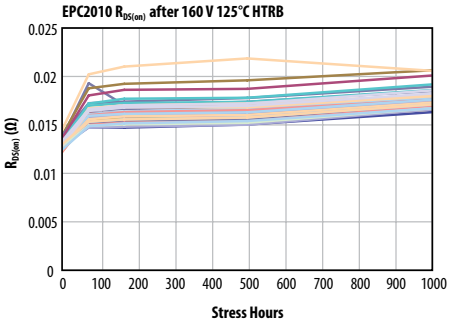

Figure 1. $R_{DS(on)}$ of the EPC2010 stressed to 160 V 125°C HTRB for a period of 1000 hours.

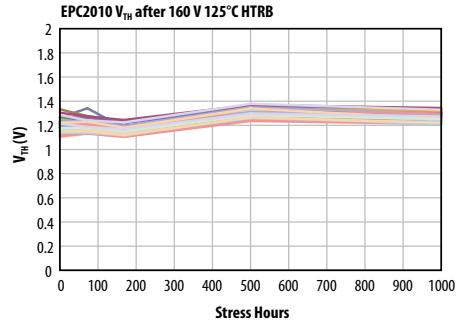

Figure 2. $V_{GS(TH)}$ of the EPC2010 stressed to 160 V 125°C HTRB for a period of 1000 hours.

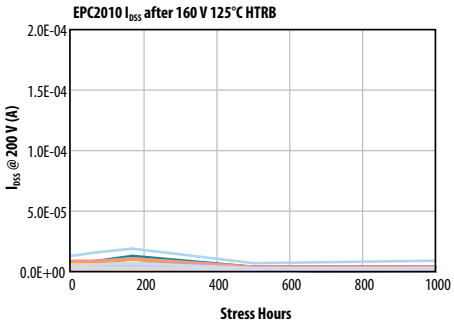

Figure 3. I_{DSS} of the EPC2010 stressed to 160V 125°C HTRB for a period of 1000 hours.

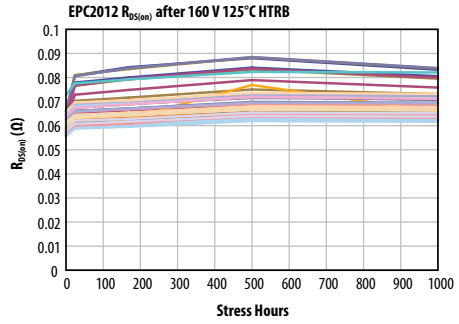

Figure 4. $R_{DS(on)}$ of EPC2012 stressed to 160 V 125°C HTRB for a period of 1000 hours.

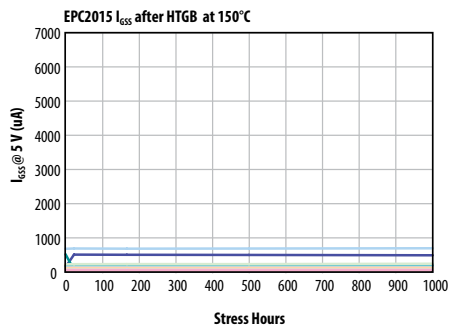

Figure 5. I_{GSS} of EPC2015 stressed to 5 V 150°C HTGB for a period of 1000 hours.

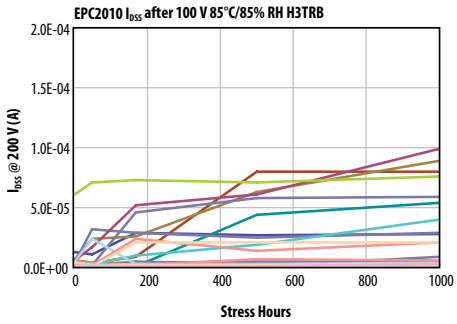

Figure 6. I_{DSS} of the EPC2010 stressed to 85°C, 85% RH and 100 V drain-source H3TRB for a period of 1000 hours.

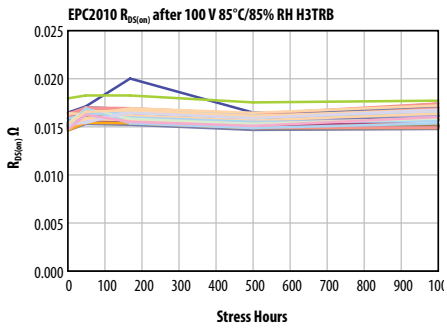

Figure 7. $R_{DS(on)}$ of the EPC2010 stressed to 85°C, 85% RH and 100 V drain-source H3TRB for a period of 1000 hours.

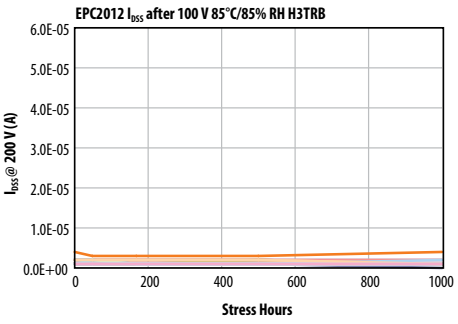

Figure 8. I_{DSS} of the EPC2012 stressed to 85°C, 85% RH and 100 V drain-source H3TRB for a period of 1000 hours.

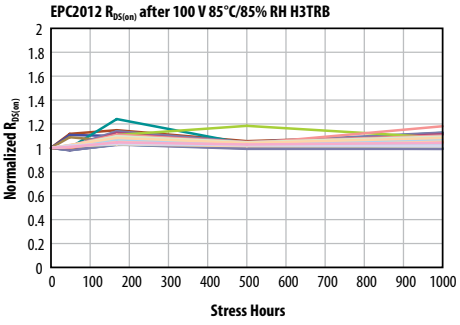

Figure 9. $R_{DS(on)}$ of the EPC2012 stressed to 85°C, 85% RH and 100 V drain-source H3TRB for a period of 1000 hours.

In the most recent tests, EPC2012 FETs were temperature cycled between -40°C to 125°C and passed 850 cycles meeting the acceptance criteria required by the JEDEC Standard JESD47.01.

Ninety-five EPC2001 were mounted and temperature cycled between 0°C and 100°C. They passed 3000 cycles, exceeding the 2300 cycles of acceptance criteria required by JESD47.01. Parts did start to show failures after 3000 cycles due to the cracking of the solder joints. Figure 10 shows the $R_{DS(on)}$ at each interim read out point and, after 3000 cycles a few parts are "open". When the gate solder joint becomes open devices would also show high drain-source leakage (see Figure 11). Figure 12 is a cross section of the gate solder joint after 3200 cycles showing cracks in the solder joint near the die surface.

HIGH TEMPERATURE OPERATING LIFE

The first generation EPC9001 is a half-bridge development board featuring EPC1015 eGaN FETs and includes on-board gate drivers [14]. The first generation EPC9002 is also a half-bridge development board with on-board gate drivers, and features EPC1001 eGaN FETs [15]. The purpose of these development boards is to simplify the evaluation process of the eGaN FET by including all the critical components, such as gate drivers, power decoupling, etc., on a single board that can be easily connected to an existing circuit.

Both development boards were operated open-loop on a multi-position burn-in mother board with a fixed pulse width and frequency. This kind of test is particularly useful because, in a standard "Buck" topology DC-DC converter operation with a high V_{IN}/V_{OUT} ratio, the control FET is turned ON with a very low duty cycle; conversely, the rectifier FET is turned ON with a very high duty cycle. This test simultaneously stresses devices both at high drain-source voltage and high drain current under actual, fast-switching conditions. Since the rectifier FET has very little switching losses, and the control FET has very little conduction losses, the effects of these two different operating conditions can be evaluated simultaneously.

The EPC9001 board was operated at 22 V_{IN} and 0.85 V_{OUT}, 10 A, at a switching frequency of 750 kHz. The EPC9002 board was operated at 60 V_{IN} and 0.9 V_{OUT}, 9 A, at a switching frequency of 200 kHz.

The board temperature was checked using an FLIR T300 infrared camera. The max PCB board temperature was about 70°C and varied from board to board and over time within a few degrees (±5°C). The junction temperature was estimated to be around 85°C taking into account the junction-to-board thermal resistance [16].

The circuit efficiency was measured at time-zero, 180, 500, 1000, 2000, and 2920 hours. The EPC9001 efficiency was measured at 300 kHz, 20 V_{IN} to 1 V_{OUT}, 15 A, and the EPC9002 efficiency was measured at 300 kHz, 60 V_{IN} to 1.5 V_{OUT}, 10 A. Typical efficiency measured with a test fixture was about 86% for the EPC9001 and 80% for the EPC9002. The normalized efficiency was plotted in Figure 13 for EPC9001 and in Figure 14 for EPC9002. Both EPC9001 and EPC9002 showed stable performance.

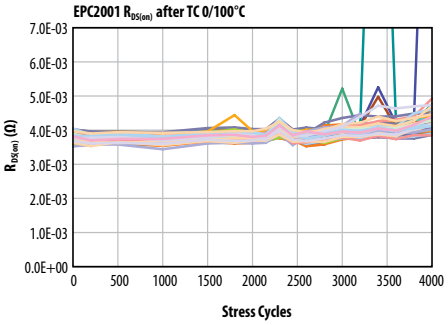

Figure 10. $R_{DS(on)}$ of EPC2001 stressed by temperature cycling between 0°C and 100°C.

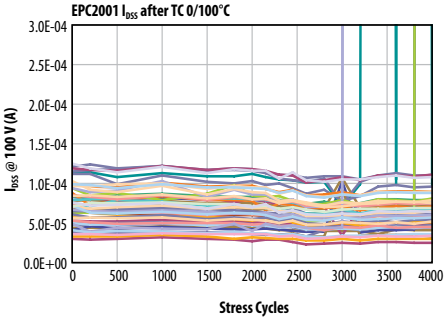

Figure 11. I_{DSS} of EPC2001 stressed by temperature cycling between 0°C and 100°C.

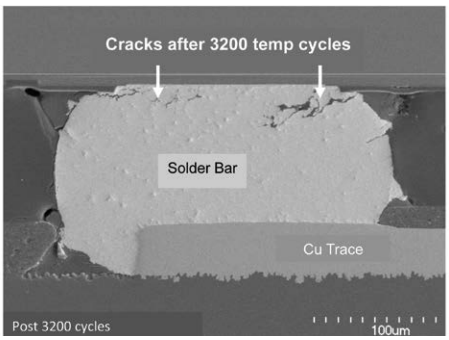

Figure 12. Cross section of the gate solder joint after 3200 cycles between 0°C and 100°C.

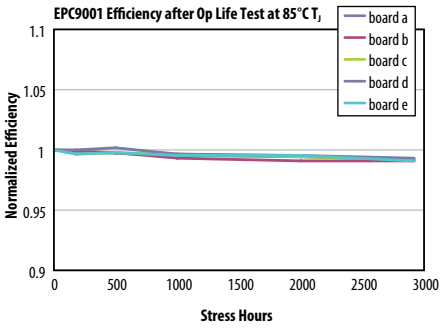

Figure 13. Normalized power conversion efficiency for the EPC9001 over 2920 operating hours.

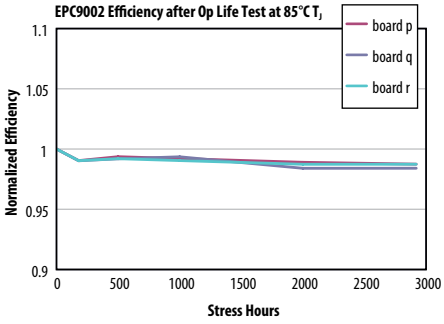

Figure 14. Normalized power conversion efficiency for the EPC9002 over 2920 operating hours.

The second generation EPC9002 features the lead-free EPC2001 eGaN FETs. The EPC9002 were operated open-loop on the same multi-position burn-in mother board as the first generation boards. These development boards were operated at 60 V_{IN} and 1 V_{OUT}, 10 A, at a switching frequency of 300 kHz. The PCB board temperature was checked using an FLIR T300 infrared camera. The max PCB board temperature was about 90°C and varied from board to board and over time within a few degrees (±5°C). The device junction temperature was estimated to be around 105°C taking into account the junction-to-board thermal resistance.

The EPC9002 efficiency was measured the same way as the previous generation boards at 300 kHz, 60 V_{IN} and 1.5 V_{OUT}, 10 A. Typical efficiency measured with a test fixture was about 82%. The normalized efficiency over the stress period of 1000 hours is shown in Figure 15.

FAILURE RATE

Reliability is typically expressed by the probability that a part will perform its intended function for a specific period of time under defined operation conditions. The failure rate

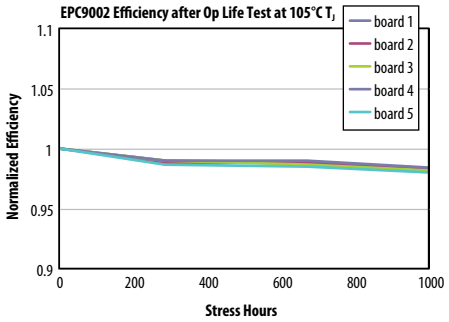

Figure 15. Cross section of the gate solder joint after 3200 cycles between 0°C and 100°C.

is typically expresses in units of FITs, or failures in one billion hours of operation. The statistical estimate of the FIT rate can be calculated from device hours by using equation (1).

$$FIT = (\chi^2_{(\alpha,\ 2r+2)}/(2*N*t*AF))*10^9 \quad (1)$$

Where:

$\chi^2_{(2r+2)}$:
CHI-square distribution factor with 2r+2 degree of freedom

α: risk associated with confidence level between 0 and 1

r: total number of failures

N: total number of device tested

t: test duration for each device at the given test conditions

AF: acceleration factor

The mean time to fail (MTTF) can be calculated from the reciprocal of the FIT multiplied by 10^9 hours (Equation 2).

$$MTTF = 10^9/FIT \quad (2)$$

The statistical FIT rate for the eGaN FETs is calculated from the operating life test data collected from the RTOL and the HTOL tests shown in Table 1 and Table 2. Since these devices are all made with the same technology, the data from these parts are combined in the preliminary FIT calculation. We have also ignored the differences in operating conditions and no acceleration factor is used in the FIT calculation. 68,720 cumulative device-hours have been accrued with zero failure which results in a FIT rate of 13,300 with a 60% confidence level. The MTTF is about 75,000 hours from this preliminary FIT value and is limited by the statistical data since there were no failures.

The FIT rate can also be calculated from all the stress tests combined. 1.7 million device-hours have been accumulated with zero failures. Without applying any acceleration factors the calculated FIT rate is 538 with a 60% confidence level. This results in an estimated MTTF of over 212 years.

FUTURE WORK

The projected FIT rate presented is preliminary. More data will be collected for a better statistical estimate. Temperature and voltage acceleration factors will also be investigated in future reports. Since eGaN technology employs a new type of semiconductor material, acceleration factors used for silicon may not be applicable [17].

SUMMARY

EPC's eGaN FETs bring designers significant performance and size advantages over silicon power MOSFETs. These advantages can be used to improve system efficiency, reduce system cost, reduce size, or a combination of all three. Because EPC's products were designed as power MOSFET replacements, designers can use their existing building blocks, skills and knowledge with only minor changes.

This application note reported the test results for the second generation 200 V new product and other new test results obtained since the Phase Four Report. The test data demonstrated that the eGaN technology is robust under a wide range of stress conditions.

The second generation eGaN FETs are lead-free, halogen free, and RoHS compliant (see Appendix I). EPC has received ISO9001:2008 certification for its quality management system in September of 2011 (see Appendix II).

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APPENDIX I: ROHS AND HALOGEN FREE

EPC's lead-free eGaN FETs are sold as bare die with a Land Grid Array (LGA) of lead-free solder bars. The solder material is 95.5Sn/4.0Ag/0.5Cu. The lead-free product line follows part number nomenclature EPC2xxx.

The final product wafers with solder bumps are RoHS compliant in accordance with the RoHS Directive 2002/95/EC. Details of the test report done by SGS Taiwan Ltd, can be found in the report published by SGS, report number CE/2010/A1486.

EPC's lead-free product was also tested for halogen element levels using the method in accordance with reference BS EN 14582:2007. None of the halogen elements were detected in the test. Details of the test results can be found in the above SGS test report CE/2010/A1486.

APPENDIX II: ISO9001:2008 CERTIFIED

EEPC has received the International Organization for Standardization ISO 9001:2008 certification for its quality management system in September 2011.

The ISO standards are published by the International Organization for Standardization and available through national standards bodies. To achieve certification, EPC passed an assessment conducted by Det Norske Veritas, an ANSI-ASQ National Accreditation Board (ANAB) certified auditor.