Using GaN FETs with Controllers and Gate Drivers Designed for Silicon MOSFETs

Gallium Nitride (GaN) FETs have revolutionized the power electronics industry, offering advantages such as smaller size, faster switching, higher efficiency, and lower costs compared to traditional silicon MOSFETs. However, the rapid evolution of GaN technology has sometimes outpaced the development of dedicated GaN-specific gate drivers and controllers. Consequently, circuit designers often turn to generic gate drivers designed for silicon MOSFETs, necessitating careful consideration of various factors to ensure optimal performance.

By Alejandro Pozo, Ph.D., Senior Applications Engineer, Efficient Power Conversion

This article explores the key differences between GaN FETs and silicon MOSFETs, provides recommendations for using generic gate drivers with GaN FETs, and outlines essential modifications for half-bridge gate drivers and controllers.

Main differences between GaN transistors and Si MOSFETs
eGaN® FETs, exhibit distinct characteristics compared to silicon MOSFETs, impacting their operation with gate drivers designed for the latter. Some of the key differences include:

a. **Lower Gate Voltage Levels:** eGaN FETs from EPC require a gate voltage of 5 V for turn-on and 0 V for turn-off, with a maximum gate rating of 6 V. This necessitates power supplies driving gate drivers to be designed accordingly. The UVLO of the driver or controller should also align with a 5 V gate drive.

b. **Faster Switching Speed:** Si MOSFETs may have more than 3x $R_{DS(on)} \cdot Q_G$ compared to GaN, and up to 10x higher $R_{DS(on)} \cdot Q_{GD}$ [1]. As a result, a dv/dt of 75 V/ns or higher may be present on the switch node, so gate drivers need to be immune to such slew rates. Faster switching speeds also make parasitic inductances more noticeable, so employing low inductance layout techniques is required in the design.

c. **Higher Reverse Conduction Voltage Drop:** Unlike silicon MOSFETs, eGaN FETs lack a parasitic body diode, but they do conduct current in reverse with a larger voltage drop; ~2.5 V [1] compared to 1 V for MOSFETs, which means the gate driver can see a higher negative switch node voltage during dead-times for the rectifying switch. Therefore, the gate driver should include bootstrap overvoltage management and be capable of operating with negative switch-node voltages down to -5V.

d. **Physical structure:** eGaN FETs have a lateral structure [1], while Si MOSFETs rated > 20 V are typically vertical devices. Consequently, the pin locations may differ, posing layout challenges when using Si MOSFET-specific gate drivers. GaN-specific gate drivers are designed to be layout compatible with most GaN transistors. Layout conflicts when using a MOSFET driver for a GaN FET require an understanding of the trade-offs that can be made in a design.

MOSFET Gate Driver Compatibility Review
Before a MOSFET gate driver can be designed to drive GaN FETs, it must meet certain requirements.

1. **Compatibility with a 5V Supply:** The gate driver must be compatible with a 5 V supply for the driver stage, either from an external regulated supply or an internal Low Dropout Regulator (LDO).

2. **UVLO Compatibility:** Under Voltage Lockout (UVLO) must be compatible with a 5 V driver stage. A typical UVLO for the low side driver stage would be between 3.75 – 4 V and 3.25 - 3.75 V for the high side.

3. **Slew Rate Immunity:** Gate drivers should exhibit slew rate immunity exceeding the maximum expected dv/dt in the switch node, preferably greater than 50 kV/µs. If this requirement cannot be met, the switching speed may need to be reduced at the expense of lower converter efficiency.

4. **Bootstrap Power Supply:** Many MOSFET drivers use a bootstrap circuit to power the upper device driver and most use a bootstrap diode. Only gate drivers that use an external bootstrap diode are suitable for use with GaN FETs as will become apparent in the recommendations. Drivers that include an LDO post the bootstrap diode are the preferred choice.

5. **Dead-time Capability:** The outstanding switching characteristics of eGaN FETs enable operating conditions in the MHz range while maintaining high converter efficiencies. Because of this, minimizing the dead time, even below 10 ns becomes very beneficial. Some controllers designed for MOSFETs will not be capable of such low dead-times thus negating the benefits of GaN devices. When considering controllers for use with GaN FETs, prioritize those with low dead-times capabilities.

Steps to Convert a MOSFET Driver to work with GaN FETs
Once a compatible MOSFET driver has been identified, then the following steps can be implemented to ensure highest compatibility with GaN FETs. Refer to figure 1 for details with the accompanying explanations. *General GaN FET driving recommendations [1] should always be followed in addition to these recommendations.*

1. **Bootstrap Diode:** For an external bootstrap diode, use the smallest possible size, capacitance, and current rating Schottky diode, such as a BAT54KFILM [2], and connect it in series with a current limiting resistor as shown in Figure 1 (a). The Schottky diode ensures the lowest loss in voltage (V_{boot}-V_{sw}) thus maintaining the driver voltage as close to 5 V as possible. The small series resistor limits the current in the bootstrap diode when any of the protection circuits kick in. It should be noted that this resistor may have an impact in the minimum pulse width required to recharge the bootstrap capacitor. Drivers with an integrated 5 V LDO after the bootstrap diode do not require the series resistor or additional circuit protections subsequently presented as those recommendations become optional.

2. **Bootstrap Clamp:** A Zener diode across the bootstrap capacitor may be used to clamp the voltage to below 6 V to prevent over-

voltage during dead-times with the low-side device in reverse conduction. A good example would be MM5Z5V6ST1G [3] with a Zener voltage of 5.6 V as shown in Figure 1 (b). Both the bootstrap capacitor and Zener diode should be placed as close as possible to each other, and as close as possible to the gate driver.

3. **Gate Return Resistor:** Adding a gate return resistor, as shown in Figure 1 (c), for the high side FET can protect the IC from a large negative voltage on the switch node during reverse conduction of the low side GaN FET as shown in Figure 2. The value of this resistor also depends on the turn-off damping and timing needed for the upper device gate circuit. Using this resistor requires an equivalent reduction in the turn-on resistor for the gate to compensate for its resistance.

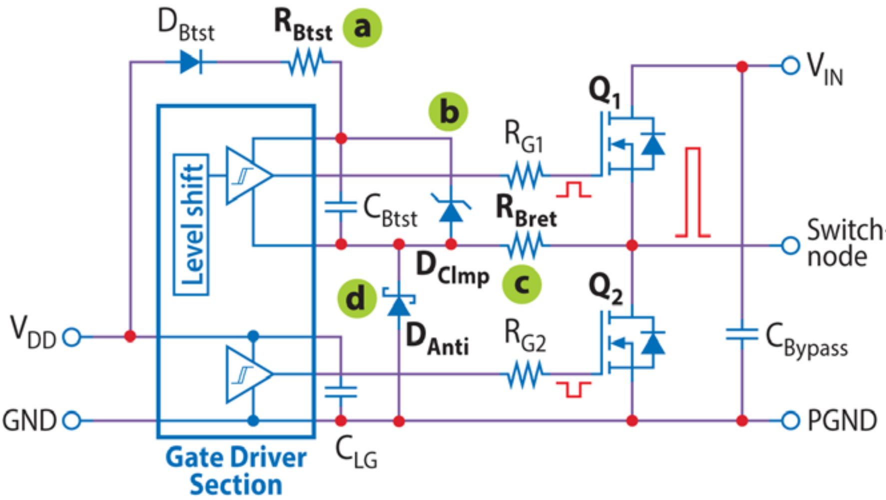

Figure 1: Recommended Si Gate driver augmentation for GaN FET compatibility.

4. **Reverse Conduction Clamp:** An anti-parallel Schottky diode across the low side of a half-bridge topology, as shown in Figure 1 (d), can limit the magnitude of negative switch node voltage the driver is exposed to. Some gate drivers become sensitive to or may even fail when the switch-node falls below certain voltages below the ground reference [4]. The voltage rating of this diode should match that of the low side GaN FET. The current rating can be significantly lower than that of the low side FET because it only conducts during dead times, so it should be selected based on its pulsed current rating.

Working with Controller ICs with Integrated Gate Drivers

Controller ICs integrate many functions into a single IC, including the gate driver [5-7]. Some of these ICs may not allow an optimal layout for GaN devices, so it is important to understand the design compromises that can be made to achieve the best performance.

When designing a power stage using GaN FETs, it is important to always follow the general layout recommendations provided in [8, 9]. The order of consideration remains common-source-inductance (CSI), followed by the power loop and then the gate loop inductance [10]. This means that the power stage is essentially designed as a block and then the gate signals connected to the controller IC as shown in Figure 3. Variations of the recommended layout for the power stage block are given in [11] making it easier to choose an optimal block that can fit the controller IC. In the case of 2-phase controllers, it may be necessary to choose between 2 alternative designs. The design criteria is to prioritize

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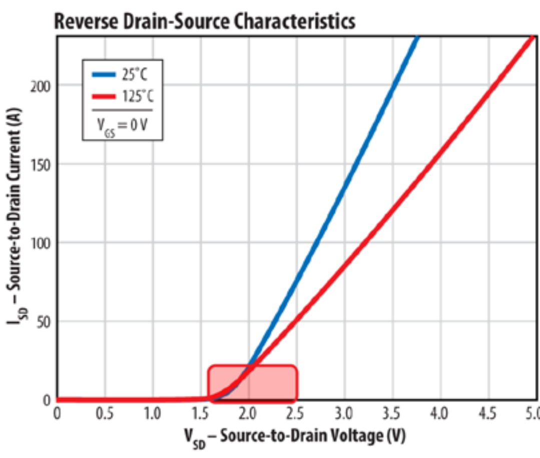
$V_{Btst} = 5\ V – V_{Qlow} \approx 7.5\ V$



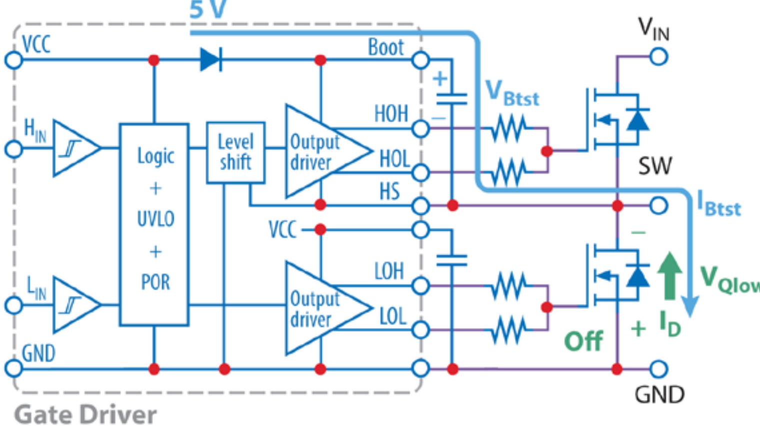


Figure 2: Bootstrap charging path during dead time.

the control FET (switch), which is typically hard switched, over the synchronous rectifier. For example, in a buck converter, the layout should be optimized to minimize parasitic inductance in the gate loop of the high side FET. The same would be true for the low side FET in a boost converter as shown in Figure 3.

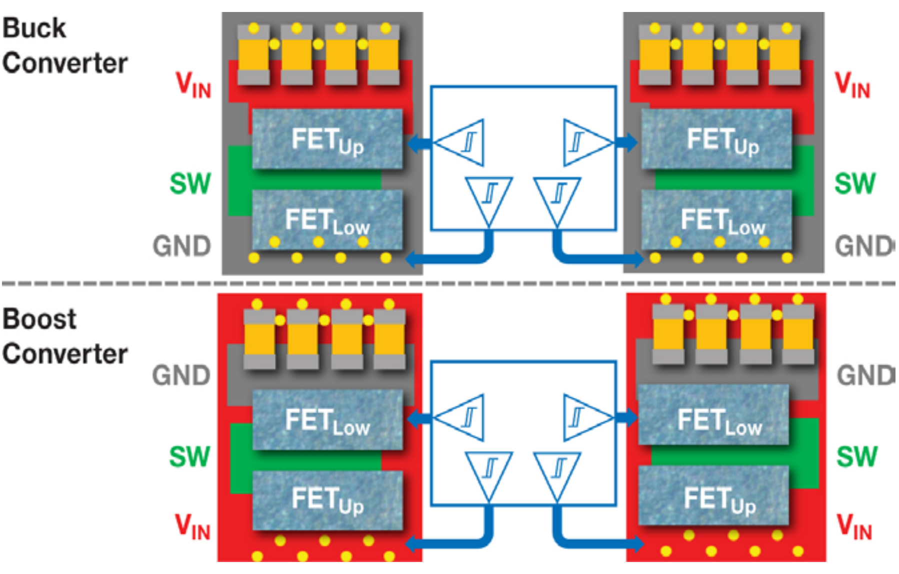


Figure 3: Recommended layouts.

Conclusions

This article presents a method to adapt MOSFET gate drivers for use with GaN FETs. Designers must ensure compatibility, implement recommended modifications, and optimize layouts to harness the full potential of GaN technology. With careful attention to these guidelines, designers can use generic gate drivers and controllers, paving the way for successful high-volume production of GaN-based power converters.

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