EPC GaN Transistor Application Readiness: Phase Two Testing

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Efficient Power Conversion Corporation's (EPC) enhancement mode Gallium Nitride (GaN) power transistors offer performance well beyond the realm of silicon-based MOSFETs. Standard power converter topologies can greatly benefit from the added performance and realize improved efficiency while maintaining the simplicity of older designs.

At the conclusion of Phase Two Testing, EPC's risk-reduction efforts include operating life information for over 760 devices and 739,000 total device hours. All devices were stressed at their maximum operating ratings and subjected to wide variety of stress tests. Phase Two test results reported in this paper confirm the results of our Phase One testing regarding EPC GaN readiness for commercial use.

PHASE ONE SUMMARY

In Phase One Reliability Testing 380 EPC devices were stressed for a total of 275,000 device hours under conditions similar to power MOSFET reliability testing including:

- Long term stability under high drain-source bias was evaluated by subjecting devices to a DC voltage equal to the maximum rated voltage at the maximum rated temperature (high temperature reverse bias, or HTRB).
- Gate reliability was evaluated by subjecting devices to various gate stresses at the maximum rated temperature (high temperature gate bias, or HTGB).
- Environmental reliability was evaluated with temperature cycling (TC) and
- Temperature-humidity-with-bias (THB).
- Operating life was evaluated by building parts onto power supply boards and subjecting parts to operating conditions over extended period of time.

"Dynamic $R_{DS(on)}$," specifically those conditions causing minimal shifting in device resistance, was also a focus of the EPC Phase One reliability program. EPC's devices have been designed to mitigate dynamic $R_{DS(on)}$, and data show significantly greater stability than devices reported in the literature.

Phase One test results were included in EPC GaN Transistor Application Readiness: Phase One Testing published in March of 2010[1].

RELIABILITY PROGRAM OVERVIEW – PHASE TWO TESTING

In Phase Two, an additional 380 devices, including 200 V devices, were stressed at their maximum operating ratings and subjected to HTRB, HTGB, TC and THB. Phase Two testing also included human body method (HBM) and machine model (MM) electrostatic discharge (ESD) testing. Selected devices were tested to evaluate the addition of underfill material for applications where an underfill option is being considered. In addition, Phase One devices continued stress testing beyond 1000 hours. An additional 464,000 total device hours were recorded in Phase Two bringing the total device hours under stress at maximum operating ratings for EPC GaN to 739,000 hours.

EPC's product offering is listed in Appendix I, in which the voltage rating, $R_{DS(on)}$ max, and package dimension of these parts are shown. A list of the reliability tests performed in both Phase One and Phase Two, the applicable standards, the device types evaluated, and the stress conditions are shown in Appendix II. The added tests in Phase Two and the extended tests from Phase One are indicated in bold font for the part numbers in the table. Appendix III shows all the stress test results in tabular form.

All devices tested were soldered onto FR408 printed circuit boards. The under-fill material used in the tests indicated was Loctite FP4549Si.

RELIABILITY TESTING RESULTS – PHASE TWO TESTING

High Temperature Reverse Bias (HTRB)

200 V rated products were added in Phase Two for high temperature reverse bias test, complementing the tests done on 40 V and 100 V in Phase One. EPC1012 (200 V 100 mΩ) parts were drain biased to the full rated voltage at 125°C, and EPC1010 (200 V 25 mΩ) parts were drain biased to the full rated voltage at 150°C. An underfill option was evaluated as well.

There were no parametric failures out of the 150 high voltage devices tested, and all electric parameters remained relatively constant throughout the entire stress period of 1000 hours for all three tests. EPC1010 devices on HTRB have continued beyond 1000 hours and passed 1336 hours at the time of this writing. Appendix V graphically presents the stability of various device parameters during test.

High Temperature Gate Bias (HTGB)

The gate stress test of EPC1001 at 5 V and 5.4 V completed 1000 hours in Phase One, and was continued in Phase Two for extended hours. At the time of this writing parts from these two tests have completed 2000 hours. All electric parameters remained relatively constant throughout the entire stress. Appendix VI graphically presents the stability of various device parameters during test. Gate stress at 6 V is under further evaluation. Results will be reported in Phase Three.

Gate performance at a higher temperature was evaluated in Phase Two. EPC1010 devices were gate biased at 5 V_{GS} at 150°C, a temperature above the rated temperature of 125°C. Devices have successfully passed 1000 hours at this stress condition, proving the device capability at 150°C. All electric parameters remained relatively constant throughout the stress period. The stability of various device parameters during test is shown in Appendix VI.

EPC1001 parts were also gate stressed at a negative voltage relative to the source. Device gates were biased at negative 5 V_{GS} at 125°C for a period of 1000 hours. All device electric parameters remained relatively constant throughout the entire stress period. The stability of various device parameters during test is presented in Appendix VI together with the other gate bias results.

Temperature Cycling (TC)

Temperature cycling was conducted in Phase One on EPC1001 (100 V 7 mΩ) and EPC1014 (40 V, 16 mΩ). EPC1001 is a large device and EPC 1014 is a small device. In Phase Two, EPC1012 (200 V, 100 mΩ) parts were added. EPC1012 is similar in size to EPC1014, but has wider bump spacing and a smaller gate bump[2]. EPC1012 parts with underfill were also evaluated.

Parts were all mounted on FR408 printed circuit board. The underfill material used was Loctite FP4549Si. Temperatures varied between -40°C to 125°C at a rate of two cycles per hour with 10 minutes soaking at the max and min temperatures. No resistance degradation was observed over the stress period of 1000 cycles and all other electrical parameters remained constant during stress. Complete test results of the parameters during test are shown in Appendix VII.

Temperature-Humidity with Bias (THB)

EPC1014 (40 V, 16 mΩ) continued on THB in Phase Two and completed 1000 hours. EPC1015 (40 V, 4 mΩ), a large 40 V device, was also evaluated in Phase Two and successfully completed 1000 hours. All device electric parameters remained relatively constant over the entire stress period. Complete test results of the parameters during test are shown in Appendix VIII.

Electrostatic Discharge Human Body Model (HBM) and Machine Model (MM)

Electrostatic Discharge (ESD) tests were done in Phase Two, evaluating the device capability under the Human Body Model (HBM) and Machine Model (MM).

ESD tests were conducted on EPC1014 and EPC1015. EPC1014 is a small size device and EPC1015 is a large device representing the typical small and large device sizes of EPC's product offerings shown in Appendix I. Both HBM and MM were conducted on these two devices. JEDEC JESD22-A114F was followed for the HBM, and EIA/JESE22-A115-A was followed for the MM.

The source-drain was shown to have high ESD handling capability. On HBM, both EPC1014 and EPC1015 exceeded ±4000 V without fail, making both of them Class 3A (or higher) capable drain-source. On MM both EPC1014 and EPC1015 have passed ±400 V, making them Class C capable drain-source.

Due to the extremely low input capacitance of EPC's transistors, the gates are quite ESD sensitive. Both EPC1014 and EPC1015 gate-source were Class 1A rated on HBM and Class A rated on MM. EPC1015 gate-drain passed ±500 V, making it Class 1B capable on HBM, and passed ±200 V, making it Class B capable on MM. EPC1014 gate-drain was Class 1A rated on HBM and Class A rated on MM.

The test results of each of the above ESD tests can be found in the ESD Results Table in Appendix IV.

FUTURE WORK

In Phase Three, EPC will develop acceleration factors and models that allow users to determine suitability for various applications beyond basic commercial use. EPC will also extend the number of devices, types of devices, and number of stress hours (or cycles).

EPC will convert to lead free solder late in 2010. This conversion will be accompanied by additional testing at 150oC to verify this change does not degrade device characteristics under stress. At that time, EPC will also conduct more extensive tests to evaluate the performance and reliability of surface mount solder attachments.

References

1. Y. Ma, "EPC GaN Transistor Application Readiness: Phase One Testing," http://www.epc-co.com/Tools and Design Support/Product-Training
2. A. Nakata, E. Abdoulin, J. Cao, and Y. Ma, "Assembling EPC GaN Transistors," http://www.epc-co.com/Tools and Design Support/Product-Training

Appendix

Appendix I: Product Matrix Table

Part Number	Voltage Rating (V)	$R_{DS(on)}$ Max (mΩ)	Package Dimensions (mm x mm)
EPC1014	40	16	LGA 1.7 x 1.1
EPC1015	40	4	LGA 4.1 x 1.6
EPC1009	60	30	LGA 1.7 x 1.1
EPC1005	60	7	LGA 4.1 x 1.6
EPC1007	100	30	LGA 1.7 x 1.1
EPC1001	100	7	LGA 4.1 x 1.6
EPC1013	150	100	LGA 1.7 x 0.9
EPC1011	150	25	LGA 3.6 x 1.6
EPC1012	200	100	LGA 1.7 x 0.9
EPC1010	200	25	LGA 3.6 x 1.6

Appendix II: Reliability Test Table

Reliability Stress Test	Applicable Standard	Product	Stress Conditions
High Temperature Reverse Bias (HTRB)	JEDEC Std JESD22-A108	EPC1001, EPC1014, **EPC1012, EPC1010, EPC1010 with underfill**	100% rated break-down drain bias, 125°C
High Temperature Gate Bias (HTGB)	JEDEC Std JESD22-A108	**EPC1001**	5 V gate bias, 125°C
		EPC1010	5 V gate bias, 125°C
		EPC1001	5.4 V gate bias, 125°C
		EPC1001	6 V gate bias, 125°C
		EPC1001	-5 V gate bias, 125°C
Temperature Cycling (TC)	JEDEC Std JESD22-A104	EPC1001, EPC1014, **EPC1012, EPC1012 with underfill**	-40°C to 125˚C, 2 cycles per hour
Temperature Humidity Bias (THB)	JEDEC Std JESD22-A101	**EPC1014, EPC1015**	85˚C/85 RH, rated drain bias or max 100 V drain bias
Power Supply Operating Life		EPC1001	10 A, 250 kHz, 30°C
ESD Human Body Model (HBM)	JEDEC Std JESD22-A114F	**EPC1014, EPC1015**	
ESD Machine Model (MM)	EIA/JEDEC Std EIA/ JESD22-A1115-A	**EPC1014, EPC1015**	

BOLD = Part numbers in Phase Two Test

Appendix III: Reliability Results Table

Stress Test	Test Condition	Part Number	Sample Size	# of Fail at Read Point					
				168 HR	500 HR	1000 HR	1366 HR	1672 HR	2000 HR
HTRB	100 V drain bias, 125°C	EPC1001	45	0	0	0	–	–	–
HTRB	40 V drain bias, 125°C	EPC1014	50	0	0	0	–	–	–
HTRB	200 V drain bias, 125°C	EPC1012	50	0	0	0	–	–	–
HTRB	200 V drain bias, 125°C	EPC1010 with underfill	50	0	0	0	–	–	–
HTRB	200 V drain bias, 150°C	EPC1010	50	0	0	0	0	–	–
Stress Test	**Test Condition**	**Part Number**	**Sample Size**	**# of Fail at Read Point**					
				168 HR	500 HR	1000 HR	1366 HR	1672 HR	2000 HR
HTGB 5 V	5 V gate bias, 125°C	EPC1001	45	0	0	0	–	–	0
HTGB 5 V	5 V gate bias, 150°C	EPC1010	45	0	0	0	–	–	–
HTGB 5.4 V	5.4 V gate bias, 125°C	EPC1001	45	0	0	0	0	0	0
HTGB 6 V	6 V gate bias, 125°C	EPC1001	50	–	–	–	–	–	–
HTGB -5 V	-5 V gate bias, 125°C	EPC1001	50	5*	0	0	–	–	–
Stress Test	**Test Condition**	**Part Number**	**Sample Size**	**# of Fail at Read Point**					
				168 HR	500 HR	1000 HR	1366 HR	1672 HR	2000 HR
TC	-40°C to 125˚C	EPC1001	45	0	0	0	–	–	–
		EPC1014	50	0	0	0	–	–	–
		EPC1012	45	0	0	0	–	–	–
		EPC1012 with underfill	45	0	0	0	–	–	–
Stress Test	**Test Condition**	**Part Number**	**Sample Size**	**# of Fail at Read Point**					
				168 HR	500 HR	1000 HR	1366 HR	1672 HR	2000 HR
THB	85˚C/85 RH, 40 V	EPC1014	45	0	0	0	–	–	–
		EPC1015	45	0	0	0	–	–	–
Stress Test	**Test Condition**	**Part Number**	**Sample Size**	**# of Fail at Read Point**					
				168 HR	500 HR	1000 HR	1200 HR		
Power Supply Life Test	10 A, 250 kHz, 30°C	EPC1001	10	0	0	0	0	–	–

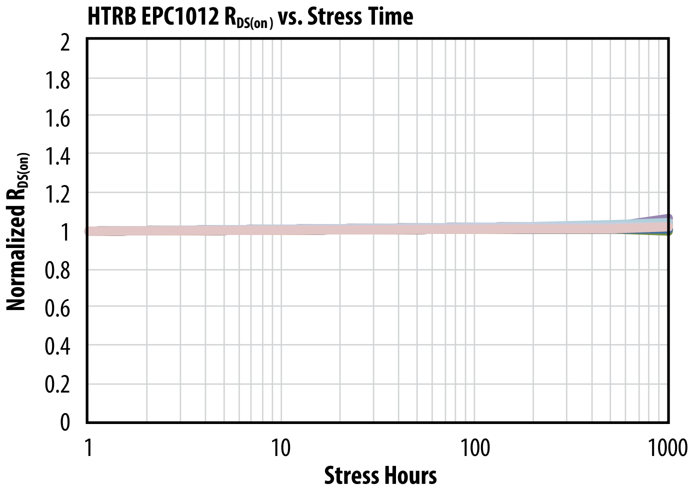
*See comments in the main text - reliability testing results

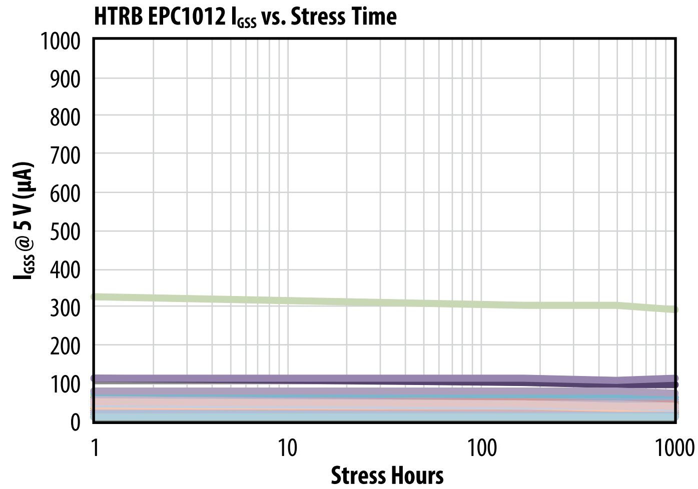
Appendix IV: ESD Results Table

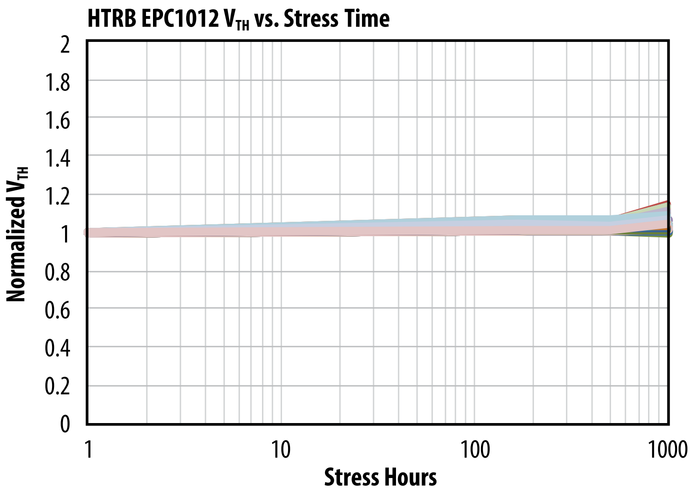
Pin-Pin (+/–)	EPC1015 HBM	EPC1014 HBM	EPC1015 MM	EPC1014 MM
G-S (+)	CLASS 1A	CLASS 1A	CLASS A	CLASS A
G-S (–)	CLASS 1A	CLASS 1A	CLASS A	CLASS A
G-D (+)	CLASS 1B	CLASS 1A	CLASS B	CLASS A
G-D (–)	CLASS 1B	CLASS 1A	CLASS B	CLASS A
S-D (+)	> CLASS 3A	> CLASS 3A	CLASS C	CLASS C
S-D (–)	> CLASS 3A	> CLASS 3A	CLASS C	CLASS C

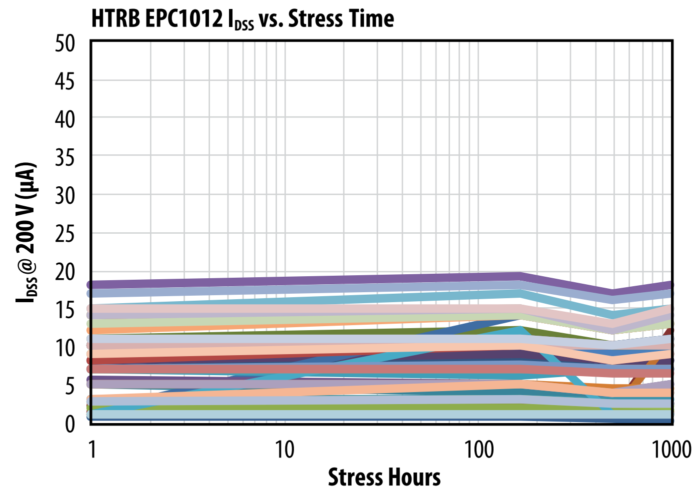
Appendix V: HTRB Results

EPC1012 HTRB 200 V at 125°C



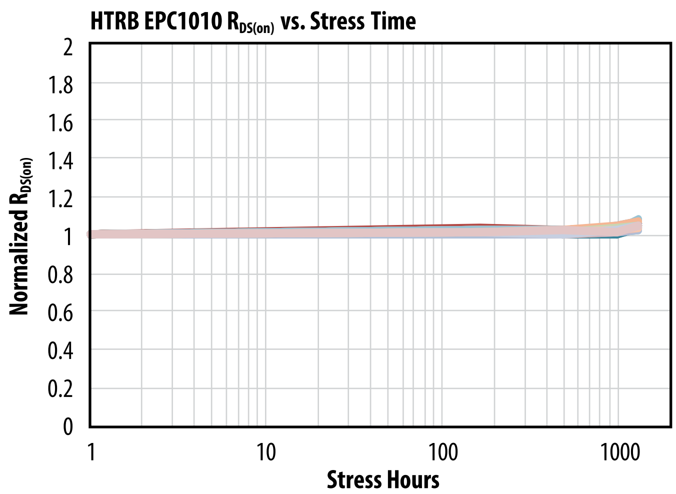


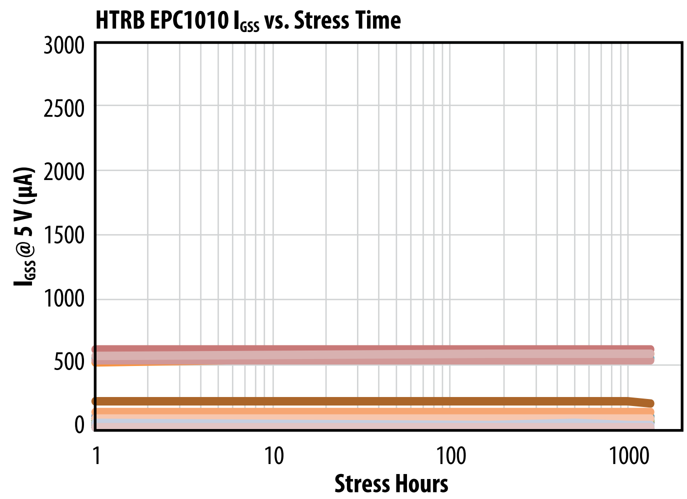


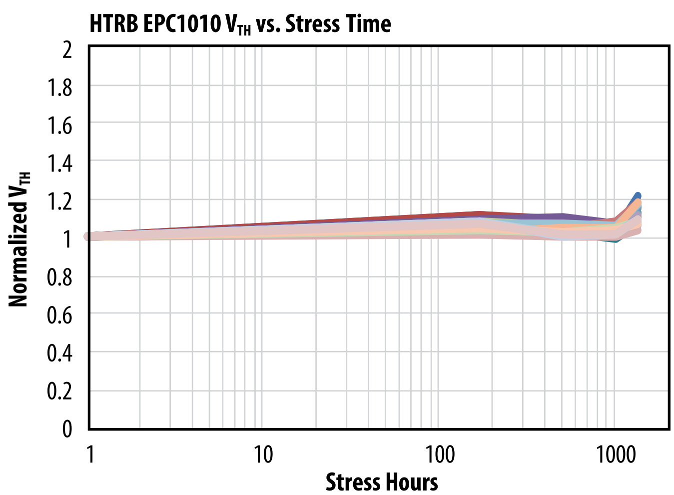


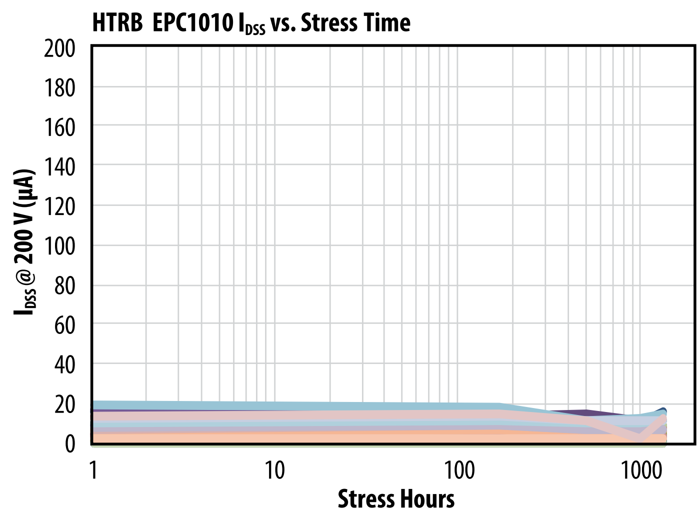
Appendix V: HTRB Results

EPC1010 HTRB 200 V at 150°C



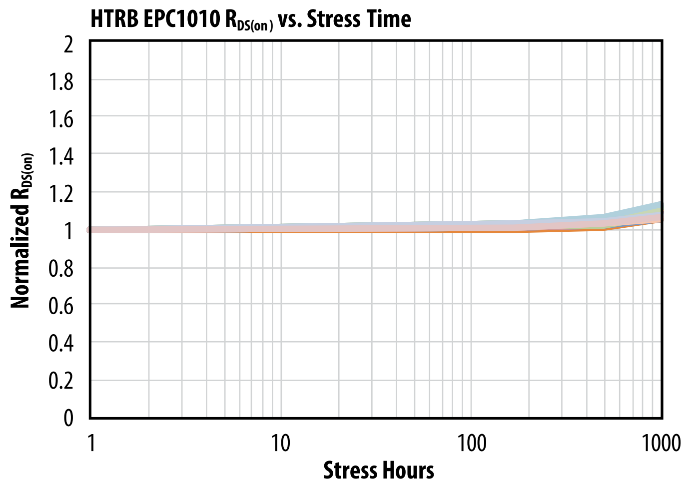


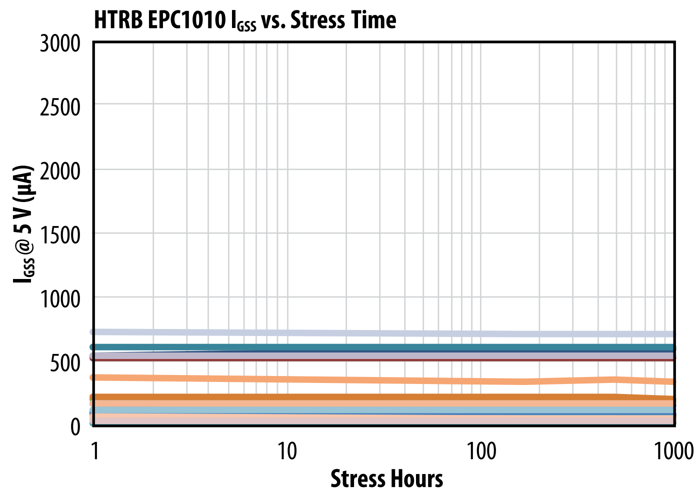


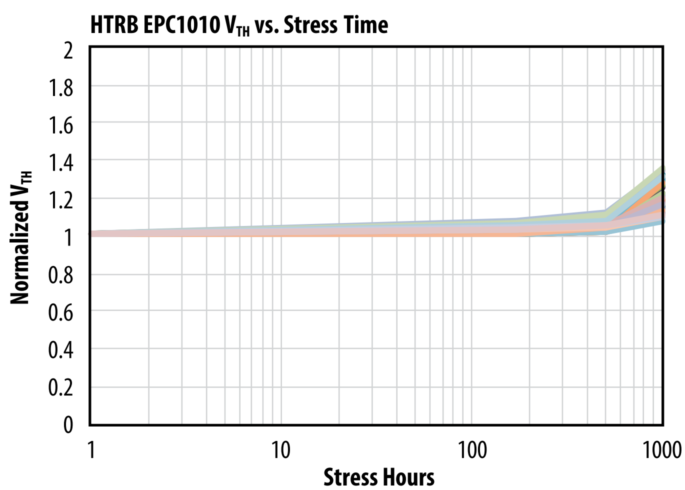


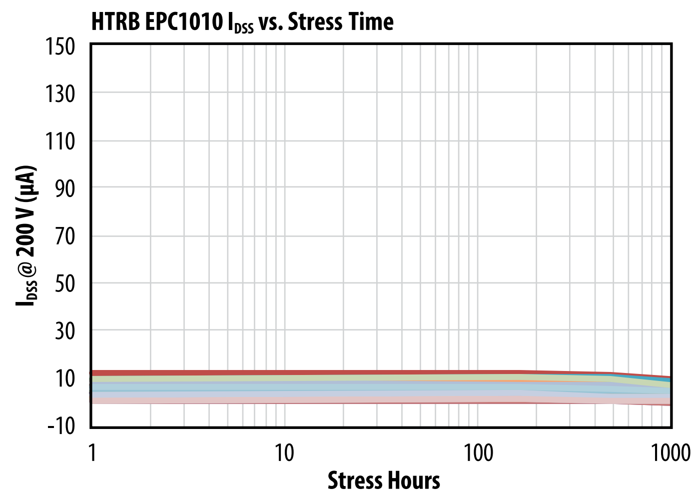
Appendix V: HTRB Results

EPC1010 with Underfill HTRB 200 V at 125°C



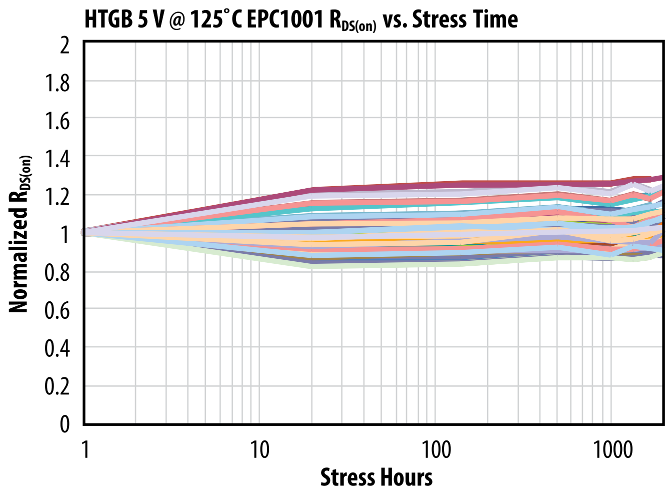


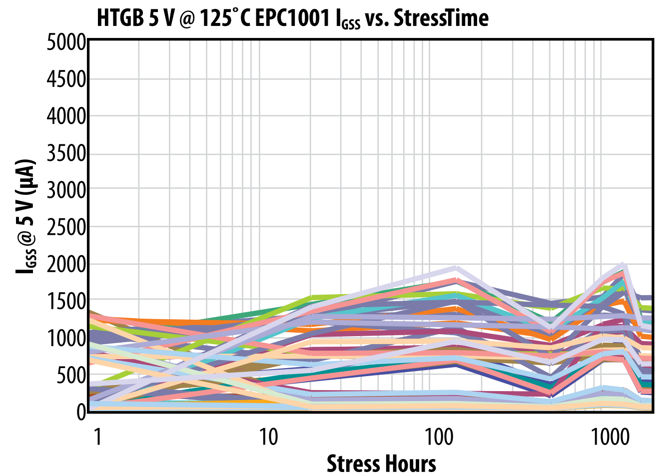


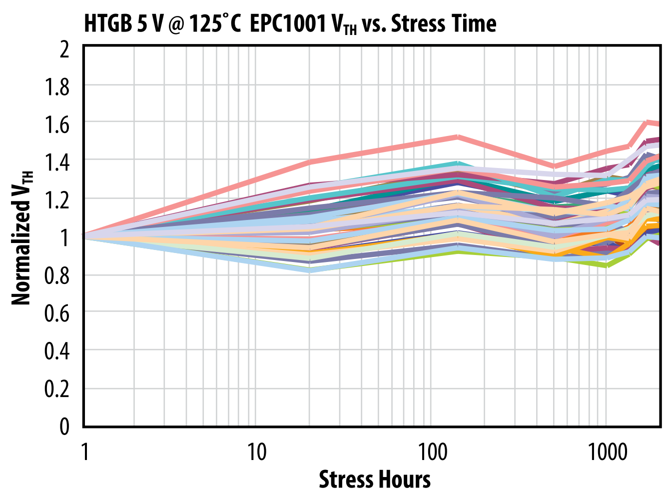


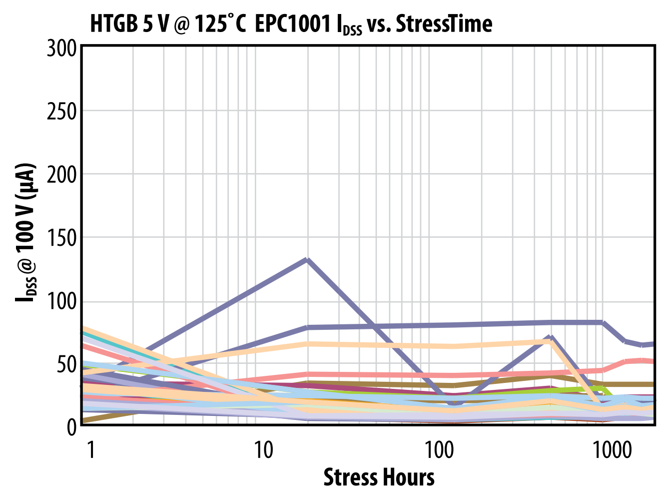
Appendix VI: HTGB Results

EPC1001 HTGB 5 V at 125°C



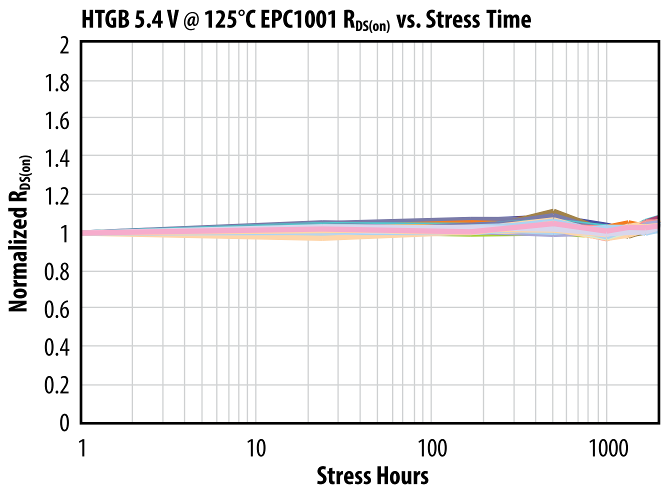


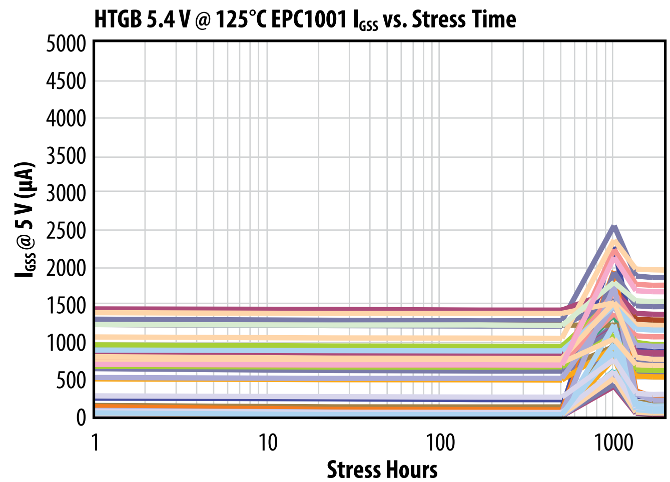


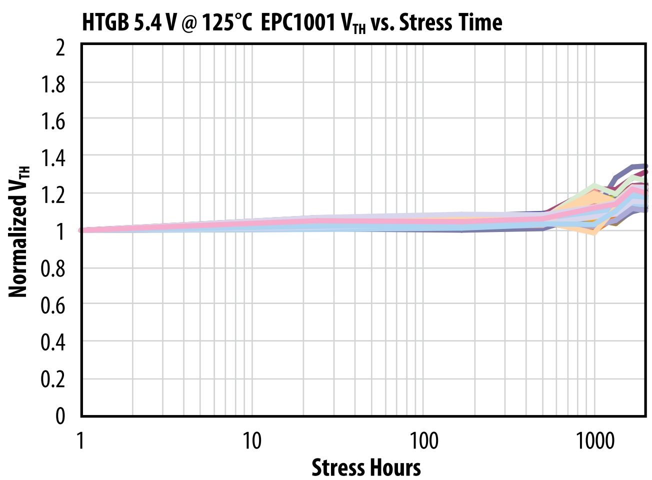


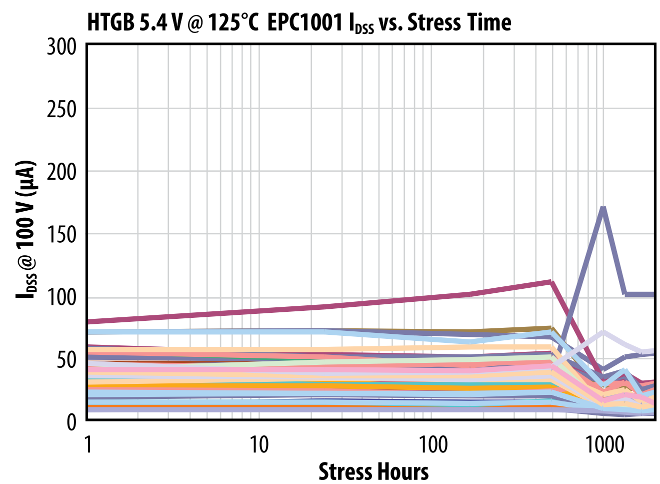
Appendix VI: HTGB Results

EPC1001 HTGB 5.4 V at 125°C



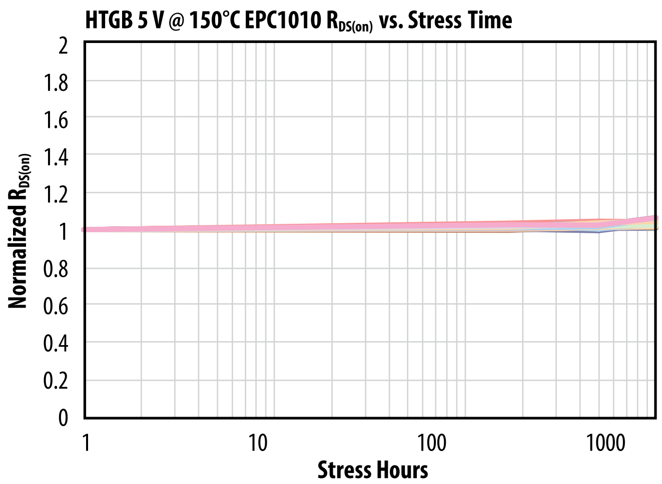


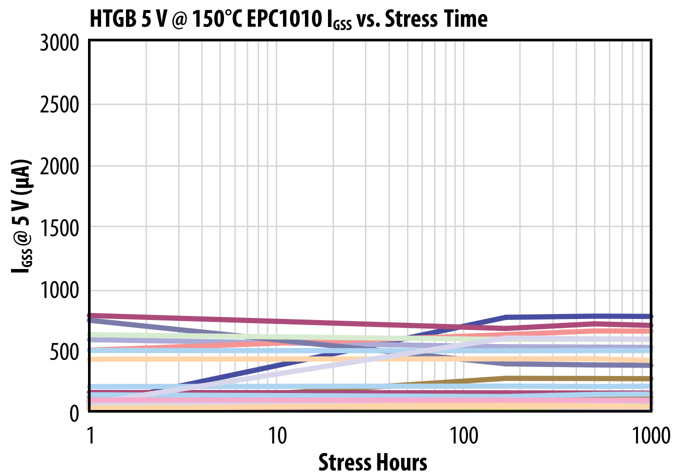


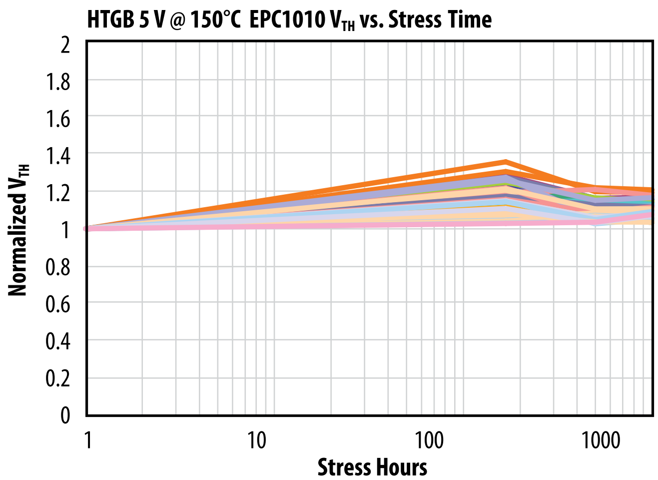


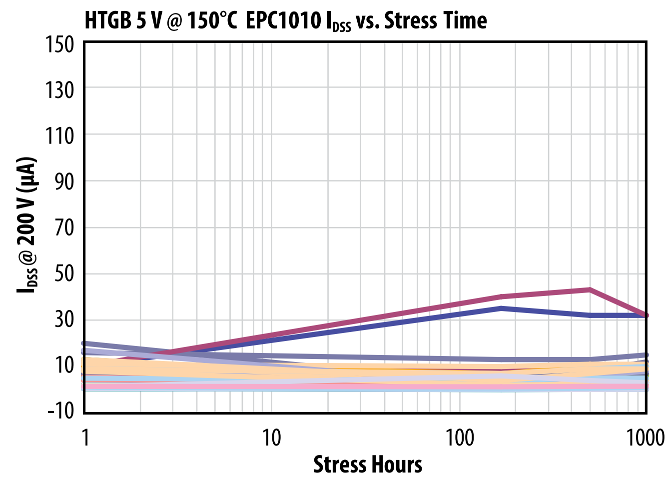
Appendix VI: HTGB Results

EPC1010 HTGB 5 V at 150°C



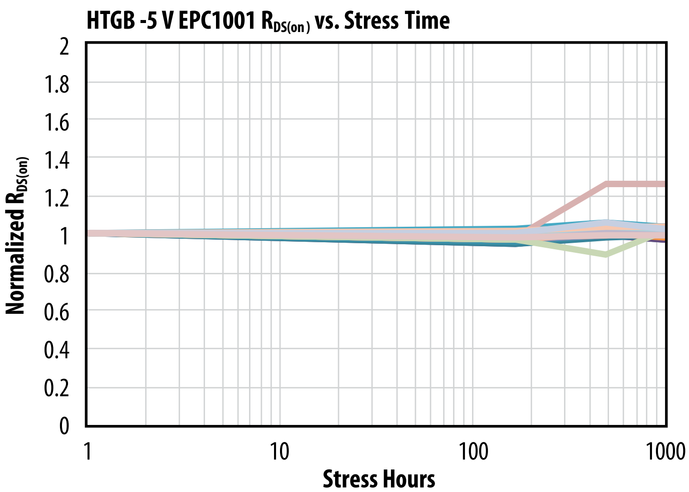


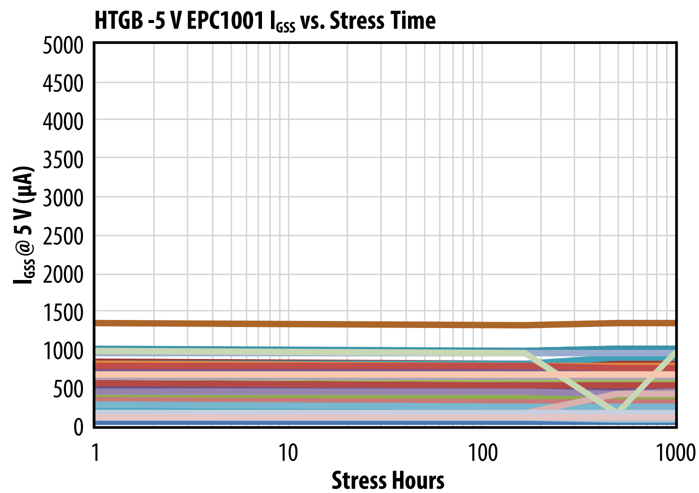


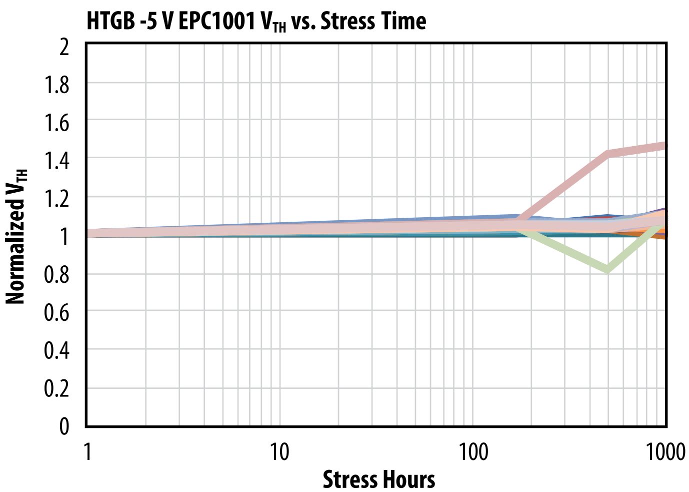


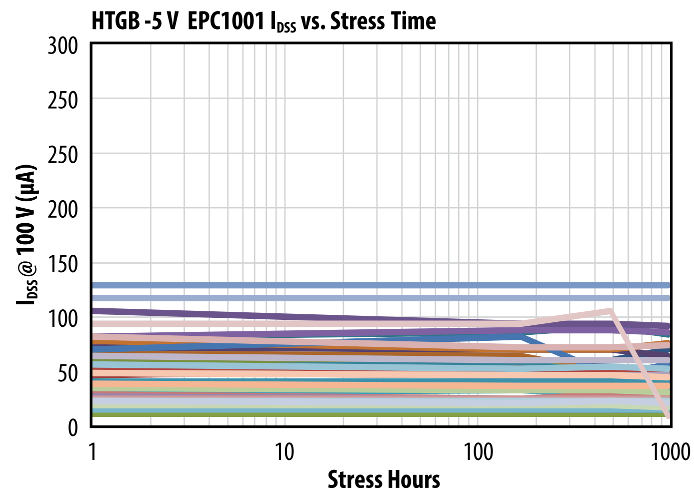
Appendix VI: HTGB Results

EPC1001 HTGB -5 V at 125°C



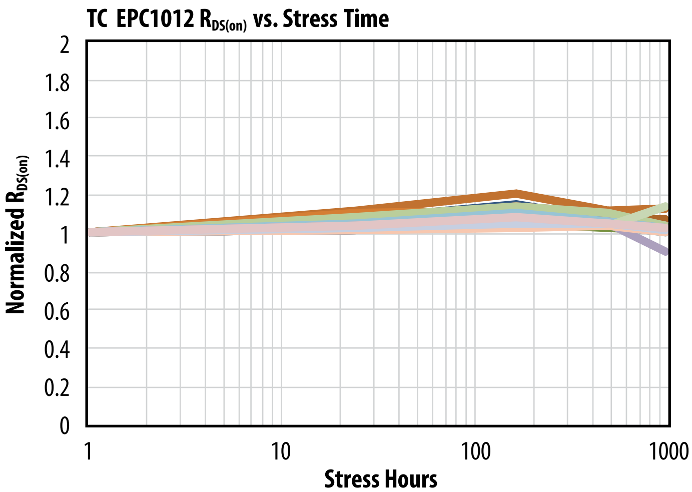


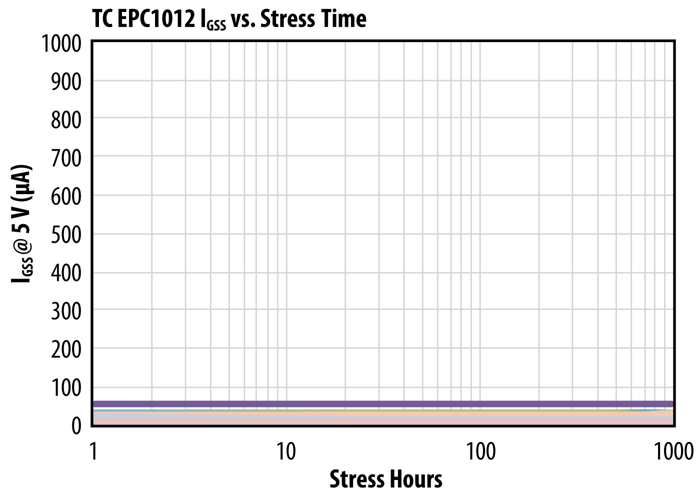


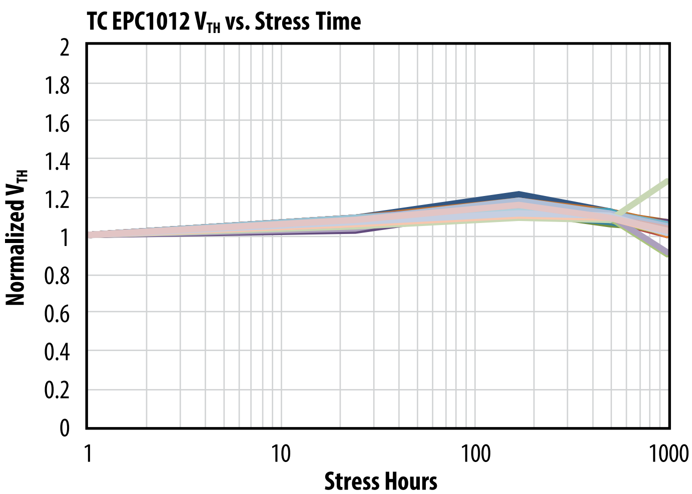


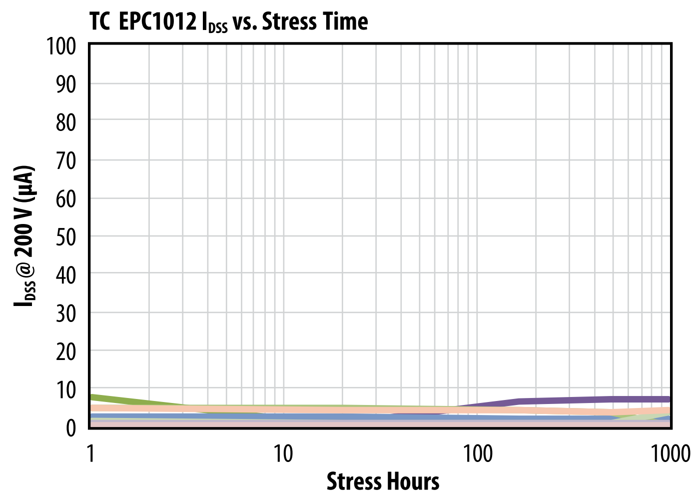
Appendix VII: Temperature Cycling -40˚C to 125˚C

EPC1012



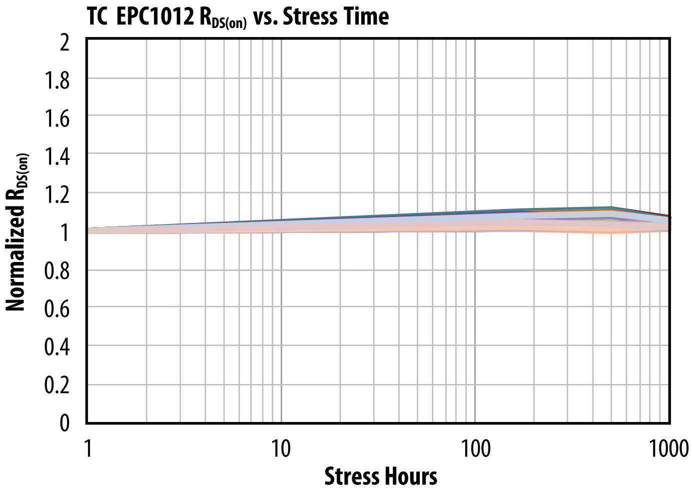


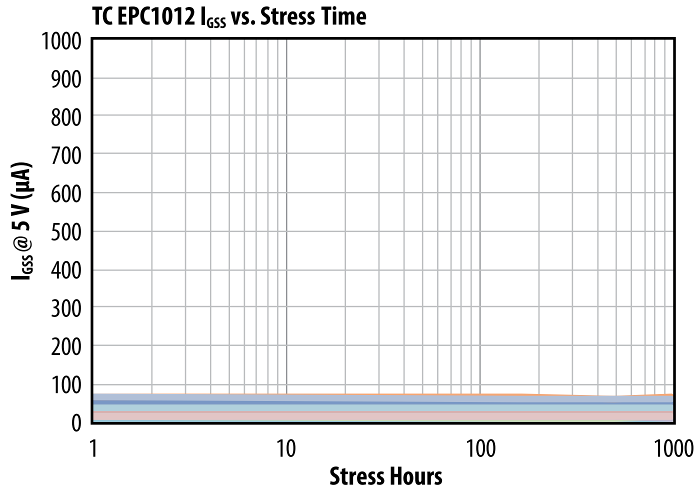


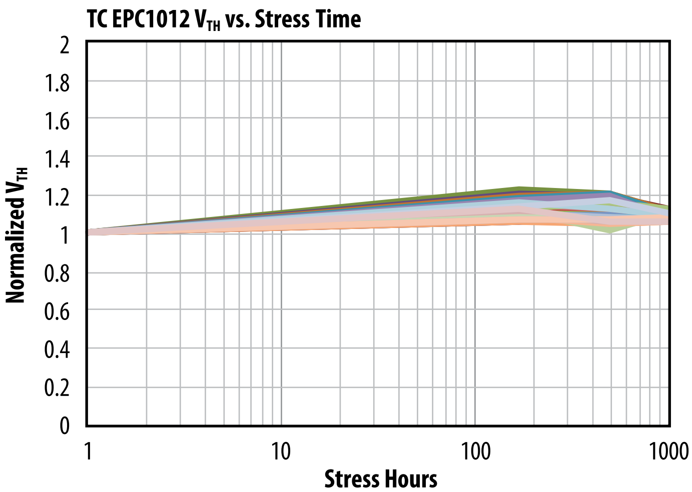


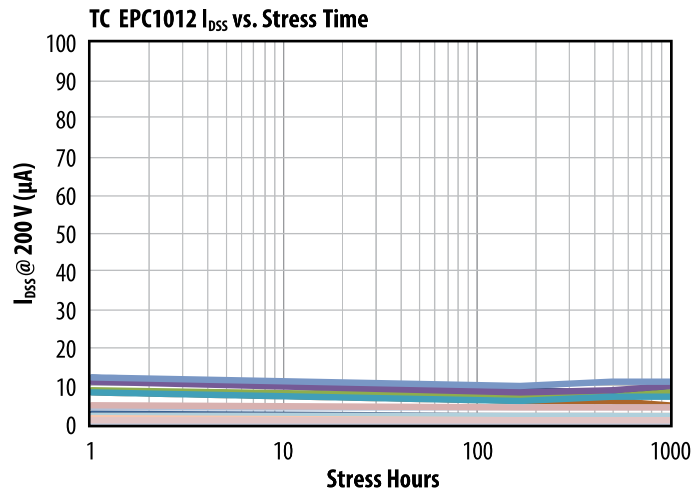
Appendix VII: Temperature Cycling -40°C to 125°C

EPC1012 with Underfill





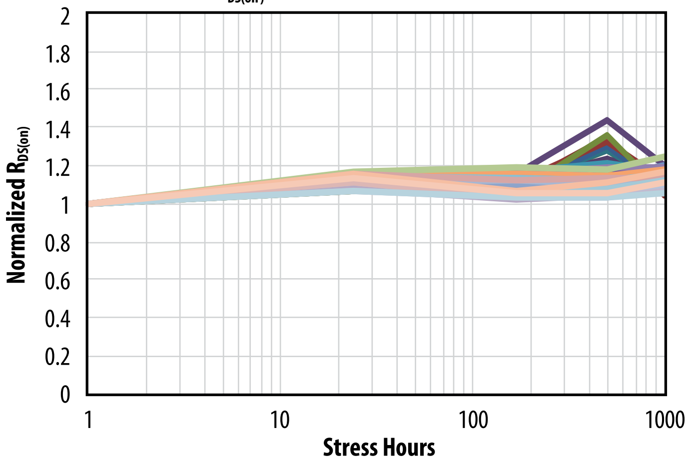




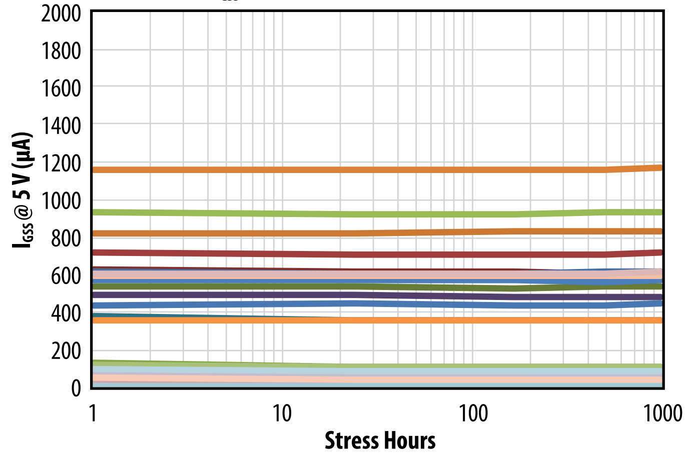
Appendix VIII: THB 85°C / 85% RH

EPC1014

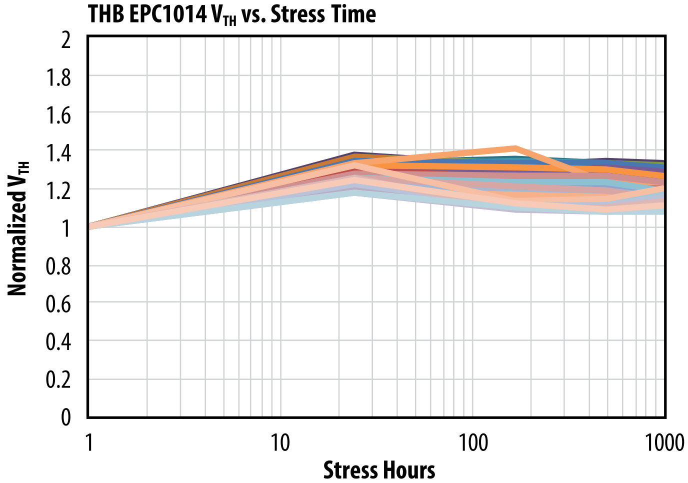
THB EPC1014 $R_{DS(on)}$ vs. Stress Time



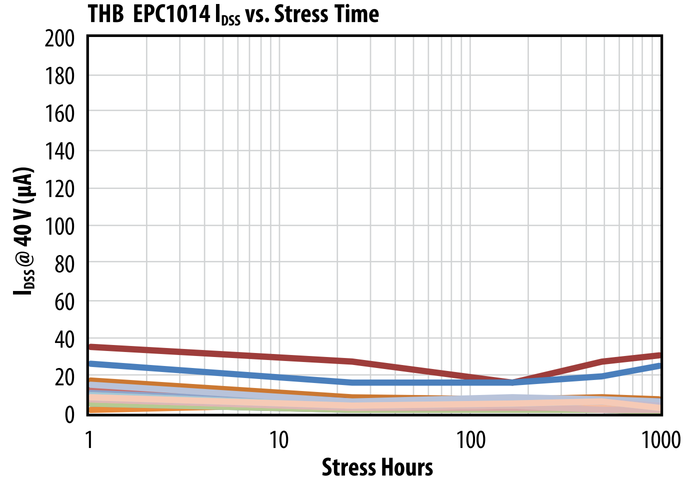
THB EPC1014 I_{GSS} vs. Stress Time



THB EPC1014 V_{TH} vs. Stress Time



THB EPC1014 I_{DSS} vs. Stress Time



Appendix VIII: THB 85°C / 85%RH

EPC1015