

# Envelope Tracking Power Supply for Cell Phone Base Stations Using eGaN® FETs



Yuanzhe Zhang, Ph.D., Michael de Rooij, Ph.D., Efficient Power Conversion

*In this application note, an envelope tracking (ET) power supply using EPC8010 high frequency eGaN FETs for LTE wireless base station infrastructure is presented. The ET power supply is based on a multi-phase, zero-voltage switching (ZVS) synchronous buck converter. It offers 20 MHz large signal bandwidth, delivering over 120 W average load power sourced from 70 V. 94% average total efficiency is achieved when tracking a 20 MHz LTE envelope with a 7 dB peak-to-average power ratio (PAPR).*

## Introduction

Modern communication systems demand high data capacity and high speed. The long-term evolution (LTE) standard for the fourth-generation (4G) and the fifth-generation (5G) wireless systems requires signals with higher PAPR compared with prior generations. This increase reduces the efficiency of the power amplifier (PA). Envelope tracking, or supply modulation, uses a dynamic power supply to vary the PA supply voltage in accordance with the time-varying envelope of the input signal so that the efficiency of the PA is maximized.

## High Frequency GaN Transistors

To meet the requirements for ET power supplies, devices must operate efficiently at very high frequencies. This requires a device with an excellent hard-switching figure of merit, and also layout and package characteristics that maximize in-circuit performance. Such devices, the EPC8000 series, are available as wafer level chip scaled packaged (WLSLP) GaN transistors with the device pin-out show in Figure 1.

## Multi-Phase Topology with Soft-Switching

A four-phase synchronous buck pulse-width modulated (PWM) topology is selected, as shown in figure 2. The power switches are EPC8010 eGaN FETs. The PWM control signals for adjacent phases are phase-shifted by 90 degrees. Switching at 25 MHz in each phase gives the full converter an effective output switching frequency of 100 MHz. A resistive load is used to represent the radio-frequency power

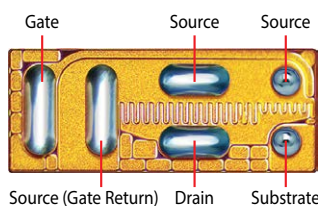


Figure 1: The bump side with pin-out locations of the EPC8000 GaN transistor series

amplifier (RFPA), and a fourth-order filter with 20 MHz band width that supports zero-voltage switching is designed, allowing high efficiency operation and automatic phase current balancing [2]. The printed circuit board (PCB) layout is optimized according to the design practices in [3].

## High Speed Gate Driver

Design of the gate driver that supports switching at high frequency is very challenging, particularly for the high-side FET in the half-bridge configuration. Traditional bootstrap half-bridge gate drivers (LM5113 [4], for instance), designed for higher current, lower frequency applications, generally have high loss due to the reverse recovery charge of the bootstrap diode. As a result, the maximum switching frequency is limited. To achieve 25 MHz switching

frequency while maintaining high efficiency, a synchronous FET bootstrap supply [5] is used.

In [5], a way to use LM5113 at high frequency is introduced, with proper circuitry to disable its internal bootstrap diode. In this application, however, a different approach is implemented. As shown in figure 3, digital isolators ISO721MD and ultra-high-speed logic gates SN74LVC2G14 are used instead of the LM5113. The EPC2038, with the smallest electrical and physical footprint is selected as the synchronous bootstrap FET ( $Q_{BST}$ ) for minimal parasitics and associated losses. The low side FET driver consists of the same component as the high side for matched propagation delay.

## Static Efficiency Measurement

The ET supply is evaluated at steady-state operating points. The measured efficiency of the converter at different output voltages is shown in figure 4. Power stage efficiency only includes losses in the FETs and output filter. Total efficiency includes gate drive losses. The probability distribution function (PDF) of a 20 MHz 7 dB PAPR LTE envelope signal is also shown. The peak power stage and total average efficiencies measured under static condition are 96.2% and 95.8%, respectively, at 234 W output power and 41 V.

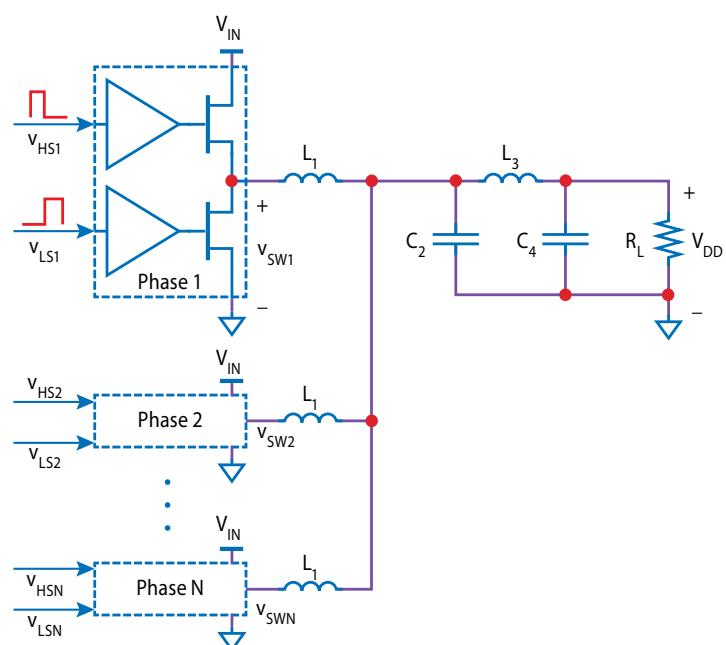


Figure 2: Diagram of an N-phase synchronous buck converter with fourth-order output filter

### Dynamic ET Measurement

The 20 MHz LTE envelope signal is converted into eight PWM signals, for controlling the high side and low side FETs in four phases. Appropriate dead times to achieve ZVS operation are also implemented at this stage. The PWM signals are stored in the memories of an Altera® Arria® V FPGA and transmitted to the gate drivers. The resolution of the pulse width is around 0.2 ns, allowing fine adjustment of duty cycles and dead times for high fidelity ET performance.

The output of the ET supply is measured with a 1 GHz passive probe (TPP1000). A comparison of the measured and target envelope waveforms for a 2  $\mu$ s duration is shown in figure 5, demonstrating accurate tracking and low output voltage ripple. The average output power is 130 W and the peak value is 680 W, corresponding to 7 dB PAPR. Average power-stage efficiency and total efficiency are 95.0% and 94.3%, respectively. Accurate tracking is achieved with the normalized root-mean square error (NRMSE) of only 1.5%. The measured maximum current slew rate is 150 A/ $\mu$ s.

### Summary

eGaN FETs and integrated circuits are helping to achieve very high switching frequency in switched mode power supplies, leading to breakthroughs in a large number of applications where bandwidth, slew rate and efficiency are critical. Envelope tracking is one of them.

Due to lower input and output capacitances ( $C_{ISS}$  and  $C_{OSS}$ ) and lower gate charge (QG) [6], GaN-based switching converters are able to operate at tens of megahertz switching frequency with high efficiency. With topologies such as multi-phase and multi-level, GaN switching converters can achieve high bandwidth that meets the requirement of modern wireless communication standards, such as 4G and 5G.

An ET power supply with four-phase soft-switching buck converter using **EPC8010** can accurately track a 20 MHz 7 dB PAPR LTE envelope signal with greater than 94% total efficiency, delivering 130 W average power. The design is also scalable to satisfy different power.

### References:

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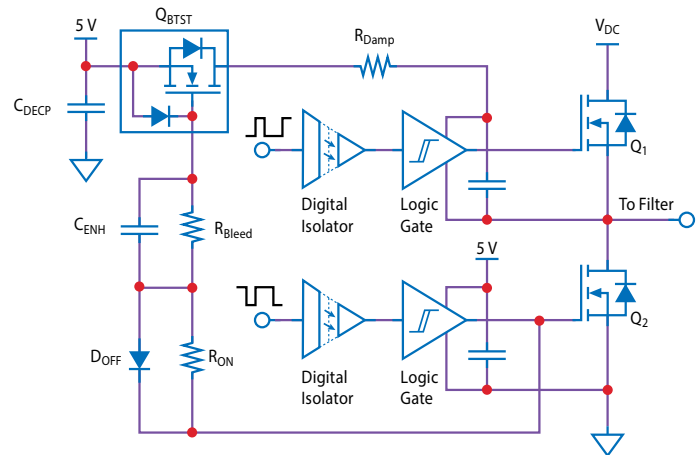


Figure 3: Schematic diagram of the gate drive circuit with synchronous FET bootstrap supply, for one phase of the system converter

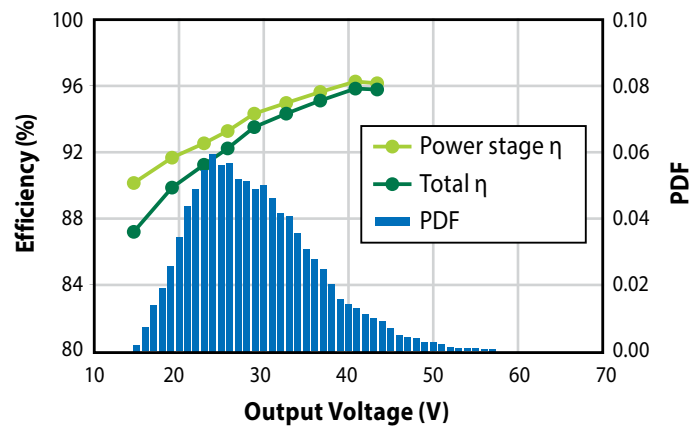


Figure 4: Measured efficiencies of the converter at fixed output voltages and the PDF of the 20 MHz LTE envelope signal

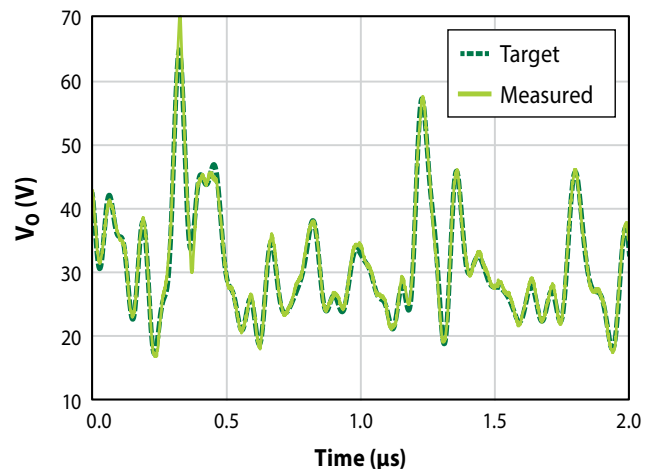


Figure 5: Comparison of target and measured 20 MHz LTE envelope signal