How to Design an eGaN® FET-Based Power Stage with an Optimal Layout

Motivation

eGaN FETs are capable of switching much faster than Si MOSFETs, requiring more careful consideration of PCB layout design to minimize parasitic inductances. Parasitic inductances cause higher overshoot voltages and slower switching transitions. This application note reviews the key steps to design an optimal power stage layout with eGaN FETs, to avoid these unwanted effects and maximize the converter performance.

Impact of parasitic inductance on switching behavior

As shown in figure 1, three parasitic inductances can limit switching performance 1) power loop inductance (L_{loop}), 2) gate loop inductance (L_g), and 3) common-source inductance (L_s). The chip-scale package of eGaN FETs eliminates any significant inductance within the transistor itself, leaving the printed circuit board (PCB) as the main contributor. Each parasitic inductance is a consequence of the total area encompassed by the dynamic current path and its return loop. (See WP009: Impact of Parasitics on Performance).

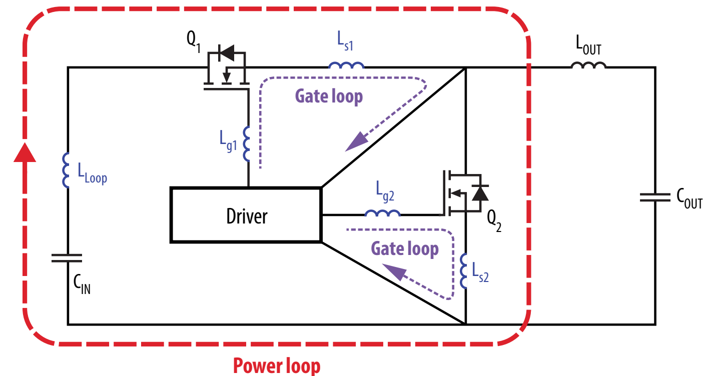

Figure 1: Equivalent circuit of an eGaN FET-based power stage with parasitic inductances and dynamic current loops highlighted.

Optimal layout for an eGaN FET-based power stage

The smallest power loop and gate loop inductance can be achieved by taking advantage of an inner PCB layer to form an optimized return path. The decoupling capacitors are placed close to the drain of the high-side transistor. PCB vias are used to connect the ground terminal of the capacitors to the low-side source by way of the first inner layer, where the dielectric thickness is intentionally kept thin to keep the inductance low. An example of this optimal layout technique is shown in figure 2.

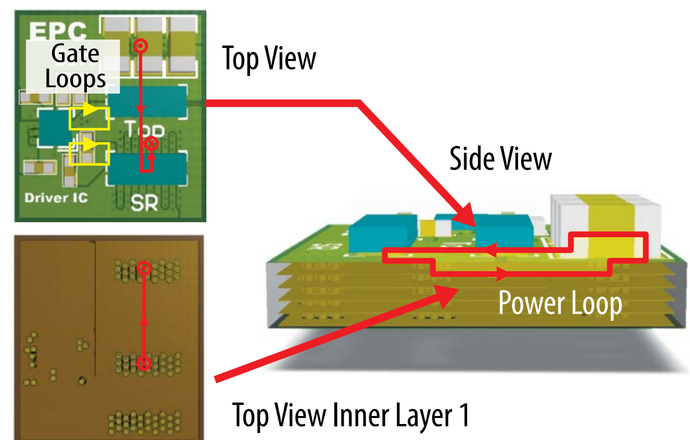

Figure 2: Optimal layout for an eGaN FET-based power stage, highlighting the dynamic current loop paths.

The gate driver must be located very close to the gate and source terminals of each transistor or transistors it drives, and the bypass/bootstrap capacitors and gate resistors should be positioned so that the gate current direction is orthogonal to the power loop. It is critical to separate the gate return current path from the power loop at the source terminal to minimize the common-source inductance.

For more detailed information please see the following resources:

- Textbook: GaN Power Devices and Applications
- Webinar: Layout Techniques to Maximize GaN Device Performance

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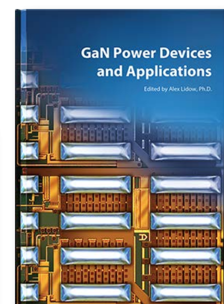

How an optimal layout benefits converter performance

Converter systems with eGaN FETs inherently outperform comparable Si-based designs, and optimal layout techniques further enhance these benefits. Figure 3 demonstrates the eGaN advantage in a 48 V to 12 V buck converter operating at 500 kHz, comparing the EPC2045 100 V eGaN FET against a 100 V Si MOSFET in an S3O8 package. Both converters employ the optimal layout technique, but the tiny chip-scale EPC2045 allows for considerably lower loop inductance than the larger Si MOSFET. Figure 3 shows that the eGaN version achieves 5x the voltage slew rate while maintaining the same peak overshoot voltage as the Si version, owing to the lower loop inductance combined with the fast switching capability of GaN. The faster switching edge has a tremendous impact on the system system performance.

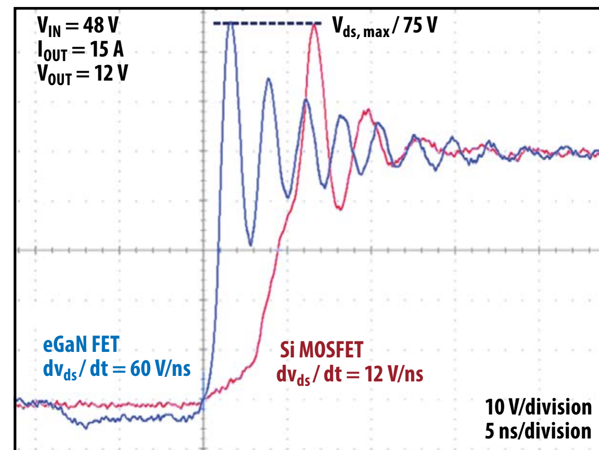

Figure 3: Comparison of switch node waveforms of a 48-to-12 V buck converter with EPC2045 eGaN FETs in the optimal layout, against a 100 V Si MOSFET example.

Monolithic eGaN half bridge IC

Monolithic integration with eGaN ICs offer further improvement in loop inductance. For example, shown in figure 4 is the system efficiency of the EPC2152 monolithic power stage (green line) when operated as a buck converter at 1 MHz with 48 V_{IN} and 12 V_{OUT} at 10 A. The black "X" in figure 4 shows the comparative performance of a state-of-the-art silicon solution at 1 MHz. The GaN monolithic power stage achieves a 50% reduction in power loss versus the silicon solution.

Also shown in figure 4, is the advantage gained by integrating the driver and the power FETs on the same chip. The blue line is the measured efficiency of the identical half bridge, but with discrete GaN FETs and the driver and level shift in a separate Si-based IC. The two main reasons for the significant improvement in efficiency are; (1) the reduced inductance in the gate loop when the driver and power devices are in intimate contact on the same chip, and (2) the monolithic integration of the two power FETs cuts in half the overall power loop inductance.

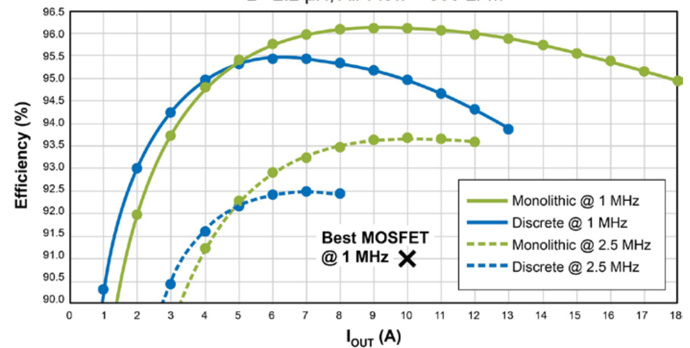

Figure 4: The EPC2152 power stage operating at 1 MHz (blue line) has an overall power loss (including inductor and control IC) at 10 A that is 50% lower than the best Si MOSFET solution (black X) when operated with 48 V_{IN} and 12 V_{OUT}. The green line shows the comparative performance when the power stage is fabricated with discrete GaN FETs driven by a silicon IC.

Conclusions

With the faster switching speed of eGaN FETs, improved packaging and layout techniques are required to minimize parasitic inductance and fully utilize these advanced devices. Chipscale eGaN FETs reduce the packaging inductance to nearly zero, while enabling ultra-low inductance PCB power loops. Optimizing the PCB layout is a crucial step in achieving the maximum performance capability of eGaN FET-based designs.

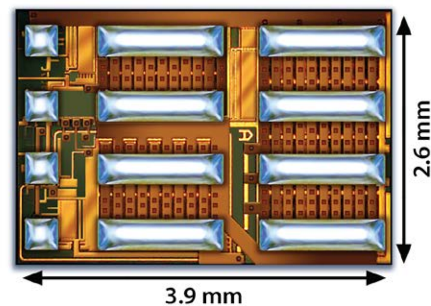

Figure 5: EPC2152, 80 V, 15 A ePower™ Stage IC.

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