Thermal Management of eGaN® FETs

Motivation

Enhancement-mode gallium nitride (eGaN®) FETs offer high power-density capabilities with ultra-fast switching and low on-resistance, all in a compact form factor. However, the achievable power levels are limited by thermal overheating due to the extreme heat-flux densities. If not managed properly, the generated heat can result in excessive self-heating and elevated temperatures that compromise reliability and performance. For that reason, thermal management strategies are essential for high-power devices, and with chip-scale packaging of eGaN® FETs, many design advantages can be leveraged at the board-side and the backside (i.e., case) for improved heat dissipation.

This application note presents simple thermal management guidelines to enhance heat conductance from the GaN FETs and optimize thermal performance. In addition, a case study is presented with simple and effective thermal management solutions for the cooling of a development board with two active GaN FETs.

Overview

Packaged electronic devices dissipate generated heat through two main heat conduction paths – to the printed circuit board (PCB) at the board-side and to the case at the backside, both of which can benefit from thermal management strategies. The first thermal resistances to heat dissipation encountered are at the FET construction level from the junction to the board ($R_{\theta JB}$) and from the junction to the case ($R_{\theta JC}$). The thermal resistance to heat conduction is generally described as:

$$R_{\theta JX} = \frac{T_J - T_X}{P}$$

Where,

$R_{\theta JX}$, alternatively, Θ_{JX} *(°C/W or K/W)* = thermal resistance from junction to a reference location X

T_J *(°C or K)* = device junction temperature in steady state conditions

T_X *(°C or K)* = temperature of reference location (board (B), case (C), or ambient (A))

P *(W)* = power dissipated in the device

These two thermal resistances differ for each FET since they depend on the device construction and on the thermal conductivity of the materials used. For wafer-level chip-scale packaged (WLCSP) GaN FETs, the thermal resistance to case is lower than silicon devices (Figure 1), and thus the junction-to-case path provides good thermal conductance. With simple methods that ensure optimal thermal practice, both $R_{\theta JC}$ and $R_{\theta JB}$ can be used to significant advantage.

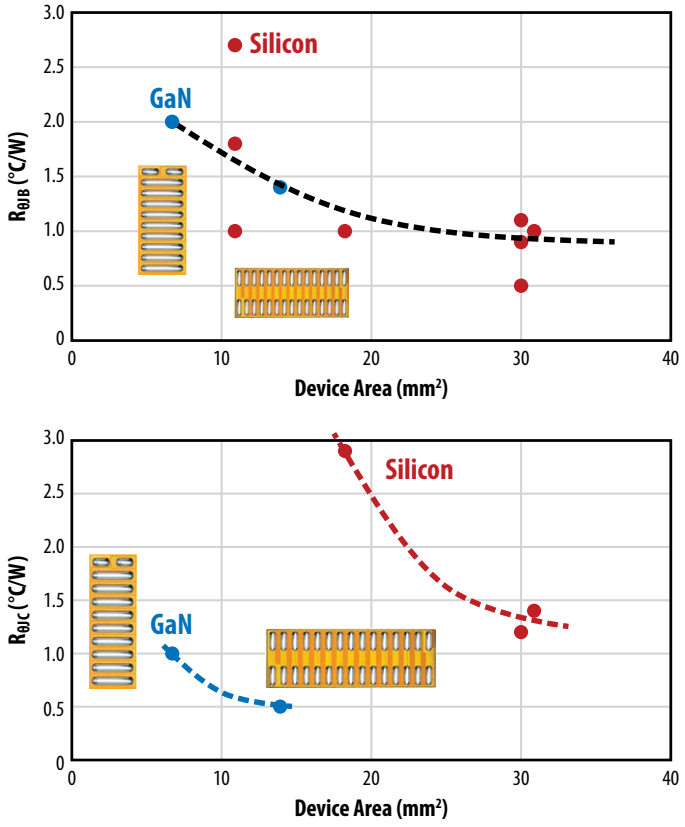


Figure 1: Junction to case and to board thermal resistance comparison between GaN and silicon devices.

Junction-to-Board Thermal Improvement Strategies

The maximum temperature rise (in °C or K), and the resulting overall thermal resistance (in K/W), are reported for the maximum temperature at the device junction, in reference to an ambient temperature in still air ($R_{\theta JA}$) or in moving air ($R_{\theta JMA}$). The thermal resistance to the board is one component in a network of heat conduction paths that determines the overall self-heating in a GaN FET device.

The simplified circuit model in Figure 2 represents the main heat conduction paths from the junction to ambient within a standard PCB layout with two FETs. Since the FET area is much smaller than that of the PCB, the heat dissipated from the FET to ambient through the case is minimal and thus the thermal resistance $R_{\theta CA}$ is large. As a result, without any back-side cooling, the main heat dissipation path from the FET is through the PCB, which is why we must ensure good thermal conductance at the board-side.

Heat conduction from the FET into the board is carried mainly by the copper traces within the conducting layers of the PCB. Designing thicker copper traces for low electrical resistance also benefits thermal resistance and provides a high heat-conductance medium at each layer of the PCB. For example, a 2-ounce (oz) copper layer has twice the conductance of 1 oz copper layer in the lateral directions. Moreover, the in-plane heat conductance is proportionally dependent on the number of layers, where more layers offer more paths to dissipate heat.

In the through-plane direction, the insulating dielectric layers separating the copper layers have a low thermal conductivity and thus obstruct heat dissipation. This issue can be partially overcome by placing vias within or near the FETs to provide a high thermal conductivity path that bridges the dielectric layers and carries the generated heat into the inner copper layers of the PCB. The inner layers, in turn, contribute to heat spreading, further decreasing the thermal resistance into the board ($R_{\theta JB}$) and eventually into ambient air ($R_{\theta JA}$). Strategically placed thermal vias near or under the FET pads can reduce self-heating (ΔT) by up to 33% as shown in detailed thermal simulations (Figure 3).

The vias modeled in the simulations have a Via-in-Pad-Plated-Over (VIPPO) construction which is described in the insert.

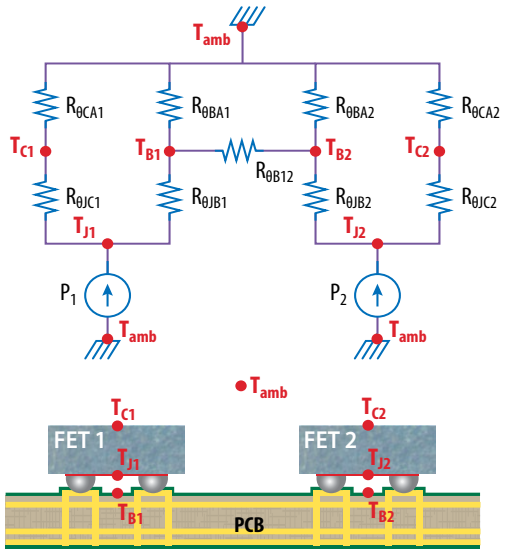
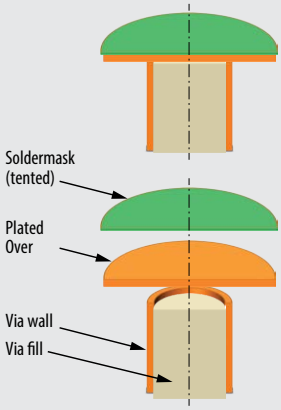


Figure 2: Simplified thermal resistance network model showing main heat conduction paths and associated temperature nodes for a FET layout.

Via-In-Pad-Plated-Over (VIPPO)

- Wall thickness = 0.78 mil per IPC standard class 2
- Hole diameter (typical) = 7.8 mil
- Annular ring = 13.8 mil diameter min.
- Plated over
- Non-conductive filled
- Tented on both sides of the board
- Used for under bump and close to component pads
- Usable up to 2 oz (2.8 mil / 70 µm) copper thickness



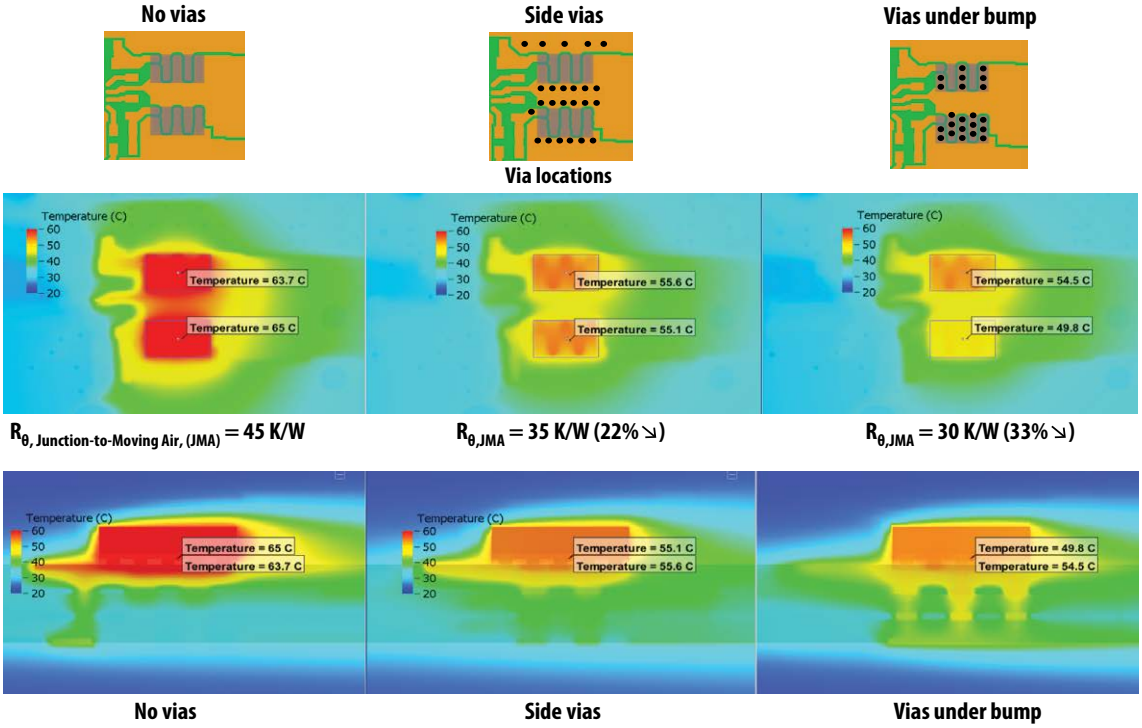


Figure 3: PCB thermal performance comparison between different configurations that include thermal vias near and underneath the FET pads.

Junction-to-Case Thermal Improvement Strategies

Another path for heat dissipation from a GaN FET device is through the "case" (i.e. the die) which, for wafer level chip-scale packaged (WLCSP) devices, offers a much lower resistance ($R_{\theta JC}$) than the board-side and lower than other types of packaged devices. Since the exposed die area of the FETs is too small for any significant thermal exchange with the surrounding air, implementing simple thermal management strategies can considerably improve backside cooling.

Adding a heat spreader in contact with the die conducts heat in the lateral direction, increases the device effective surface area, and reduces its operating temperature. To further increase the heat exchange area with ambient air, a heat sink can be attached to the heat spreader. High-conductivity materials such as aluminum and copper should be used to ensure optimal performance of the heat spreader and heatsink (Figure 4).

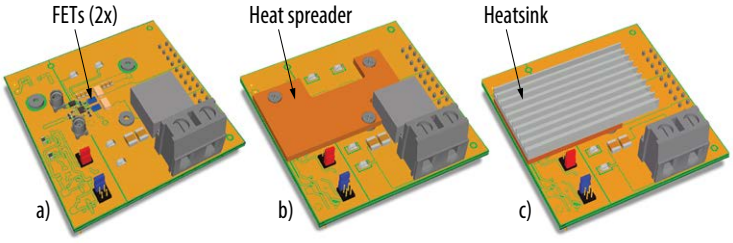


Figure 4: PCBs with a) no back-side cooling, b) with a connected Copper heat spreader, and c) with an Aluminum heatsink. Note: The heat spreader and heatsink can be combined or independent and heat flux still flows into PCB.

Heatsink Attachment Approach

A simple and assembly-friendly approach to attaching a heatsink to GaN FETs and ICs is illustrated in Figure 5. It includes a thermal interface material (TIM) to enhance the thermal conductivity at the interface between the device and the heatsink, as well as to provide electrical insulation. An SMD spacer maintains a proper distance between the heatsink and the GaN device for the TIM and provides sturdy mechanical attachment for the heatsink. Components that are taller than the SMD spacers must be excluded from under the heatsink.

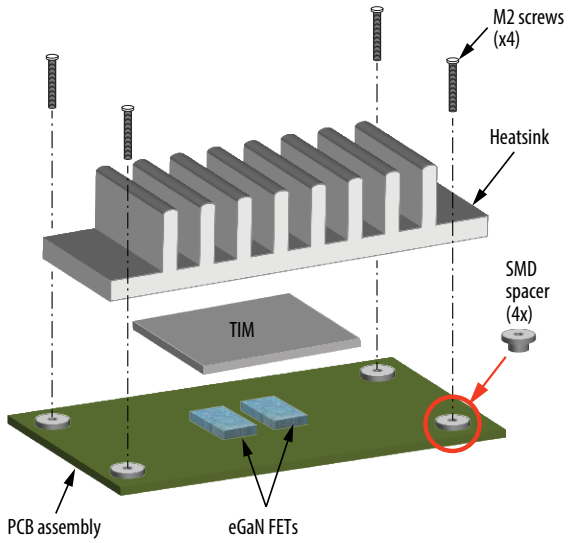


Figure 5: An example of heatsink assembly using screws.

Thermal Interface Material (TIM) Properties Considerations

The heat spreader/heatsink attachments added for backside cooling introduce several interfaces that add resistance to heat conduction due to surface roughness and thermal contact imperfections. Moreover, air gaps between the components and attachments are not effective in transporting heat across. To overcome the thermal resistance encountered, thermal interface materials (TIMs) are used to improve thermal contact and provide good conductance at the interface. TIM materials can come in several forms, including pads, gels, and liquid gap fillers.

The choice of a TIM should be based on several selection criteria. First, the TIM must have good thermal conductivity (κ) to ensure good heat conductance and low thermal resistance. A good value for $\kappa > 3$ W/m.K is cost effective. TIMs with higher performance reaching $\kappa > 15$ W/m.K are available, but are more expensive, and thus can be used at the FET interface for optimal heat conductance. The electrical resistivity is also important for the GaN FET die since the upper FET case will be at switch-node potential and must be electrically isolated from the thermal solution (Figure 6). T-Global A1780 and A6200 TIMs are examples for thermally and electrically compliant TIMs with high and moderate $\kappa = 17.8$ W/m.K and 6.2 W/m.K respectively.

Another consideration for TIM selection is the exerted compression force on the die for a certain compression rate (thickness percentage given in the materials' datasheets). The compression force must not exceed the stress limit of the GaN FETs. Generally, larger devices can withstand higher force, LGA devices can withstand higher force than the equivalent BGA devices of the same size. The maximum recommended pressure on eGaN FETs and ICs is 40 PSI/mm^2 of the total bump area and 50 PSI for GaN devices in general based on testing results.

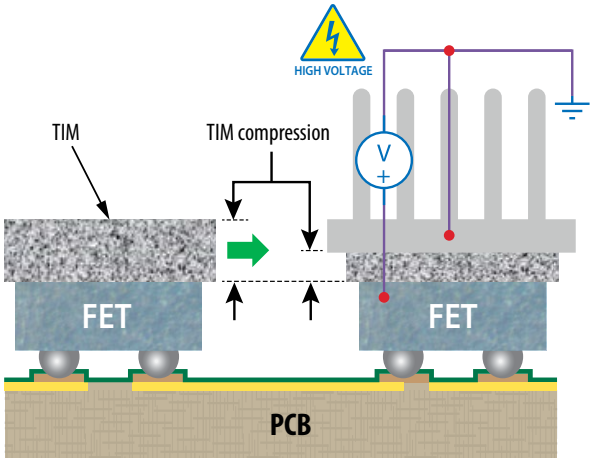


Figure 6: Illustration of a heatsink attachment with a TIM pad for GaN FETs and ICs.

For the small scale of GaN FETs, the area of the die sides is comparable to the top and bottom surfaces, and thus the sides can contribute considerably to heat conductance. For instance, the 0.9 mm x 0.9 mm x 0.625 mm **EPC2038** FET die has a top and bottom surface area of 1.62 mm^2 with the four sides measuring 2.25 mm^2 in all. As a result, the four sides can also be utilized to increase heat dissipation.

This can be done by adding a gap filler material around the sides of the FET such as the GF4000 liquid gap filler from Bergquist (κ = 4 W/m.K). The filler replaces the gap air with a good thermal conductivity material (Figure 7) and thus offers a good medium for heat conductance from the four sides of the GaN device to the board and to the backside cooling solution.

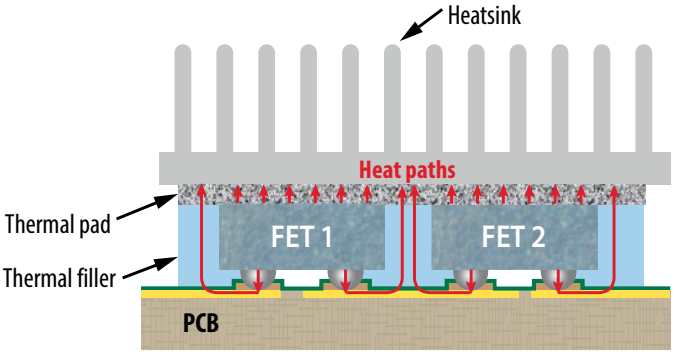


Figure 7: Illustration showing thermal solution attachment with TIM pad and thermal gap filler.

The resistive circuit model of Figure 2 is now modified in Figure 8 to include the additional thermal resistances for the backside (case) cooling representing the heat conduction from the case to the sink ($R_{\theta CS}$) and from the sink to ambient ($R_{\theta CS}$) (Figure 9). Since the board is also connected to the sink through the metal shim, spacers and gap filler, heat conduction is also present between the board and sink and is represented by ($R_{\theta BS}$). It might appear that more thermal resistances are added to the thermal resistive network after the thermal solution is attached, however, the combined thermal resistances of $R_{\theta CS}$ and $R_{\theta SA}$ are ideally much lower than $R_{\theta CA}$. Thus, the overall effect is an improvement in the total thermal resistance.

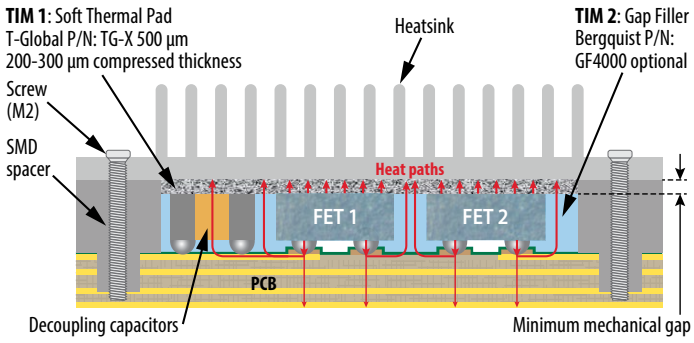


Figure 8: Illustration of comprehensive thermal solution assembly with heatsink, SMD spacers, TIM pad and gap filler.

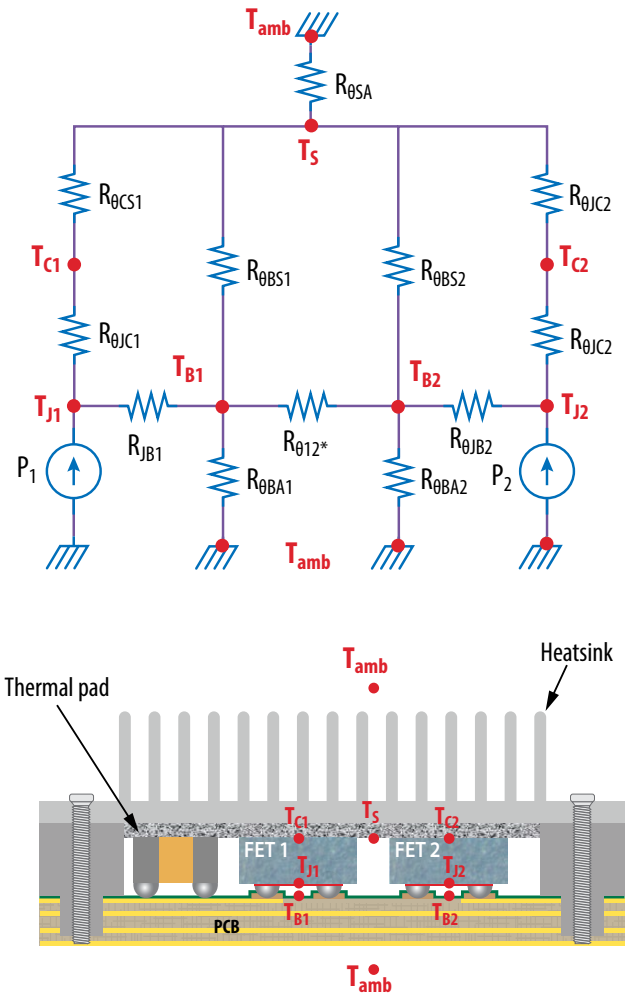


Figure 9: Thermal resistance circuit model with heat sink attachment and corresponding cross-sectional image. Note: T_S assumed uniform in location of FETs.

Heat Spreading and Heat-Sinking Performance

The thermal improvement of attaching a heat spreader and heatsink is demonstrated using the **EPC9097** development board with two **EPC2204** GaN FETs which are considered major heat sources that must be cooled. Multiple scenarios are considered in Table 1. First, a copper heat spreader ($\kappa \approx$ 400 W/m.K) is attached to the board using M2 screws and SMD spacers. The high-performance TG-A1780 TIM (κ = 17.8 W/m.K) is used between the FETs and the heat spreaders (Figure 2). In the second model, an aluminum heatsink is attached to the heat spreader using the same type of TIM. Power losses of 1W are assigned to each FET. The PCBs are placed in 400 LFM air flow at 20°C for forced convection cooling.

The models in Table 1 are also compared with the baseline models where only board-side cooling is present, and the effect of the via placement is also analyzed. The maximum temperature is extracted from the thermal model and the overall thermal resistance is calculated in reference to ambient temperature for each FET power (1 W). The percentage of heat dissipated from the board-side and from the case-side are also reported to compare the thermal resistance of each path.

The results of the thermal analysis in Table 1 show that even without backside cooling, improvements to the board design can result in enhanced heat conductance to the board and up to 30% reduction in temperature (Figure 3). In comparison to board-side cooling, adding a heat spreader to the FETs reduced the overall thermal resistance from 34 K/W to 22 K/W (about 40%), while a heatsink reduced the overall thermal resistance to ambient to around 15 K/W (a 60% decrease from baseline). By reducing the thermal resistance to back-side cooling, the percentage of heat dissipated through the case increased from 2% (baseline) to 45% with a heat spreader and 61% with an attached heatsink. Given that junction-to-sink thermal resistance is at 4.9 K/W, improving the heatsink solution (larger fins, more air flow) can reduce the overall thermal resistance of 14.9 K/W even further.

Conclusions

A detailed overview of simple and cost-effective thermal management strategies is presented to improve heat conductance from active GaN FETs. Both board-side cooling and backside (case) cooling strategies are discussed. When limited to board-side cooling, strategically placing thermal vias under or near the FETs can improve board conductance significantly and allow heat to dissipate into the board's inner copper layers more effectively, reducing peak operating temperatures by around 30%. Moreover, with a low junction-to-case thermal resistance of WLCSP GaN FETs, the backside offers considerable thermal cooling potential.

Simple thermal management strategies, such as attaching a heat spreader or a heatsink, can increase the device effective thermal dissipation area and reduce FET temperatures by up to 60% as shown by detailed simulations. With good thermal considerations and simple thermal management strategies, small chip-scale devices can be adequately cooled for reliable performance in high-power applications.

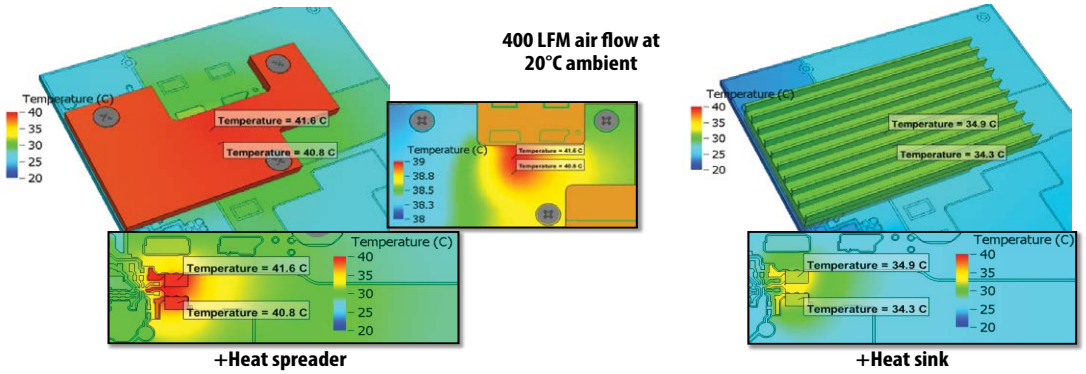


Figure 10: Thermal simulation results for EPC9097 PCB with EPC2204 FETs with heat spreading and heatsinking solutions.

Table 1: Results Summary of the Thermal Simulations for the different analyzed cases

Case	$R_{th,JMA}$ (K/W)	Percent Improvement	Percent of Heat Extracted From PCB	Percent of Heat Extracted From Case	$R_{th,JS}$ (K/W)
No Vias	45.0	-28%	96	3	—
Side Vias	35.6	-7%	97	2	—
Vias Under Pads (Baseline)	34.5	—	97	2	—
+ Heat Spreader	21.6	39%	54.5	45	4.9
Heat Spreader + Heat Sink	14.9	60%	38.5	61	4.9

For more detailed information please see the following resources:

- Textbook: GaN Power Devices and Applications
- Webinar: Layout Techniques to Maximize GaN Device Performance
- Web-based Thermal Calculator