GaN FETs and ICs Visual Guide

APPLICATION NOTE: AN010

Enhancement Mode GaN FETs and ICs Visual Characterization Guide

EFFICIENT POWER CONVERSION

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A detailed description of the EPC enhancement mode transistors and integrated circuits physical characteristics is given including the visual criteria all devices must meet before they are released for shipment to customers. This article, used in conjunction with the two companion articles, "Assembling eGaN FETs"¹, and "EPC GaN Transistor Parametric Characterization Guide"², gives the user a set of tools to develop circuits and systems that take advantage of the enhancement mode GaN FET's and IC's advanced form factor and consequent unprecedented performance potential.

OVERVIEW OF GALLIUM NITRIDE (GaN) TECHNOLOGY

In June of 2009, Efficient Power Conversion Corporation (EPC) introduced the first enhancement mode gallium nitride on silicon power transistors designed specifically as power MOSFET replacements. These products were developed to be produced in high volume at low cost using standard silicon manufacturing technology and facilities. For more information about EPC's GaN technology, go to www.epc-co.com.





STRUCTURE

A device's cost effectiveness starts with leveraging existing production infrastructure. EPC's process begins with silicon wafers. A thin layer of Aluminum Nitride (AIN) is grown on the Silicon to isolate the device structure from the substrate. On top of this AIN, a thick layer of highly resistive GaN is grown. This layer provides a foundation on which to build the active transistor. An electron generating material comprised of Aluminum, Gallium, and Nitrogen (AlGaN) is applied on top of the GaN. This layer creates an abundance of free electrons just below it. Further processing forms a depletion region under the gate. To enhance the transistor, a positive voltage is applied to the gate in a similar manner to turning on an n-channel, enhancement mode power MOSFET. A cross section of this structure, repeated many times to form a





Figure 2: Device construction

complete power device, is depicted in figure 1. The end result is a fundamentally simple, cost effective solution for power switching³. EPC's GaN transistors are lateral devices with all three terminals: gate, drain, and source, on the top side of the chip. Generally, EPC devices have three layers of metal used to connect the active device to the outside world (fig 2). The top metal layer is then used as a foundation for solder bumps as shown in Figure 3. This configuration allows EPC's GaN transistors to eliminate unnecessary elements of traditional power MOSFET packaging that contribute to higher inductance, thermal and electrical resistance, higher costs, and compromised reliability.

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A VISUAL TOUR

This section includes bump and side views of selected EPC's GaN transistors and integrated circuits. Solder bars or solder balls are used to make reliable connections directly to a printed circuit board. A polyimide coating on top of multiple silicon dioxide and silicon nitride layers are used to seal the active device from the outside environment.

This section shows a selection of EPC's eGaN FETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNF

EPC2040



0.85 mm x 1.2 mm Max size (µm): 880 x 1230





1.3 mm x 0.85 mm Max die size (μm): 1330 x 880





1.35 mm x 1.35 mm Max die size (µm): 1380 x 1380



EPC8002 EPC8004 EPC8009 EPC8010



2.05 mm x 0.85 mm Max die size (μm): 2080 x 880





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100 +/- 20

EPC2015C EPC2001C



4.1 mm x 1.6 mm Max size (μm): 4135 x 1662

EPC2029

EPC2030 EPC2031

EPC2032

EPC2033 EPC2034

EPC2034C 4.6 mm x 2.6 mm

Max size (µm): 4135 x 1662





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EPC2020 EPC2021 EPC2022 EPC2023 EPC2024 EPC2206

6.05 mm x 1.6 mm Max size (μm): 6080 x 2330





This section showed a selection of EPC's eGaN FETs and ICs. For a full listing of products please see the website at: epc-co.com/epc/Products/eGaNFETsandICs

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EPC designed these devices such that they are quite robust. In figure 4 are some examples of devices that were intentionally tested after extreme mechanical abuse.

Figure 4a, b, and c: EPC transistors with extreme mechanical damage successfully completed long term reliability testing. It should be noted that the substrate is not electrically active with respect to the device.



Fig 4c: EPC1001 part (above) passed 1000 Cycle TC -40°C to 125°C . Die width ~1900 µm Back side chip >250 µm

The edge protection structure reduces the risk of damage to the active portion of the device. Figure 5 is a set of microscope images of the typical edge structures and, for clarity, the original design plots are also shown to the left. Care should be taken during assembly such that chips cannot touch the polyimide edge seal ring.



Fig 4a: Visual reject part shown in pictures above – EPC1001 part above passed 1000 hours HTRB 100 V bias 125°C. Back side chip extends down to the front of the chip. **Far right:** (area indicated with arrow) Unsupported chip structure hanging out over corner passed 1000 hours HTRB.



Fig 4b: Visual reject part shown in pictures above – EPC1001 part with severe corner chip. Back side chip extends all the way through the chip. Die was still functioning in application. Die is shown post dismount from PCB board.



Fig 5: EPC's die top surface is designed to reduce the probability that chips will intrude into the active portion of the device. Pictured is the edge structure which includes two dummy metal rings and a polyimide coating.

SHIPMENT CRITERIA

Prior to shipment, 100% of EPC devices are electrically tested and visually inspected. Tables 1a and 1b show a summary of the visual Acceptance/Rejection criteria used as of the date of this writing. Tables 2a and 2b, over the following pages, contain several examples of both good and bad die measured against these criteria.

Table 1a: Front side visual inspection criteria

Die Front Side Visual Inspection Category	Rejection Criteria	
Amount of remaining street	Amount of remaining street can be zero providing no chip is beyond second (outer) metal dummy ring	
Chips	Chip touches seal ring	
Damaged Solder Bumps	Solder drag or displacement >50% of original distance between bumps; defect which reduces bump height by 30% of original height	
Foreign material	Foreign material linking any two bumps	
Contamination /defect / metal residue / bridging material (can appear as stains or severe discolorations)	Any contamination, defect, metal residue or bridging material that is $>50\%$ of original distance between bumps or eliminates the separation between adjacent metal lines	
Ink dots	Ink on front of chip	
Missing Bumps	Any missing bumps	
Particles	Reject if particle reduces the original distance between bumps by 50%	
Polyimide peeling, incomplete	Area bridging two adjacent top metal layers	
Probe Marks	Reject if no probe marks	
Probe Needle Drag	Solder drag or displacement >50% of original distance between bumps or crossing metal lines	
Scratches	Scratches through the polyimide > 25% of the width of the metallization block under the bump	

Table 1b: Back Side Visual Criteria

Note : substrate is not electrically active with respect to the device

Die Back Side Visual Inspection Category	Rejection Criteria	
Chips	Nominal chip thickness without the bump is listed in datasheet for each device. MIL883 says reject if chip is $>50\%$ of total die thickness deep. Post datecode 1944* the reject chip extends a distance/depth of 100 µm or more away from the edge of the die.	
Correct back side marking for part number EPCXXXX, first line of back side laser mark will be XXXX	Reject if EPC part number is not correct in first scribe line or if marking is not legible	
Orientation in pocket	Incorrectly oriented in pocket (locator dot should be on side near carrier tape holes)	
Particles	Specification in development	
Scratches	Specification in development	
Stains / Discoloration / Burn Marks	Laser mark not readable	

*Note: Prior to datecode 1944, reject if chip is $> 250\,\mu\text{m}$ wide

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TABLE 2a: EPC die front side visual examples of Accept/Reject categories

Amount of remaining street

Reject Criteria:

Amount of remaining street can be zero providing no chip is beyond second (outer) metal dummy ring.

See section on chips



Street (thin white line) seen all the way around die in above pictures. Remaining street width can vary.



No street visible at 40X on left side of die, but no chips into the outer metal dummy ring at 200X

ACCEPT





No street visible at 40X on left side of die. Chip can be seen. This chip extends past both metal dummy rings when checked at higher magnifications



Chip on left side can be seen at 100X is past both dummy metal rings. At 200X, defect is shown certainly past both the dummy metal rings.

REJECT

Chips

Reject Criteria: Chip cannot touch edge seal



At 400X, showing the two metal dummy rings in one die edge design type

ACCEPT

Damaged solder bumps

Reject Criteria:

solder drag or displacement >50% of original distance between bumps; defect which reduces bump height by 30% of original height



Clean die



2 1



Shown at 400X. Defect is

past the outer the metal dummy ring #2.

REJECT

Solder drag

Squashed bumps

TABLE 2a: EPC die front side visual examples of Accept/Reject categories (continued)

Foreign material	ACCEPT	REJECT
Reject Criteria: Foreign material linking any two bumps	Ko foreign material (street not shown in picture)	Foreign material bridging bumps
Contamination /defect / metal residue / bridging material (can appear as stains or severe discolorations) Reject Criteria: Any contamination, defect, metal residue or bridging material that is >50% of original distance between bumps or eliminates the separation between adjacent metal lines	ACCEPT	REJECT Interpretent of KYEC Interpretent of KYEC
Ink dots	ACCEPT	REJECT
Reject Criteria: Ink on front of chip		
	Image: No ink on these chips	Ink dot seen on chips
Probe marks	ACCEPT	REJECT
Reject Criteria: Reject if no probe marks	This die has probe marks on the bumps	No probe marks – this is a reject

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REJECT

TABLE 2a: EPC die front side visual examples of Accept/Reject categories (continued)

Scratches

Reject Criteria:

Scratches through the polyimide > 25% of the width of the metallization block under the bump or bridging metal lines



ACCEPT

No scratches





Scratch straddling metal lines



Scratch cuts across all the metal dummy rings

and first metal 3 ring

TABLE 2b: EPC die back side visual examples of acceptable and rejectable categories

Note : Substrate is not electrically active with respect to the device

Back Side Chips Reject Criteria:

Nominal chip thickness is listed in the datsheet for each device. MIL883 says reject if chip is >50% of total chip thickness deep. Post datecode 1944*, the reject chip extends a distance/depth of 100 um or more away from the edge of the die.

Die Back Side Chipping Details

Nominal chip thickness is listed in the datsheet for each device. MIL883 says reject if chip is >50% of total die thickness deep. Post datecode 1944*, the reject chip extends a distance/depth of 100 um or more away from the edge of the die. Example against part number EPC2007C that has max length of 1632 µm is shown below:



ACCEPT



Die is > 0.9 mm wide Chips < 100 μm wide



Same die as at left: Backside chips are very shallow

1015 9001 5241

REJECT



Die is 1.6 mm wide, chip is $>100 \ \mu m$ wide. Lower left corner is broken down to front side of die

*Note: Prior to datecode 1944, reject if chip is > 250 µm wide

TABLE 2b: EPC die back side visual examples of Accept/Reject categories (continued)

Note : substrate is not electrically active with respect to the device

