Bodo´s Power Systems®

Testing Gallium Nitride Devices to Failure Under Extreme Voltage and Current Stress

Standard qualification testing for semiconductors typically involves stressing devices at-or-near the limits specified in their data sheets for a prolonged period of time, or for a certain number of cycles, with the goal of demonstrating zero failures. By testing parts to the point of failure, an understanding of the amount of margin beyond the data sheet limits can be developed, but more importantly, an understanding of the intrinsic failure mechanisms of the semiconductor can be found.

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By knowing the intrinsic failure mechanisms, the root cause of failure, and the device's behavior over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions [1].

Stressors and Intrinsic Failure Mechanisms

The key stress conditions for all power transistors involve voltage, current, temperature, and humidity as listed in Table 1.

Stressor	Device/ Package	Method	Intrinsic Failure Mechanism	Evidence
Voltage	Gate-Source	HTGB	Dielectric failure (TDDB)	Gate-Source Leakage
			Threshold shift	Gate-Source Threshold
	Drain-Source	HTRB	$R_{DS(on)}$	$R_{DS(on)}$ Shift vs. Time
Current	Drain-Source	DC current	Electromigration	$R_{DS(on)}$ Failure
			Thermomigration	$R_{DS(on)}$ Failure
			Thermal	DC SOA failures
		Pulsed current	Thermal	Pulsed SOA failure
			Unknown mechanism	Hyper-fast high current pulses
Voltage rising/falling	Drain-Source	Super-hard switching tests	$R_{DS(on)}$	$R_{DS(on)}$ Shift vs. Time
Current rising/falling	Drain-Source	High current narrow pulse	Unknown mechanism	Hyper-fast high current pulses
Temperature	Package	Storage Temperature	Unknown mechanism	MSL1 testing
				High temp storage
Chemical	Package	Humidity	Dendrite formation/ corrosion	H3TRB testing
				HAST testing
Mechanical strain	Package	Temperature cycling	Solder fatigue	Temperature cycling test
		IOL	Solder fatigue	Temperature and Current test
		Bending force test	Delamination	I_{DSS} failures
		Die shear	Solder strength	Solder strength test
		Package force	Device breakage	Device pressure testing

Table 1: Stress Conditions and Intrinsic Failure Mechanisms for eGaN® FETs

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test (DUT) can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the data sheet limits of the product.

This article focuses on the stressor of current. Parts were tested to failure under two specific conditions that demonstrate the exceptional robustness of eGaN FETs; (1) Safe Operating Area (SOA), where eGaN FETs are exposed simultaneously to high current (I_D) and high voltage (V_{DS}) for a specified pulse duration; and, (2) short circuit withstand time, where eGaN FETs are subjected to a short circuit with the gate turned on up to its maximum voltage.

Safe Operating Area

The primary purpose of SOA testing is to verify the FET can be operated without failure at every point (I_D, V_{DS}) within the data sheet SOA graph. It can also be used to probe the safety margins by testing to fail outside the safe zone.

During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure. In Si MOSFETs, another failure mechanism, known as secondary breakdown (or Spirito effect [2]), has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D, is caused by an unstable feedback between junction temperature and threshold V_{TH}.

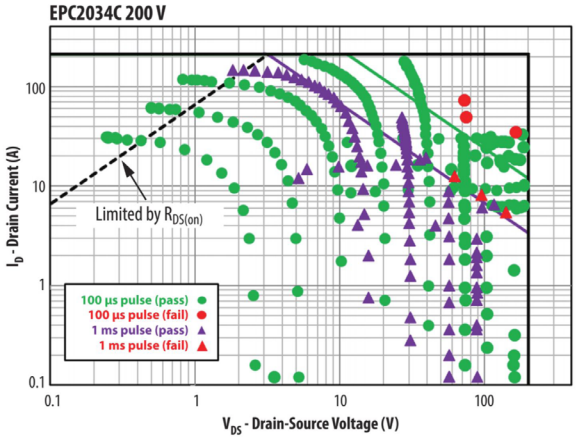

Figure 1: EPC2034C SOA plot. "Limited by $R_{DS(on)}$" line is based on data sheet maximum specification for $R_{DS(on)}$ at 150 °C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown. Failures are denoted by red triangles (1 ms) or red dots (100 µs).

Figure 1 shows the SOA data of a 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D,V_{DS}) space. These points are overlaid on the data sheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. A broad area of the SOA was interrogated without any failures (all green dots), ranging from

low V_{DS} all the way to $V_{DS;max}$ (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the data sheet graph. The same applies to 1 ms pulse data (purple and red triangles): all failures occurred outside of the data sheet SOA.

Figure 2 compares SOA data between a commercial power MOSFET (dotted lines) and an EPC2045 eGaN FET (solid lines) with a similar rating. The secondary breakdown is evident in the Si power MOSFET at drain voltages as low as 10 V_{DS} for 1 ms pulses.

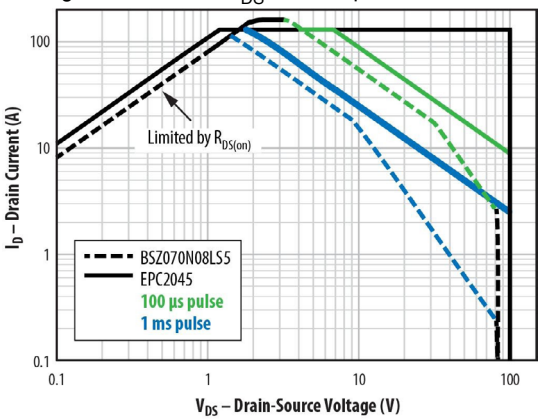

Figure 2: Comparison between a BSZ070N08LS5 MOSFET and an EPC2045 eGaN FET safe operating area

Short Circuit Testing

Short-circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in a power converter while in the ON (conducting) state. In such an event, the part will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor itself and the circuit parasitic resistance. If the short-circuit state is not quenched by protection circuitry, the extreme power dissipation will ultimately lead to thermal failure of the FET.

The goal of short-circuit testing is to quantify the withstand time the part can survive under these conditions. Typical protection circuits can detect and react to over-current conditions in 2-3 µs. It is therefore desirable for eGaN FETs to withstand unclamped short-circuit conditions for about 5 µs or longer.

Two representative eGaN FETs were tested: EPC2203 (80 V), a 4th generation automotive grade (AEC) device, and EPC2051 (100V), a 5th generation commercial-grade device.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure. Table 2 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS(max)}$), with mean withstand time of 20 µs and 13 µs respectively. Note that the part survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 µs) compared with the EPC2203 at 6 V. This is expected because of more aggressive scaling and current density of this device. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 2 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was calculated to determine the rise in junction temperature, ΔT_J, during the short-circuit pulse. The results are shown in figure 3.

The intense power density during the pulse leads to rapid heating in the GaN layer and nearby silicon substrate. or EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of 850 °C. The same is true for EPC2051, where both conditions fail at the same ΔT_J of 1050 °C.

Short Circuit Pulse V_{DS} = 60 V	EPC2203		EPC2051	
	V_{GS} = 6 V	V_{GS} = 5 V	V_{GS} = 6 V	V_{GS} = 5 V
Mean TTF (µs)	13.1	20	9.33	21.87
Std. dev. (µs)	0.78	0.37	0.21	2.95
Min. TTF (µs)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	3.211	2.554	5.516	3.699
Energy (mJ)	43.36	50.24	50.43	77.34
Die area (mm²)	0.9025		1.105	
Average power / area (kW/mm²)	3.558	2.83	4.99	3.35
Energy / area (mJ/mm²)	48.05	55.67	45.64	69.99

Table 2: Short-circuit withstand time statistics for EPC2203 and EPC2051. Average pulse power and energy correspond to a typical part within the population.

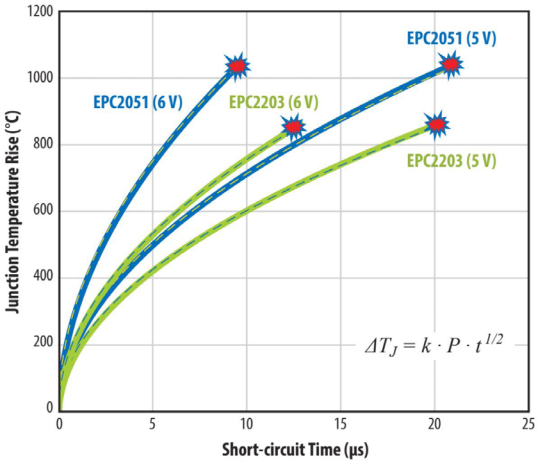

Figure 3: Calculated junction temperature rise vs. time during the short-circuit pulses for EPC2051 and EPC2203 at 5 V and 6 V V_{GS}. Measured failure times are indicated by red markers.

Conclusion

Further analysis is required to determine the exact mechanism of failure. Nonetheless, the experimental results presented in this study demonstrate the outstanding capability of eGaN FETs under extreme voltage and current stress.

References

[1] ZVEI Robustness Validation Working Group, Eds., Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications, Third edition: May 2015, Published by ZVEI – Zentralverband Elektrotechnik – und Elektronikindustrie e.V. Available at https://www.zvei.org/fileadmin/user_upload/Presse_und_Medien/Publikationen/2015/mai/Handbook_for_Robustness_Validation_of_Semiconductor_Devices_in_Automotive_Applications__3rd_edition_/Robustness-Validation-Semiconductor-2015.pdf

[2] G. Breglio, N. Rinaldi, P. Spirito, "Thermal Mapping and 3D Numerical Simulation of New Cellular Power MOS Affected by Thermal Instability," Microelectronics Journal, Vol. 31, Issues 9-10, October 2000, pp 741-746