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POWER GaN

GaN – Moving Quickly into
Entirely New Markets



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GaN – Moving Quickly into Entirely New Markets

Gallium Nitride (GaN) based power devices are rapidly being adopted due to their ability to operate at frequencies and switching speeds beyond the capability of Silicon power devices. With discrete GaN devices capable of switching at slew rates up to 70 V/ns, the system performance is greatly impacted by aspects outside the active power devices, such as high speed gate drivers and printed circuit board layout. In this article, the latest family of high frequency enhancement mode Gallium Nitride power transistors (eGaN FETs) is presented for use in multi megahertz buck converters. These devices were designed to address high-frequency hard-switching power applications at higher voltages. **Alex Lidow, Johan Strydom and David Reusch, Efficient Power Conversion (EPC), El Segundo, USA**

The introduction of a new family of high performance enhancement mode eGaN FETs offers the potential to switch at higher frequencies and efficiency than possible with traditional Si MOSFET technology. Combined with an improved switching figure of merit and low parasitic packaging, the new devices also have optimized device pin-out to minimize parasitic PCB layout inductance to fully utilize the device's capability. Example buck converters operating at 10 MHz show experimental peak efficiencies of over 89 %. Although the results are impressive, there is still a significant loss component due to the current silicon gate driver. To fully utilize the capability of the new high frequency, reduced size eGaN FETs, a focused improvement in the gate driver structure is required, which in turn will allow a further increase in efficiency and switching frequency capability.

Hard Switching FOM

The impact of the miller charge (Q_{GD}),

which controls the voltage falling (t) and rising speed on the switching time is apparent and, for hard-switching applications, the use of $Q_{GD} \times R_{DS(ON)}$ as a switching figure of merit (FOM) is common. For cases at lower voltages and higher currents, the current-dependent term (Q_{GS2}) cannot be neglected. Q_{GS2} is the portion of the gate source charge between the device threshold voltage (V_{TH}) to the gate plateau voltage (V_{PL}), which controls the current rising (t) and falling speed. These different gate charge portions are shown on the right side of Figure 1.

The idealized turn-on period, shown on the left side in Figure 1, begins with an increase of gate drive voltage; when the gate voltage reaches the threshold voltage, the current through the device will begin to rise, being driven by the gate current (I_G). During the drain current rising period, the transistor encounters both current and voltage in the device, resulting in switching loss. For the current rising period, the

device parameter determining loss is Q_{GS2} . When the transistor current reaches the load current, the voltage across the device will begin to fall and more switching loss in the device will be incurred. For the voltage falling period, the device parameter determining loss is Q_{GD} . For the turn off switching losses, the same principles apply and minimizing the Q_{GD} and Q_{GS2} parameters will decrease switching losses incurred in a hard switching application. The overall switching loss is given by:

$$P_{SW} = \frac{V_{DS} \cdot I_{DS} \cdot (Q_{GD} + Q_{GS2})}{2 \cdot I_{DS}} + \frac{V_{DS} \cdot I_{DS} \cdot (Q_{GD} + Q_{GS2})}{2 \cdot I_{DS}}$$

Over the years, a number of different figures of merit (FOMs) have been proposed to simply reflect the in circuit performance capability of a given device technology in different applications. The above idealized hard-switching power equations forms the basis of the hard-switching FOM (FOM_{HS}) or $Q_{SW} \times R_{DS(ON)} = (Q_{GD} + Q_{GS2}) \times R_{DS(ON)}$ where Q_{SW} is the total switching gate charge during the

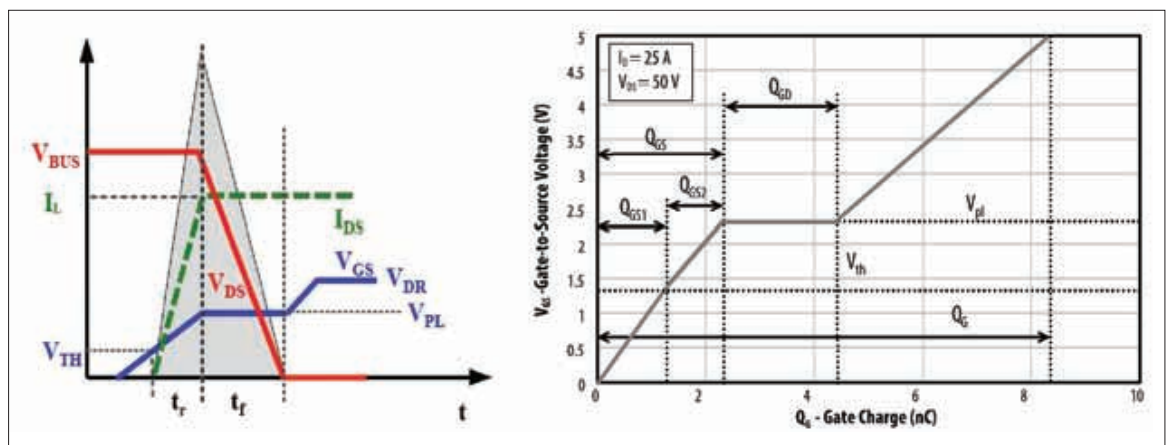


Figure 1: Idealized switching waveform used for calculating switching loss (left) and related FET charge diagram (right)

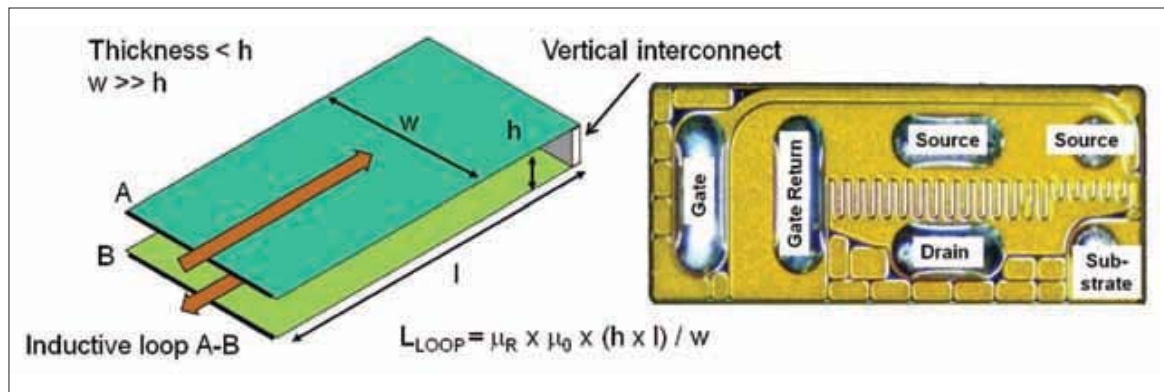


Figure 2: Optimum high frequency loop layout (left) and eGaN FET package showing pin-out (right)

hard switching interval.

These idealized switching waveforms rarely translate directly into actual in circuit performance results, as device and layout parasitics can significantly increase or even dominate switching losses. For a buck converter there are two major parasitic inductances that have a significant impact on converter performance: The common source inductance (L_s) is the source inductance shared by the drain-to-source power current path and gate driver loop; and the high frequency power loop (L_{LOOP}) is the power commutation loop and comprised of the parasitic inductance from the positive terminal of the input capacitance, through the top device, synchronous rectifier, ground loop, and back through the input capacitor. The common source inductance has been shown to be critical to performance because it directly impacts the switching speed of the devices.

The high frequency loop inductance, while not as penalizing to switching speeds as common source inductance, still negatively impacts switching performance. Another major drawback of high frequency loop inductance is the drain to source

voltage spike induced during the switching transition, shown on the right in Figure 1. This voltage spike reduces maximum usable device voltage and increases switching loss. To enable the high switching speed available from the low FOM of GaN devices, low parasitic packaging and PCB layout, and separation of the gate and power loops to minimize common source inductance are required.

On the packaging level, this requires a low inductance package, such as a ball grid array (BGA) or other similar wafer level chip scale package (WLCS). Furthermore, the common source inductance, being most critical parasitic, can be all but eliminated through the addition of a separate source terminal solely dedicated as a gate signal return path (gate return). To reduce power loop and gate loop reduction on a packaging level, the resultant board layout should be optimized. This is best achieved through generating large parallel conductors, where the loop current is flowing in opposite directions as shown in the left of Figure 2.

The current opposition results in magnetic flux cancellation outside the inductive loop, while minimizing the loop

length and vertical interconnect height can reduce the magnetic energy storage inside the loop. Lastly, the conductor width should be maximized to minimize the inductance per unit length. To support this optimized layout structure on a packaging level, the device terminals should be designed to be wide and laid-out perpendicular to the power loop current flow direction. The resultant EPC8000 series eGaN FET package is shown on the right of Figure 2.

To push the switching frequency higher requires lower charge devices, which in turn result in higher on-resistance, suitable for lower power per phase operation. An example of such a reduced charge EPC8004 device is shown on the left in Figure 3 and is compared to the smallest existing same voltage (40 V) rated device, the EPC2014 and shows about a seven times reduction in gate charge.

Another important aspect to consider is dv/dt immunity. An important metric for dv/dt immunity is the Miller ratio, which is an indicator of how susceptible gates are to turning back on at high dv/dt . For the EPC8000 series, the Miller ratio ($Q_{\text{GD}}/Q_{\text{GS1}}$) at half rated voltage has been reduced to

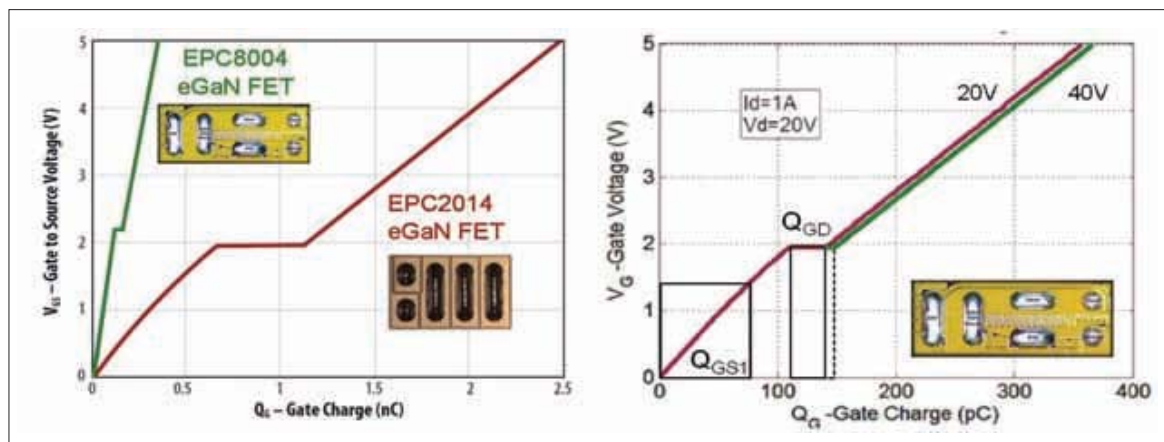


Figure 3: Gate charge diagrams, showing relative size of an EPC8004 device and existing EPC2014 device (left) and the EPC8004 device's inherent dv/dt immunity resulting from miller charge ratio ($Q_{\text{GD}}/Q_{\text{GS1}} < 1$) (right)

below 0.4, well below the theoretical requirement of one. The EPC8004 charge diagram, showing the Q_{GS1} and Q_{GD} intervals are shown on the right in Figure 3. It is important to note that the Miller ratio should remain below one, even up to full rated voltage, if dv/dt induced turn-on is to be avoided.

New Applications

GaN technology is enabling entirely new applications. In this article, we explore GaN penetration in four of these new applications, envelope tracking, wireless power transfer, LiDAR, and satellites. We also discuss GaN's penetration in the original target market, DC/DC conversion. The overall conclusion is that GaN is creating markets that are as large as the markets where they are displacing their Silicon ancestors.

Envelope Tracking: The concept of envelope tracking for radio frequency

amplifiers is not new. But the ever-increasing need for better base station efficiency and output power, as well as the need for improving RF power amplifier efficiency, is driving intense research and development in envelope tracking. RF power amplifiers are used to transmit all of our voice and data through satellites, base stations, and cell phones. Conventional RF power amplifiers operate at a fixed power level delivering maximum power whether or not the transmitter needs it. When envelope tracking is deployed in a RF power amplifier, the amplifier does not operate at a fixed power level, but precisely fits the power delivered to the amplifier's signal modulation needs. This is illustrated in Figure 4. Figure 5 shows a prototype board for envelope tracking applications.

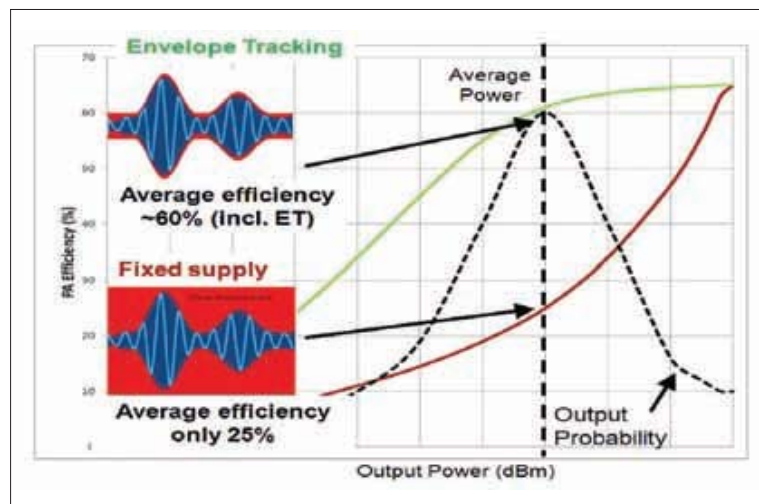
For many years designers have tried to make envelope tracking work using

expensive LDMOS transistors without general success. However, the power modulation required is enabled by enhancement-mode GaN transistors that can operate at the high voltages and switching speeds needed for efficient envelope tracking, which are just beyond the reach of Silicon.

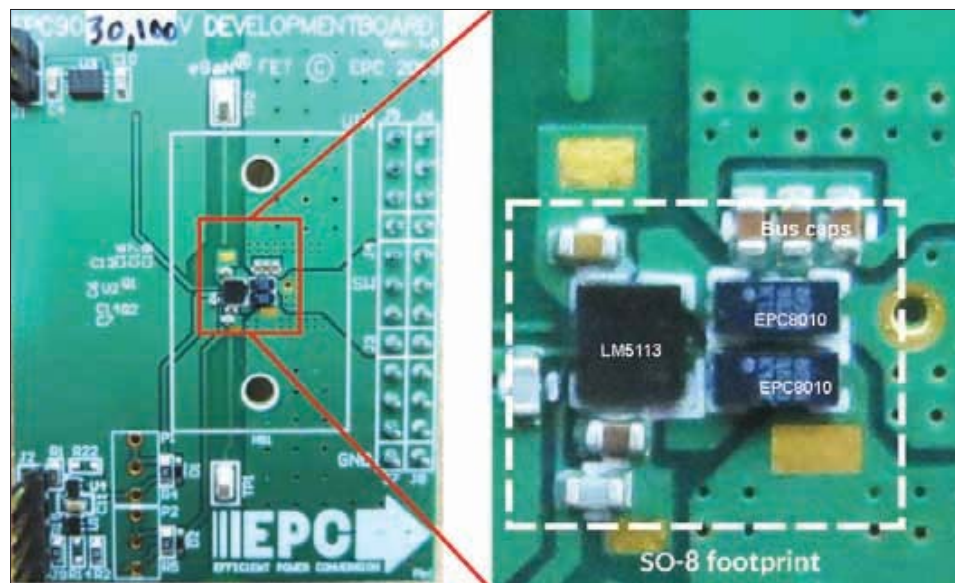
RF power amplifiers for 4G LTE technology have higher power requirements than previous generations and are the biggest beneficiary of envelope tracking. Today 4G LTE technology is just nine percent of the global wireless platform, but will eventually supersede earlier 3G networks in the world of data transmission. Envelope tracking can double the energy efficiency of RF power amplifiers for the 4G network with even greater gains probable for 5G.

Wireless Power: Wireless power applications are gaining popularity in many commodity products such as mobile phone chargers. Most of the wireless power solutions to date have focused on tight coupling with induction coil solutions operating at frequencies around 200 kHz. This is the Qi standard and its major drawbacks are conversion efficiency and its requirement for exact placement of the devices so that the transmit and receive coils are aligned.

Industry leaders including Qualcomm, Intel, Broadcom, Samsung, Delphi, and Witricity, have established a consortium (A4WP) for the development and commercialization of a recently selected high-frequency standard (6.78 MHz) for wireless power transmission (Highly Resonant Power Transfer). The fast switching capability of GaN transistors is ideal for highly resonant power transfer applications, particularly when high



ABOVE Figure 4: Schematic of fixed and envelope tracking power profile in a RF Power amplifier



LEFT Figure 5: Prototype board for envelope tracking applications

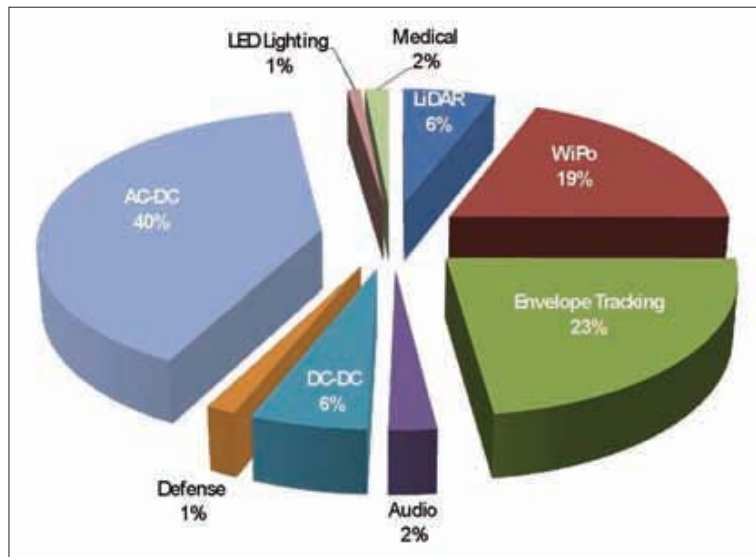


Figure 6: EPC's projected revenue by application in 2018

transfer efficiency and robust foreign object detection is desired.

Initial applications for wireless power transfer include cell phones, game controllers, laptop computers, tablets, and even electric vehicles that re-charge without being plugged in or having actual physical contact, merely proximity within a specified range is all that is required. The global wireless power transfer market CAGR is estimated at 55.5 %, and is forecasted to be \$15.1 billion by 2020. Demand for automotive wireless charging alone is expected to triple in the next eight years.

LiDAR: Light Detection and Ranging uses pulsed lasers to rapidly create a three dimensional image or map of a surrounding area. One of the earliest adopters of this technology is the Google Maps "driverless" cars. Today's enhancement-mode GaN transistors' higher frequency capability results in LiDAR systems with superior spacial resolution, faster response time, and greater accuracy. These device characteristics enable new and broader

applications such as real-time motion detection for video gaming, computers that respond to hand gestures as opposed to touch screens, and fully autonomous vehicles.

Rad Hard: Power converters used in harsh environments, such as space, high-altitude flight, or high-reliability military applications must be resistant to damage or malfunctions caused by radiation. Most electronic components require specialized design or manufacturing processes to reduce their susceptibility to radiation damage. For this reason, radiation-hardened devices tend to lag behind the most recent technology developments. Silicon-based power MOSFETs are no exception, and enhancement-mode GaN transistors have been shown to perform 40 times better electrically while being able to withstand 10 times the radiation. In addition, since commercial grade GaN power transistors are intrinsically radiation-hardened, they open the door to major cost savings in communications and research satellites. It is anticipated

that the overall \$ 200 billion global space market in 2023 will drive a greater than \$100 million Rad Hard transistor market that will be dominated by GaN transistors.

Datacom DC/DC: The hunger for more efficiency continues to be a driving factor in most electronics – especially in applications such as server farms and centralized telecommunications centers. When compared with MOSFETs, GaN transistors are significantly more efficient. The lower power losses translate into products with higher output, improved power density, and increased efficiency. This translates into lower energy consumption and reduced electric bills.

More to Come

We expect GaN devices to re-enact the famous Moore's Law in the coming years, expanding beyond discrete transistors into a variety of integrated circuits with high performance, low cost, and very high value. This drives a "virtuous cycle" where each subsequent generation has increasingly higher performance and lower cost, thus enabling even more new, unforeseen applications.

GaN is facing a period of very rapid growth. This growth is coming from both the replacement of lower performing (and soon to be higher relative cost) Silicon devices and from emerging applications that are enabled by GaN's performance. Figure 6 shows EPC's forecasted 2018 revenue breakout for its eGaN FET product line. Emerging applications, LiDAR, envelope tracking, and wireless power transfer, represent 48% of these projected revenues – applications that are in their infancy today, but are exploding on the market.

Literature

'Multi Megahertz Buck Converters using eGaN® FETs for Envelope Tracking'
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