Extreme GaN – What Happens When eGaN® FETs are Exposed to Voltage and Current Levels Well Above Data Sheet Limits

Recently, Efficient Power Conversion (EPC) did a series of tests to take eGaN FETs beyond their data sheet limits to quantify the effects of large amounts of overstress voltage and current and the results are published here for the first time.

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Efficient Power Conversion

GaN transistors, and more recently integrated circuits, have been in mass production for over a decade [1] with several manufacturers reporting tens of millions of units shipped with billions of hours in actual end-use applications. The track record has been extraordinarily successful, and one of the key reasons is that GaN devices are far more rugged than their silicon MOSFET ancestors [2].

Beyond Data Sheet Voltage Limits

EPC tested several fifth generation 100 V-rated EPC2045 eGaN FETs with up to 150 V drain-source bias under hard-switching conditions described in [2]. Figure 1 shows the normalized $R_{DS(on)}$ of the EPC2045 devices being hard-switched at voltages ranging from 60 V to 150 V. At lower drain voltages within datasheet limits, the model predicts no or small $R_{DS(on)}$ increase that grows linearly with the log(t). At extreme voltages, over datasheet limits, the growth begins to deviate from the linear dependence on log(t). In this figure the $R_{DS(on)}$ is extrapolated using methods described in [2] to project out to 10-year operation. These projections, superimposed on the actual data, are derived using the physics-based models based on hot carrier injection and trapping that were developed in [2].

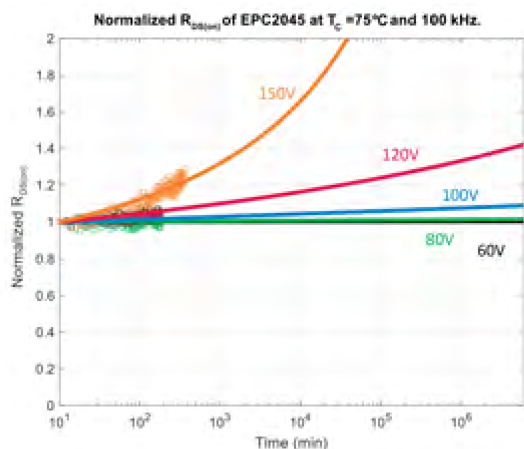

Figure 1: Measured and normalized values for $R_{DS(on)}$ of a 100 V-rated EPC2045 at 75°C under various hard-switched voltages. Solid lines are the predicted results under these conditions using the hot carrier injection trapping model of [2].

Figure 2 shows the impact of temperature on the rate of increase in $R_{DS(on)}$ with the predicted values from the model superimposed on the plot. Model agreement is good and, as previously reported, there is a reduction in trapping with increasing temperature, so it is expected that $R_{DS(on)}$ would shift less at higher temperatures. It is important to note that the devices do not fail abruptly because of this extreme voltage over-stress.

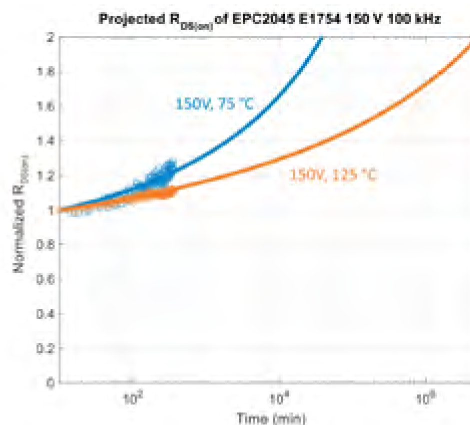

Figure 2: Measured and normalized values for $R_{DS(on)}$ of a 100 V-rated EPC2045 hard-switched at 150 V at two different temperatures. Solid lines are the predicted results under these conditions using the hot carrier injection trapping model of [2].

Beyond Data Sheet Current Limits

EPC tested several parts to over 500,000 cycles under short-circuit conditions that caused device currents that were about four times the maximum rated pulse current listed on their data sheets. In the test setup, gate bias of either 5 or 6 VDC was applied to the device under test (DUT) gate. Drain bias was set at 10 VDC and a 60 mF capacitor was connected across the drain supply. A low $R_{DS(on)}$ high side transistor in series with the DUT controlled the otherwise unlimited flow of current. The control transistor was then pulsed with 5-μs pulses at 1 Hz to give the channel time to re-equilibrate. Table 1 shows the various types of devices tested, their data sheet rating for maximum pulsed current, and the amount of short-circuit current that pulsed through the device during each cycle at the start of the test.

Table 2 shows the various key device parameters for a representative device, the EPC2051, a 1.1 mm^2 device from the fifth-generation family of eGaN FETs. Even under these extreme conditions of 150 A pulses that are four times the data sheet maximum ratings, all electrical characteristics remained within data sheet specifications. There was, however, a small reduction in the amount of short circuit current "consumed" by the DUT over time, consistent with the small increase in V_{TH}.

Device	Type	Datasheet Pulsed (A)	V_{GS}	Mean (A)	Sigma (A)
EPC2203	80V AEC Gen4	17	5	63	4.3
			6	79	4.6
EPC2212	100V AEC Gen4	75	5	226	3.9
			6	292	6.4
EPC2051	100V Gen5	37	5	124	1.8
			6	158	2.4
EPC2052	100V Gen5	74	5	268	2.9
			6	297	4.0
EPC2207	200V Gen5	54	5	180	8.6
			6	241	9.1

Table 1: Devices tested under extreme pulsed short circuit current, typically four times the maximum data sheet limit.

EPC2051	t = 0	100k Pulses	500k Pulses	Post 10 min. 175 °C Anneal
V_{TH} (V)	1.8	2.0	2.1	1.8
I_{GSS} (uA)	11	33	55	23
I_{DSS} (uA)	7	5.5	5.1	5.6
R_{DSON} (mΩ)	22	22.3	22.3	22
$I_{short\ circuit}$	152	141	135	150

Table 2: Key device parameters for EPC2051 at the start of pulse testing, after 100 k pulses, after 500 k pulses, and after a 175°C, 10 minute anneal. Device parameters stayed within data sheet limits at all times.

After this 500k pulse sequence, this part underwent an unbiased 10 minute anneal at 175°C. As can be seen in the right-hand column of Table 2, the electrical parameters and short-circuit current recovered to near their values before being subjected to repetitive pulse stresses. This recovery indicates that no permanent damage occurred from repetitive high-current pulses.

How to Use This New Information

EPC does not recommend using the information in this document instead of the parameters and maximum conditions listed in the product data sheets. EPC is testing under extreme conditions to better understand and characterize intrinsic failure mechanisms that will lead to better performance and reliability in future generations of eGaN transistors and integrated circuits. EPC is continuing these tests on large, statistically significant sample sizes and based upon results may increase the absolute maximum limits on data sheets of existing products in the future.

Conclusions

GaN is an amazing new semiconductor material with especially high potential in power conversion applications. In the eleven years since they first went into mass production, eGaN FETs have demonstrated field reliability well in excess of the aging power MOSFET [2] for two key reasons; (1) eGaN devices are designed using a test-to-fail methodology [3] that pinpoints intrinsic failure mechanisms that can be attenuated or eliminated in subsequent technology generations, and (2) wide bandgap devices, in general, are less susceptible to degradation due to temperature. In fact, the intrinsic failure mechanisms for gate-voltage stress and drain-source voltage stress have a negative temperature coefficient making operation under extreme conditions for long periods of time a practical new tool for power system design engineers.

References

[1] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, GaN Transistors for Efficient Power Conversion. Third Edition, Wiley, ISBN 978-1-119-59414-7.

[2] Alejandro Pozo, Shengke Zhang, Gordon Stecklein, Ricardo Garcia, John Glaser, Zhikai Tang, and Robert Strittmatter, "EPC eGaN Device Reliability Testing: Phase 12," Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/Reliability%20Report%20Phase%2012.pdf

[3] A. Lidow, R. Strittmatter, S. Zhang, and A. Pozo, "Intrinsic Failure Mechanisms in GaN-on-Si Power Transistors," IEEE Power Electronics Magazine, December 2020.

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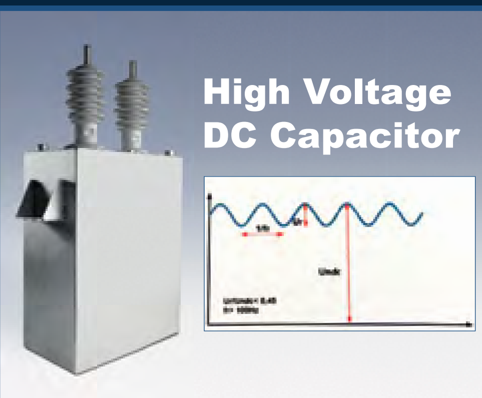

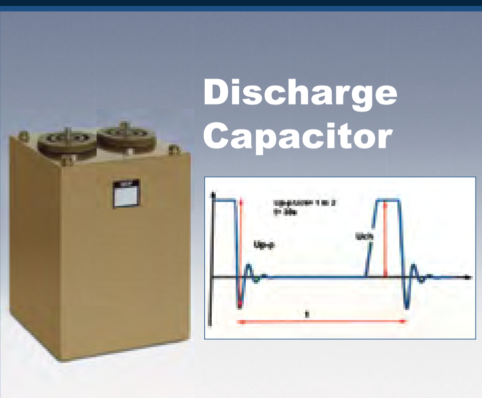

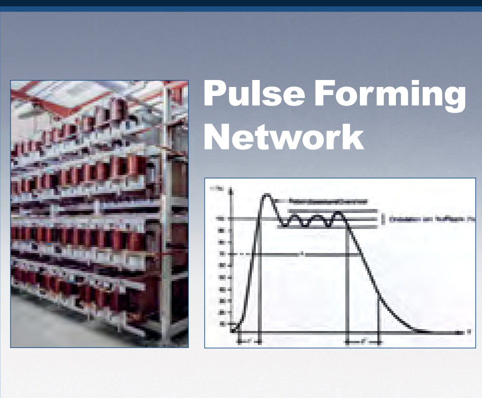

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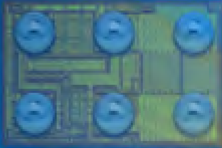

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