Driving eGaN™ FETs

Both gate and Miller capacitances are significantly lower

As enhancement mode gallium-nitride-on-silicon transistors (eGaN™) gain wider acceptance as the successor to the venerable - but aged - power MOSFET, designers have been able to improve power conversion efficiency, size, and cost. eGaN FETs, however, are based on a relatively new and immature technology with limited design infrastructure to quickly design and implement products.

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In this article we discuss several key considerations for designers wanting to quickly get eGaN-based systems to market.

Gate drive requirements

To determine the gate drive circuit requirements, and how they differ from silicon MOSFET drivers, it is necessary to compare their device parameters (see table 1). The three most important parameters for eGaN FETs are, (1) the maximum allowable voltage, (2) the threshold voltage and, (3) the "body diode" voltage drop. The maximum allowable gate-source voltage of 6V is low in comparison with silicon. Secondly, the threshold is also low compared to most power MOSFETs, but does not suffer from as strong a negative temperature coefficient. Thirdly, the "body diode" forward drop can be a volt higher than comparable silicon MOSFETs.

FET type	Typical 100 V Silicon	100 V eGaN™
Maximum gate-source voltage	+/-20 V	+6 V /-5 V
Reverse 'body diode' voltage	~1 V	~1.5-2.5 V
Gate threshold	2 V – 4 V	0.7 V - 2.5 V
dV/dt capacitance (Miller) ratio $Q_{GD(50\,V)}/Q_{GS(VTH)}$	0.5-0.8	1.1
Internal gate resistance	>1 Ω	<0.6 Ω
Change in $R_{DS(ON)}$ from 25°C to 125°C	>+70%	<+50%
Change in V_{TH} from 25°C to 125°C	-33%	-3%
Gate to source leakage	few nA	few mA
Body diode reverse recovery charge	high	none
Avalanche capable	Yes	not rated

Table 1: Comparison between 100V Si MOSFETs and eGaN™ FETs

Gate pull-down resistance

A great advantage offered by eGaN FETS is their fast switching speed. However, the higher di/dts and dV/dts that accompany this not only require a layout with less parasitic capacitance, resistance, and inductance, but also cause some new considerations for the gate driver. Let's consider a half- bridge with a high dV/dt turn-on of a complementary device as shown in Figure 1. The 'Miller' charge current flows from the drain (switching node) through C_{GD} and C_{GS} to source as well as through C_{GD} to R_G (internal gate resistance) and R_{Sink} (gate driver sink resistance) to source. The requirement for avoiding dV/dt (Miller) turn-on is given by:

$$C_{GD} \times dV/dt \times (R_G + R_{Sink}) \times (1 - e^{-dt/\alpha}) < V_{TH}$$

Where α is the passive network time constant $(R_G + R_{Sink}) \times (C_{GD} + C_{GS})$ and dt is the dV/dt switching time. Thus to avoid Miller turn-on, it is necessary to limit the total resistance path (internal gate resistance R_G and external gate drive sink resistance R_{Sink}) between the device gate and its source. To be safe, a gate drive pull-down resistance of 0.5Ω or less is recommended for higher voltage eGaN devices.

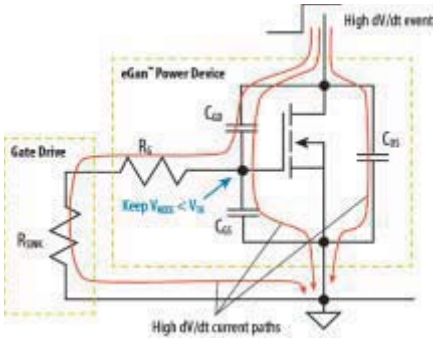

Figure 1: Effect of dV/dt and requirements for avoiding Miller turn-on

Gate pull-up resistance

Because the total Miller charge (Q_{GD}) is much lower for an eGaN FET than for a similar on-resistance power MOSFET, it is possible to turn on much faster. As stated above, too high of a dV/dt can actually reduce efficiency by creating shoot-through during the 'hard' switching transition. It would therefore be advisable to have the ability to adjust the gate drive pull-up resistance to minimize transition time without inducing other unwanted losses. This also allows adjustment of the switch node voltage overshoot and ringing for improved EMI. The simplest solution is to split the gate pull-up and pull-down connections in driver and allow the insertion of a discrete resistor.

Gate drive dead-time matching

eGaN FET reverse bias or "body diode" operation has the benefit of no reverse-recovery losses. This advantage, however, can be offset by the higher "body diode" forward voltage drop. The diode conduction losses can be significant, especially at low voltages and high frequencies. Unlike diode reverse recovery losses; these conduction losses can be minimized through proper dead-time management that minimizes the "body diode" conduction interval.

Silicon gate drivers / controllers tend to have effective minimum dead-time around 20ns (+/-10ns) for low voltages, increasing with bus voltage to around 400ns (+/- 100ns) for 600V drivers. With eGaN FETs, both gate and Miller capacitances are significantly lower than equivalent silicon devices, leading to shorter delay and switching times. These allow for much tighter dead-time control which would be beneficial in reducing "body diode" conduction loss. A reduction of dead-time between half and one-fourth the above values, with a similar reduction in the variation, would be preferred.

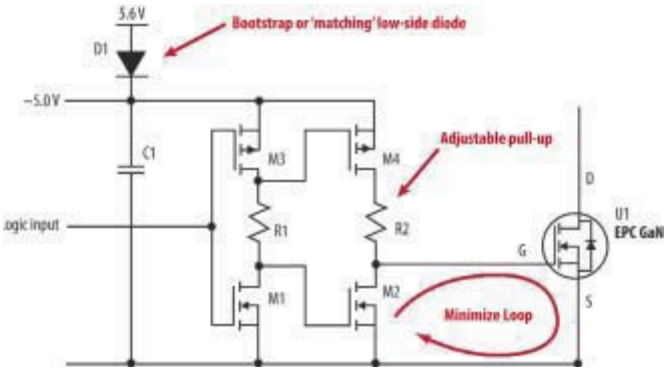

Figure 2: Discrete gate-driver solution showing method for complementary high-side and low-side supply voltage matching.

Gate drive supply regulation

The current maximum gate voltage limitation of 6V on the eGaN FET restricts the allowable gate drive supply range, and requires at least some form of supply regulation – especially on the high side. A post bootstrap diode regulator eliminates the effect of changes in the sup-

ply due to the dead time variation with a higher "body diode" voltage drop. For complementary driven half-bridge with minimal dead-time, a diode matching network shown in Figure 2 can be used.

Layout considerations

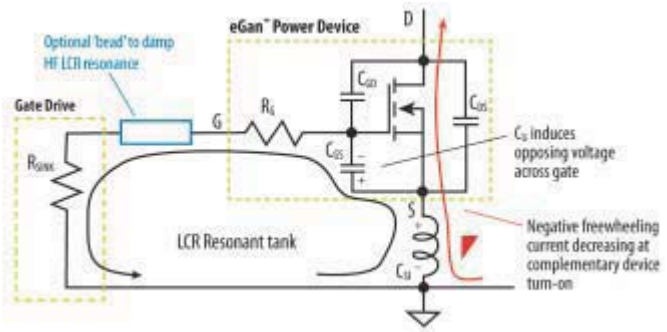

Figure 3: Equivalent circuit showing di/dt effect of 'hard' turn-on of complementary device

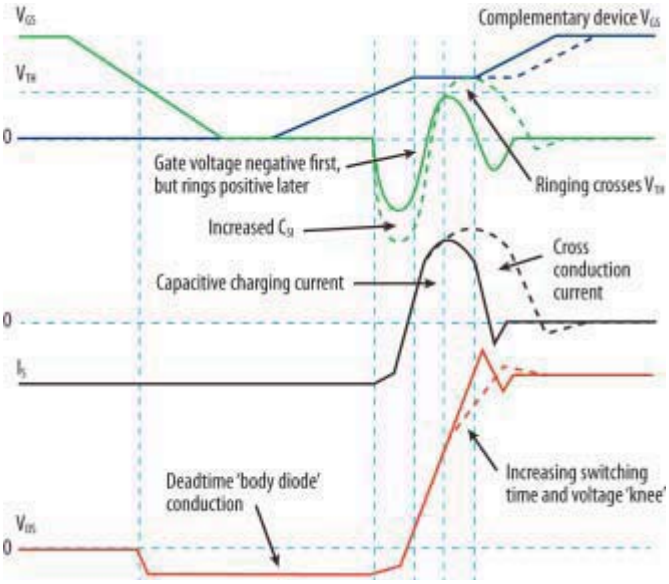

Figure 4: Conceptual waveforms for circuit in Figure 2 during 'hard' turn-on of complementary device showing effect of CSI ringing

Gate drive loop inductance

The maximum allowable gate voltage of 6V is only one volt above the recommended 5V drive voltage. This requires an accurate gate drive supply, as well as a limited inductance between the eGaN device and gate driver as the inductance can cause an overshoot on the gate.

Effect of common source inductance (CSI)

The addition of CSI effectively reduces efficiency by inducing a voltage across the CSI that opposes the gate drive voltage, increasing switching times. It is therefore critical to minimize common source inductance for optimum switching performance. Increase in CSI will actually decrease the possibility of Miller turn-on if one accepts its increased switching loss. This is because at the 'hard' turn-on of the complementary device, the current commutation di/dt across the CSI induces a negative voltage across the gate to help keep the device off during part of the voltage transition. However, CSI, gate capacitance, and gate drive pull-down loop now form an LCR resonance that must be damped to avoid an equivalent positive voltage ringing across the gate. This ringing could turn the device on again near the end, or even after the voltage transition. Although increasing the gate drive sink resistance can help damp this resonance, the addition of a ferrite bead that is resistive at the resonant frequency can achieve the same result with less increase in Miller turn-on sensitivity (Figure 3 shows the equivalent circuit and Figure 4 the conceptual waveforms). In short, CSI is much more important to eGaN FETs than silicon due to higher di/dt and dV/dt and should be minimized through careful layout.

Suggested Layout

Given the considerations listed above, it is possible to develop a recommended layout. The layout presented depicts a half-bridge configuration, but following the above requirements can be applied to other applications as well

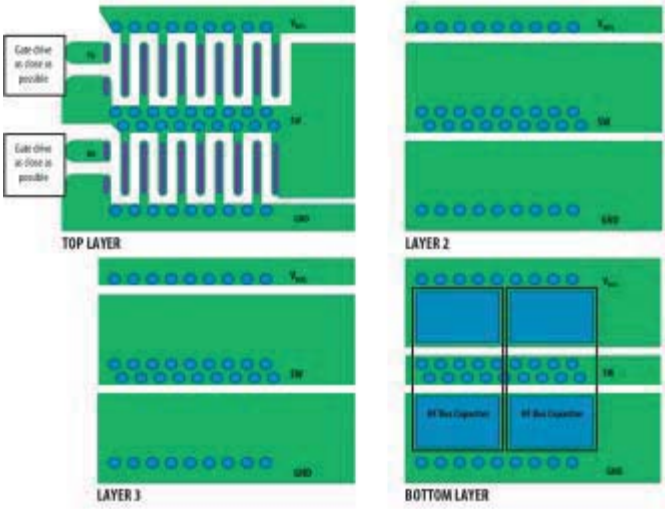

Figure 5: Suggested half bridge layout using 4-layer PCB

A simple four layer PCB is presented in Figure 5. It should be noted that the copper thickness must be maximized to limit resistive losses and improve thermal spreading (2 oz copper on outer layers is recommended). In this example the source connection of each part is brought underneath to act as shield (especially under the gate area) and minimize additional parasitic C_{GD}. The gate return connection is made on the smaller source pad to separate gate return current and power source current paths,– thus minimizing CSI.

Summary

EPC's eGaN FETs give the engineer a new spectrum of performance compared with silicon power MOSFETs. In order to extract full advantage from this new, game-changing technology, designers must learn some new techniques on how to design cost-effective eGaN drive circuitry that works on a cost-effective PCB.

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