Performance Evaluation of Enhancement-Mode GaN Transistors in Class-D and Class-E Wireless Power Transfer Systems

The popularity of wireless energy transfer has increased over the last few years and in particular for applications targeting portable device charging. In this article, the focus will be on loosely coupled coils, highly-resonant wireless solutions suitable for the A4WP [1] standard operating at either 6.78 MHz or 13.56 MHz unlicensed Industrial, Scientific and Medical (ISM) [2] bands.

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Many of the wireless energy transfer solutions have targeted portable device charging that require features such as low profile, high efficiency, robustness to changing operating conditions and, in some cases, light weight. These requirements translate into designs that need to be efficient and able to operate without a bulky heatsink. Furthermore the design must be able to operate over a wide range of coupling and load variations. There are a few amplifier topologies that can be considered such as the voltage mode class-D, current mode class-D and class-E. The class-E has become the choice for many wireless energy solutions as it can operate with very high conversion efficiency.

eGaN® FETs have been previously demonstrated in a wireless energy transfer application using a voltage mode class-D topology [3, 4] and showed superior performance when compared to a system utilizing equivalent MOSFETs by as much as four percentage points higher peak conversion efficiency. At output power levels above 12W, the design required a heatsink to provide additional cooling to the switching devices and gate driver. In addition, the traditional voltage mode class-D topology requires that the resonant coils be operated above resonance to appear inductive to the amplifier. This is needed to allow the amplifier to operate in the ZVS mode and overcome the C_{OSS} of the devices that would otherwise lead to high losses in the devices as opposed to being operated in the ZCS mode. Operating the coils above resonance comes at the cost of coil transfer efficiency and high losses associated with the matching inductor due to the presence of reactive energy.

eGaN FETs have also been demonstrated in a class-E topology by Chen et al [5] with up to 25.6 W power delivered to the load while operating at 13.56 MHz. The wireless energy transfer system was operated with very high load resistance (350 Ω) which ensured a high Q resonance, and the system efficiency was measured at 73.4% including gate power consumption. The shunt capacitor in that example was completely embedded in the EPC1010 device used in the experimental setup, thereby keeping the component count low.

Coil and Load simplification

To facilitate the discussion and design evaluation, the coil set, device side matching, rectifier and load will be reduced to a single reactive element (Z_{load}) as shown in figure 1.

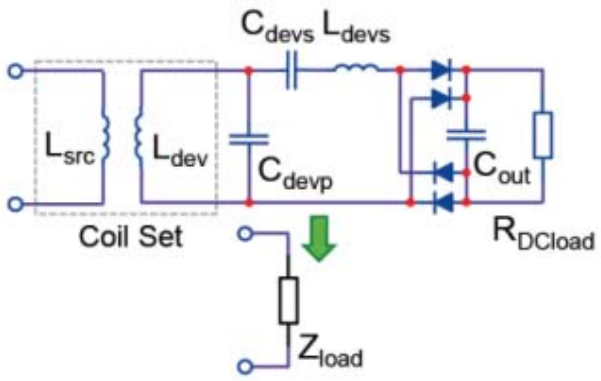

Figure 1: Single element simplification of the entire coil system and DC load.

All subsequent design and discussion will make use of this single element, which allows for equal comparison between various topologies under equivalent load conditions.

Class-E Wireless Energy Transfer

The ideal single ended class-E circuit for a wireless energy transfer system is shown in figure 2. In this setup C_s is used to resonate out the reactive component of Z_{load} to yield only the real portion of the coil circuit to the amplifier.

The design and operation of the class-E amplifier is well documented in [6, 7, and 8]. The matching network is designed for a specific load impedance to establish the necessary conditions for zero voltage and current switching.

Adopting the class-E topology for wireless energy transfer requires detailed knowledge of the coils and how the load affects the impedance seen by the amplifier. The design is further complicated by variations in load power demand and coupling between the source and device coils. This can introduce variations in the impedance seen by the amplifier that are not typically present in communication based designs. These variations and impact on the performance of the amplifier need to be considered in the design of the class-E, which is particularly prone to high device losses if the variations fall outside specific parameters. Changes in DC load resistance can shift the tuned reactance of Z_{load} to be either capacitive or inductive depending on what DC load resistance value was used to tune the coil set.

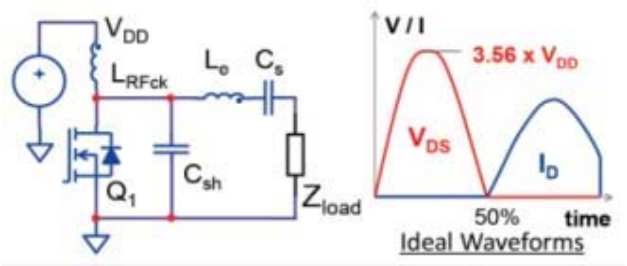

Figure 2: Class-E amplifier with ideal waveforms

Design of the class-E amplifier

A wireless class-E amplifier was designed based on a Q_L factor of infinity [9]. The coil spacing and load was fixed to eliminate source impedance variation. The design was made to deliver 30 W into the following coil: Coil impedance Z_{load} for a 20.2 Ω DC load = 14.7 Ω and in series with a 3.1 µH. The coil was tuned to 6.78 MHz using a series capacitor (C_s) of 178 pF which results in only the real 14.7 Ω being presented to the amplifier.

To deliver 30 W into 14.7 Ω, the class-E amplifier needs to operate from a supply of 31 V, with a peak voltage across the shunt capacitor (C_{sh}) and the drain-to-source (V_{DS}) of the device of 110 V. A shunt capacitance of 293 pF was needed for this design, and any device selected must have a charge equivalent C_{OSSQ} that is equal to, or lower in value. The charge equivalent capacitance of C_{OSSQ} must be determined from two parameters; (1) the C_{OSS} as function of drain-to-source voltage of the device selected and (2) the RMS voltage to which the device will be exposed. For this design the RMS voltage was 78 V. Selecting the EPC2012 [10], with V_{DS} rating of 200 V, the charge equivalent C_{OSS} at 78 V was 126 pF, thus an additional capacitance was required to complete the design of 167 pF which will be C_{sh}. Finally, the extra inductance L_e calculates to 390 nH.

The choice of RF choke is based on the required ripple specification and minimal impedance impact to the circuit. In this design example a value of 150 µH was chosen and a smaller value can also be used without degradation in performance.

To summarize the Class-E design:
C_s = 178 pF
L_e = 390 nH
C_{sh} = 167 pF
L_{RFck} = 150 µH
Q1 = EPC2012

An analysis of the design predicts device losses to be around 250mW under full load conditions. This is low enough to operate without the need for a heatsink.

Experimental performance of the Class-E System

An experimental class-E amplifier was built that connects to the WiTricity coil set [11] and rectifier with load board set to R_{DCload} = 20.2 Ω. The amplifier board is shown in figure 3 (without the coil set). An adapter board was designed to interface the extra inductance (L_e) with the coil set. This allowed the same coil set to be used with other amplifiers without the need to retune and is also shown in figure 3.

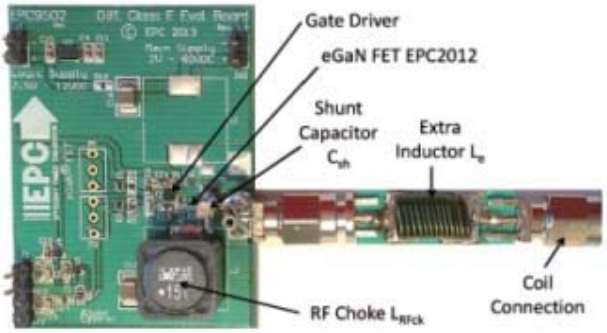

Figure 3: Class-E eGaN FET experimental setup

To properly evaluate the performance of the class-E amplifier, given that the C_{OSS} of the device was used in the matching circuit, the power required for the gate must also be included in the performance evaluation. This further allows for a fair comparison against a MOSFET version of the amplifier.

The eGaN FET experimental board efficiency was measured as function of output power by varying the input voltage to the amplifier and is shown in figure 4. The board was operated at 6.78 MHz during this test.

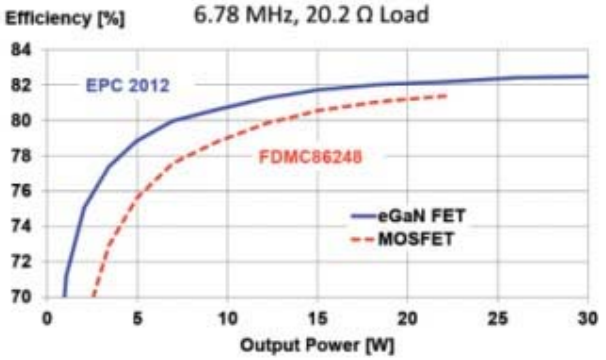

Figure 4: Class-E efficiency results

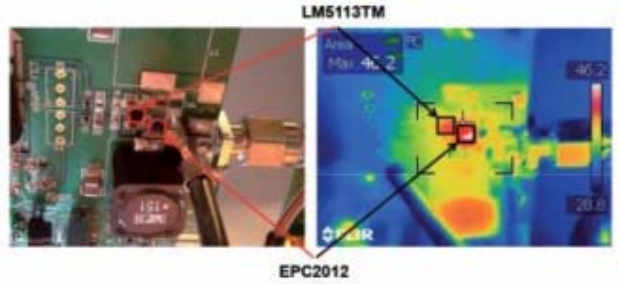

Figure 5: Class-E Thermal performance with R_{DCload} = 20.2 Ω, V_{in} = 28 V, P_{out} = 30 W.

Figure 5 shows the thermal performance of the eGaN FETs operating in the experimental circuit delivering 30 W into a 20.2 Ω load.

Both the gate driver and eGaN FET temperature remain well below 50°C when operating in an ambient temperature of 25°C. No heatsink or forced air cooling was used for this test.

There have been many questions about how to compare the performance between a class-E amplifier utilizing an eGaN FET or MOSFET, given that C_{OSS} is included in the matching network. The first step to answer that question is to look at the soft switching figure of merit (FoM_{SS}) [12]. Figure 6 shows the soft switching figure of merit comparison between an EPC2012 [10] eGaN FET and FDMC86248 [13] MOSFET. The comparison is made for two gate voltage operating conditions for the MOSFET, 6 V and 10 V. This allows a comparison in performance for a circuit that uses the same gate driver for both the eGaN FET and MOSFET. From figure 6 is can be seen that the gate charge is significantly lower for the eGaN FET, which is an important consideration for low power converters as gate power is a significant portion of the total power processed by the amplifier.

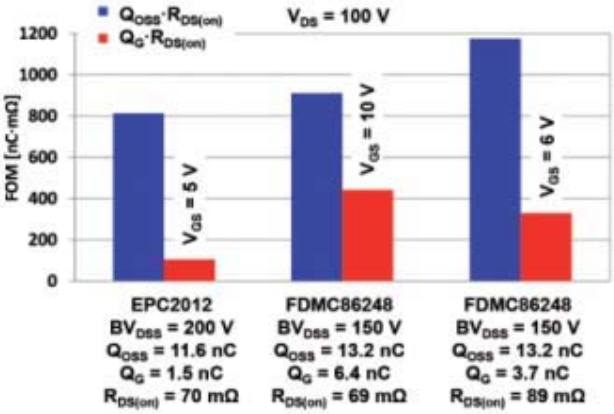

Figure 6: Soft Switching Figure of Merit comparison for the class-E Amplifier

Comparing the output charge, the difference is smaller. However, the eGaN FET is still lower for the same $R_{DS(on)}$ and has a higher voltage rating than the MOSFET. This allows the class-E amplifier to be operated at a higher voltage than the MOSFET, with resulting higher output power. Operating the MOSFET based amplifier with a gate voltage of 6 V yields lower performance than at 10 V gate despite the halving of the gate charge figure of merit. Figure 4 shows the performance of the MOSFET based class-E amplifier operating with a 10 V gate.

Class-E sensitivity to load variation

Loosely coupled wireless energy transfer systems operate with large load variations as load power demand fluctuates and coupling varies between the source and device units. These variations introduce changes in the coil impedance (Z_{load}) as seen by the amplifier, which when tuned at a specific load condition can shift from inductive to capacitive in addition to introducing large changes in the resistance component of Z_{load}. These changes must be understood and accounted for when designing wireless power systems. Most important is the impact these changes have on the power dissipation of the devices.

The full power circuit of class-E system was simulated in LTspice and the DC load resistance (R_{DCload}) was varied while maintaining a fixed supply voltage to the amplifier. The simulation results were first compared with the experimental results and found to correlate well.

Figure 7 shows the simulation results for the losses in the eGaN FET as function of the DC load resistance. It can be seen that below the design point (20.2 Ω for this example), the losses in the FET increase rapidly with decreasing load resistance. This condition equates to an increase in load current demand by the device. Also shown in figure 7 is the corresponding output power as function of DC load resistance.

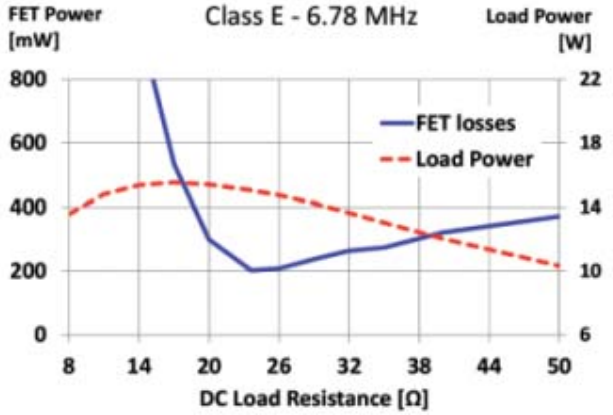

Figure 7: Simulated FET power losses and load power as function of DC load resistance.

ZVS Voltage Mode Class-D Wireless Energy Transfer

In this section we introduce a zero voltage switching (ZVS) variation of the traditional voltage mode class-D. The ideal voltage mode class-D amplifier comprises a half bridge topology that drives the load Z_{load}. Since the load must be tuned by C_s, this capacitor also serves to block the average DC voltage present on the output of the amplifier. The voltage mode class-D incurs high losses due to the output capacitances of the devices and therefore must be operated with the load tuned to be slightly inductive. The output inductance then serves to self-commutate the output voltage, providing the conditions necessary for zero voltage switching. However, tuning the load to appear inductive causes the coil set resonant frequency to shift with a drop in coil transmission efficiency due to the increase in circulating energy between the coil and the amplifier. A ZVS variation to the traditional voltage mode class-D amplifier is shown in figure 8. In this configuration a ZVS tank circuit is added to the output of the amplifier which operates as a no-load buck converter.

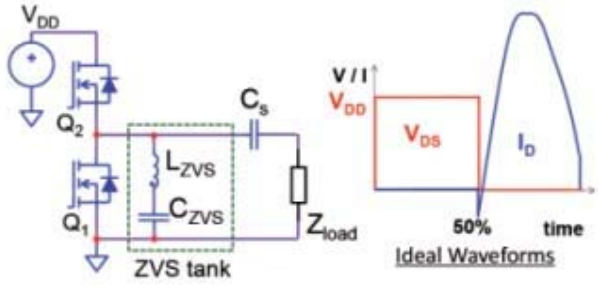

Figure 8: ZVS Class-D amplifier with ideal waveforms

The ZVS tank circuit is not operated at resonance, and only provides the necessary negative device current for self-commutation of the output voltage at turn off. The capacitance C_{ZVS} is chosen to have a very small ripple voltage component and is typically around 1 µF for many wireless energy transfer applications. The value of the inductance L_{ZVS} depends on the operating voltage V_{DD}, C_{OSS} of the devices, the transition voltage slew rate, and the immunity required for shifts in the tuned load (C_s + Z_{load}) impedance and can be calculated using the following equation:

$$L_{ZVS} = \frac{\Delta t_{vt}}{8 \cdot f_{sw} \cdot C_{OSSQ}} \qquad (1)$$

Where:

Δt_{vt} = voltage transition time [s]
f_{sw} = Operating frequency [Hz]
C_{OSSQ} = Charge equivalent device output capacitance [F]

Note that the supply voltage V_{DD} is not present in the equation as it is already accounted for by the voltage transition time, as the voltage doubles so does the transition time. To add immunity margin for shifts in load impedance, the value of L_{ZVS} can be decreased to increase the current at turn off of the devices. Typical voltage transition times range from 2 ns through 15 ns, and are application dependent. The transition time should also be kept as low as possible to ensure sufficient voltage for the load.

Design of the ZVS voltage mode class-D amplifier

A ZVS voltage mode class-D wireless amplifier was designed for the same coil set as for the class-E example. The design was made to deliver 30 W into the following coil: Coil impedance Z_{load} for a 23.6 Ω DC load = 12.6 Ω, and is in series with a 3.1 µH. The coil is tuned to 6.78 MHz using a series capacitor (C_s) of 176 pF which results in only the real 12.6 Ω being presented to the amplifier.

To deliver 30 W into 12.6 Ω, the ZVS class-D amplifier needs to operate from a supply of 40 V. The switching devices need to have a drain-to-source (V_{DS}) voltage rating, with margin, of at least 50 V. The charge equivalent capacitance of C_{OSSQ} must be determined from two parameters; (1) the C_{OSS} as function of drain-to-source voltage of the device selected, and (2) the supply voltage to which the device will be exposed. For this demonstration design, the EPC2007 [15], with V_{DS} rating of 100 V was selected, with charge equivalent C_{OSSQ} at 40 V of 223 pF. To correctly calculate the inductance, the output device capacitances of both devices need to be added together. For a transition time around 7.3 ns, and using equation 1, an inductance of 300 nH for the ZVS tank circuit was calculated.

To summarize the ZVS Class-D design:

C_s = 176 pF
L_{ZVS} = 300 nH
C_{ZVS} = 1 µF
Q1, Q2 = EPC2007

An analysis of the design predicts device loss to be around 170 mW per device under full load conditions, which is low enough to operate without the need for a heat-sink.

Experimental performance of the ZVS Class-D System

An experimental ZVS class-D amplifier was built that connects to the same coil, rectifier with load board as used in the class-E example and was set to R_{DCload} = 23.6 Ω. The amplifier board is shown in figure 9 (without the coil set).

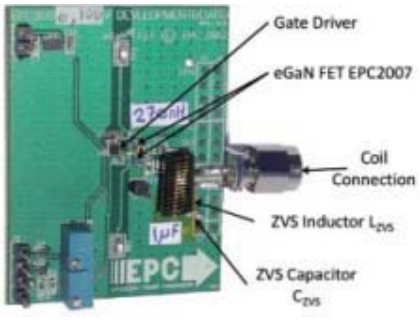

Figure 9: ZVS Class-D experimental setup

The eGaN FET experimental board efficiency was measured as a function of output power by varying the input voltage to the amplifier, and is shown in figure 10.

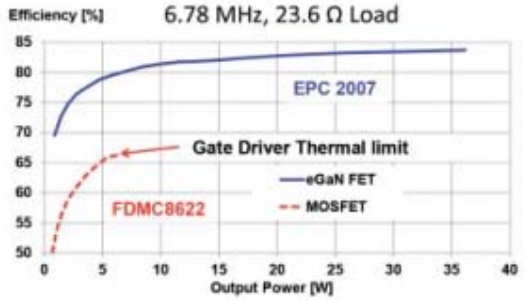

Figure 10: ZVS Class-D results

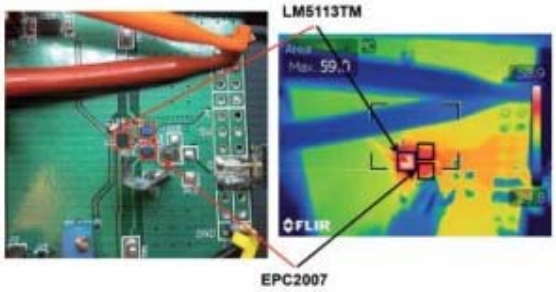

Figure 11: ZVS Class-D thermal performance with R_{DCload} = 35 Ω, V_{in} = 42 V, P_{out} = 35 W.

Figure 11 shows the thermal performance of the eGaN FETs operating in the experimental circuit delivering 35 W into a 35 Ω load.

Both the gate driver and FET temperature are below 60°C when operating in an ambient temperature of 25°C. No heatsink or forced air cooling was used for this test. It is notable that the gate driver IC is the hottest component, which is in part due to the reverse recovery of the internal bootstrap circuit diode and the parasitic capacitance between the switch-node and ground within the gate driver [14]. These factors introduce additional losses and can be mitigated by design or improvements in future gate drivers that are designed to operate at higher frequencies.

Again we compare the performance between an eGaN FET and MOSFET, this time in the ZVS class-D amplifier. In this example it was important to closely match the Q_{OSS} rather than the $R_{DS(on)}$ as it affects the voltage transition time and hence the RMS voltage applied to the coil set. Again we turn to the soft switching figure of merit, as shown in Figure 12, for a comparison between an EPC2007 [15] eGaN FET and the FDMC8622 [16] MOSFET. The comparison is made for two MOSFET gate voltages; 6 V and 10 V. This allows a comparison in performance for a circuit that uses the same gate driver for both the eGaN FET and MOSFET. From figure 12 is can be seen that the gate charge is again significantly lower for the eGaN FET than it is for the MOSFET.

Comparing the output charge, the difference is smaller. Operating the MOSFET based amplifier with a gate voltage of 6 V yields lower performance than at 10 volts on the gate despite nearly halving of the

gate charge on-resistance product. Figure 10 shows the performance of the MOSFET based ZVS class-D amplifier operating with a 5 V gate. The experimental setup was unable to exceed 6.4 W output power as the gate driver had exceeded the thermal limit of 85°C despite force air cooling. The measured gate power for the eGaN FET amplifier was 26 mW, versus 232 mW for the MOSFET, an almost 10 times difference. Using a gate driver with higher power capability will no doubt enable the MOSFET based amplifier to increase its power output, but it will be unable to improve the total system efficiency. Furthermore, operation at 13.56 MHz for a MOSFET based converter may not even be possible due to the more than doubling in gate driver losses, rendering the system efficiency to drop well below 50%.

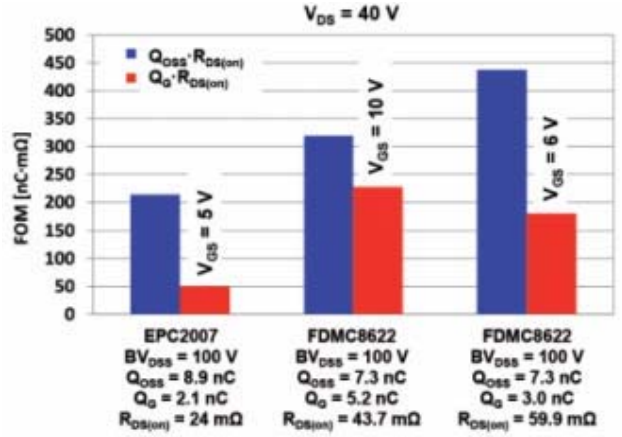

Figure 12: Soft Switching Figure of Merit comparison for the ZVS class-D amplifier

ZVS Class-D sensitivity to load variation

As for the class-E topology we again look at the sensitivity of load variation on the performance of the ZVS class-D amplifier. The full power circuit of ZVS class-D system was simulated in LTspice and the DC load resistance (R_{DCload}) was varied while maintaining a fixed supply voltage to the amplifier. The simulation results were first compared with the experimental results and found to correlate well. Figure 13 shows the simulation results for the losses in the eGaN FET as function of the DC load resistance using the same scale as in figure 7. In this case it can be seen that output power is a strong function of DC load resistance and output power increases as DC load resistance increases, also shown in figure 13. This is due to the increase in the Q-factor of the coil set with increase load resistance.

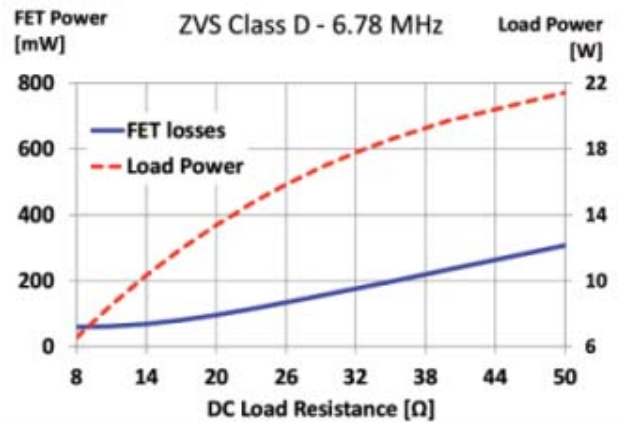

Figure 13: Simulated FET power losses and load power as function of DC load resistance.

Conclusions

The class-E topology has shown promise as a simple and efficient wireless energy transfer converter that is further enhanced when using eGaN FETs. This is despite the inclusion of C_{OSS} into the matching network, and is primarily due to two factors; the significantly lower gate charge of the eGaN FET and the lower $R_{DS(on)}$ for equivalent Q_{OSS}. In the example presented the voltage rating of the eGaN FET was also 33% higher than the MOSFET, further extending the available output power range.

The ZVS class-D showed higher system efficiency than the class-E when operated under the same load conditions. This is mainly due to ZVS switching and the elimination of matching inductors in the main current path. The use of eGaN FETs further enables this topology due to the low gate charge requirement, and the difficulty of driving the upper device using a simple bootstrap supply when using MOSFETs. At 13.56 MHz it may not be possible to drive the upper device without the use of an expensive fully-isolated power supply. The ZVS class-D topology has further been demonstrated to be less sensitive to load variations that causes the coil set impedance to shift, and can even tolerate a small amount of capacitive loading given sufficient current is established in the ZVS tank circuit.

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