# Comparison of Silicon Versus Gallium Nitride FETs for the Use in Power Inverters for Brushless DC Servo Motors

*The Institute of Robotics and Mechatronics of the German Aerospace Centre (DLR) is actually developing a new lightweight robot named SARA, what stands for Safe Robot Assistant. As successor of the LBR III it is the 4th generation of lightweight robots made at the institute. It will feature safe sensor signal supervision to guarantee signal integrity and safe motor and brake control systems to allow secure man machine interaction even with the significant higher dynamics of the new system.*

*By Robin Gruber, German Aerospace Center (DLR)*

SARA consists of seven joints and a flexible gripper, each driven by a brushless DC servo motor from a series of motors, which have also been developed at the institute to get an optimized drive regarding efficiency, space and weight.

*Figure 1: SARA Robot*

To drive these motors low voltage motor power pulse inverters are being developed to fulfill the constraints regarding output power, control of an electromagnetic brake, efficiency and digital interface.

In the final design the inverters are equipped with an FPGA or DSP riser board that will process the 3-phase current controller that is required for a smooth motor control. Four of these inverters will be placed in a heat spreader plate and connected to a common power supply that also carries the bulk DC-link capacitance and a control board that will read in and preprocess the commutation, joint position, force and torque sensors as well as optional additional sensors resulting in a very compact Drive Control Unit. Each unit supplies and evaluates up to 16 sensors and controls four motors so that two Drive Control Units are sufficient to operate the complete arm.

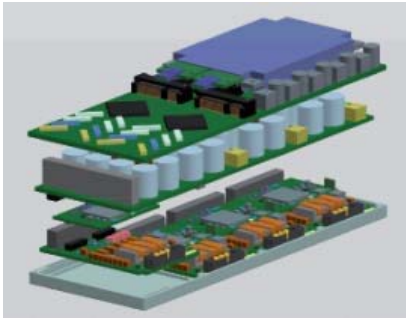

*Figure 2: SARA Drive Control unit for 16 Sensors and 4 Motors*

This different approach compared to the LBR III where each joint had a dedicated inverter and control board directly attached to the motor, improves the modularity and the thermal design - the heat sources like motor and inverter are distributed over the arm and not concentrated at the joints - as well as the serviceability and allows for a more compact joint design.

Since the Robotics and Mechatronics Institute is highly interested in the improvement of sensor and power electronics we used the opportunity of this new robot development to evaluate the new enhancement mode Gallium Nitride FET technology from EPC and compare it with our up to this time best inverter design. Therefore we designed two inverters with the same form factor and electrical interface as well as similar parameters, one Silicon based and one Gallium Nitride based FETs for the 3-phase bridge.
Both inverters are able to deliver at least 25A continuous (35A peak) at a nominal voltage of 48 to 60V (75V peak) (safety extra low voltage) into a motor with an inductance of as low as 100µH requiring at least 40kHz PWM frequency and a current control loop of the same speed. Additionally both inverters provide a digitally controllable output voltage of up to 12V/2A to actuate an electromagnetic brake with current measurement to implement brake inductance measurement for an open / close detection. Overcurrent protection and some housekeeping measurements like motor and inverter temperature and the surveillance of several voltages are implemented as well. Figure 3 shows the two inverters from the bottom side. The tiny blue parts are the GaN-Power-FETs.

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**Phase Current Measurement**

Our standard approach to phase current measurement is a shunt resistor in the source to ground path of each low side transistor for each of the tree half bridges. The shunt signal is then EMI-filtered (to avoid EMI induced offset effects of the amplifier, also known as EMI rejection ratio), amplified and fed into a 12 bit AD converter (see Figure 5). During the operation of the inverter with a symmetric PWM pattern (that originates from the space vector modulation that we usually implement), there is an instant when all low side transistors are conducting and all three phase currents are fed through the shunt resistors so that they can be measured. Timing is essential here, because the measured decaying current equals the average motor phase current only when the sampling point is exactly in the center of the PWM period.

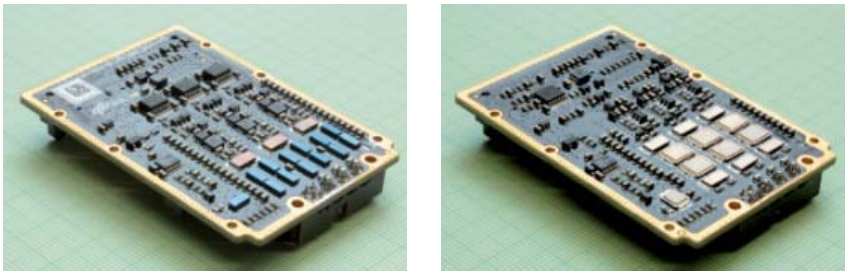

*Figure 3: GaN-FET inverter (left) and Si-MOSFET inverter (right)*

*Figure 4: Topside of the Si-Inverter*

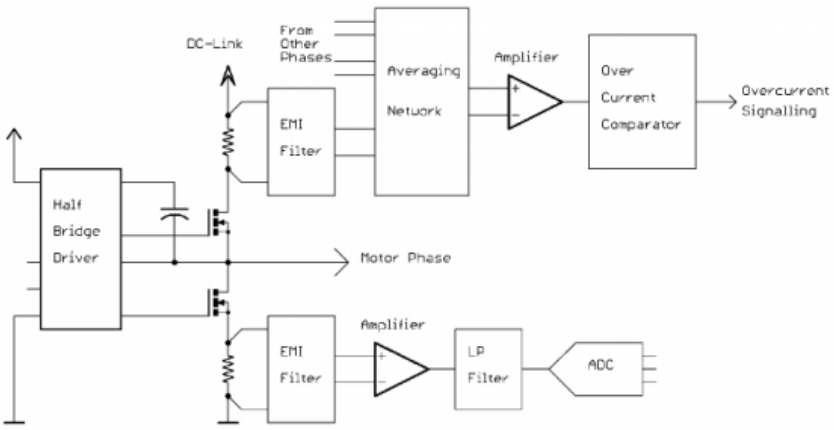


*Figure 5: Low Side Source Shunt Current Measurement*

The advantages of this technique are its simplicity, the (theoretically) small size of the solution and the possibility to implement an automatic offset and 1/f-noise compensation when two measurements per PWM period are performed and subtracted, one when all low side FETs are conducting and one when all high side FETs are on, resulting in no current flow through the low side shunts.

The drawbacks result from the location of the shunt in a fast switched current path. Even when resistors with a very low inductance are being used, the changing current due to the switching of the half bridge, and even worse, the current change of the low side body diode recovering can result in more than 8A/ns, which then will result in a few volts of voltage drop over the resistor followed by excessive ringing compared to a few millivolts of current sensing. The voltage peak and the ringing have to be filtered out, limiting the corner frequency of the amplifier's bandwidth resulting in more time for the amplifier to settle. This settling time limits the minimum pulse width and thus the length of the resulting voltage vector. Figure 6 shows the raw value of the DC current of all three phases as measured by the ADC with current flowing through one phase (only possible on a test setup). For this test the inverter is operated at 50% pulse width for all phases, so current flows for half of the time through the shunt only. The spike on the left originates from the filter's response to the removal of the low side MOSFET's reverse recovery, and the smaller one on the right from discharging the MOSFET's output charge. The decay of the signal near the center is generated by driving an inductive load.

This effect can be reduced by dynamically taking the measurements from the two half bridges that commutate the widest pulse width only and calculate the third phase current. But the ringing of one half bridge induces noise into the DC-link supply which cannot be built infinitely "stiff" and thus is exciting the other half bridges resonant tank resulting in a crosstalk error between the half bridges. To keep this effect as low as possible, we managed to shift the resonant frequency above 200MHz so it can be separated from the measurement signal more easily, provide a very low inductance DC-link voltage and use low inductance resistors which also reduce the chance of self-conducting of the low side FETs when the ringing pulls the source potential below the gate potential.

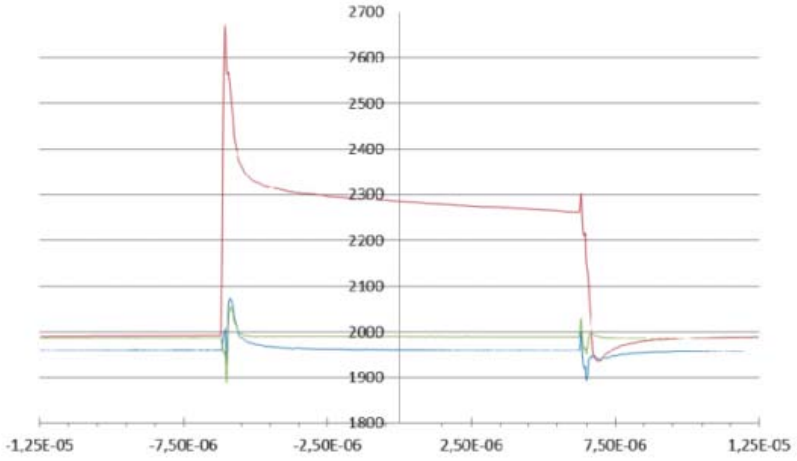


*Figure 6: Signal at the ADC of the low side source shunt current measurement*

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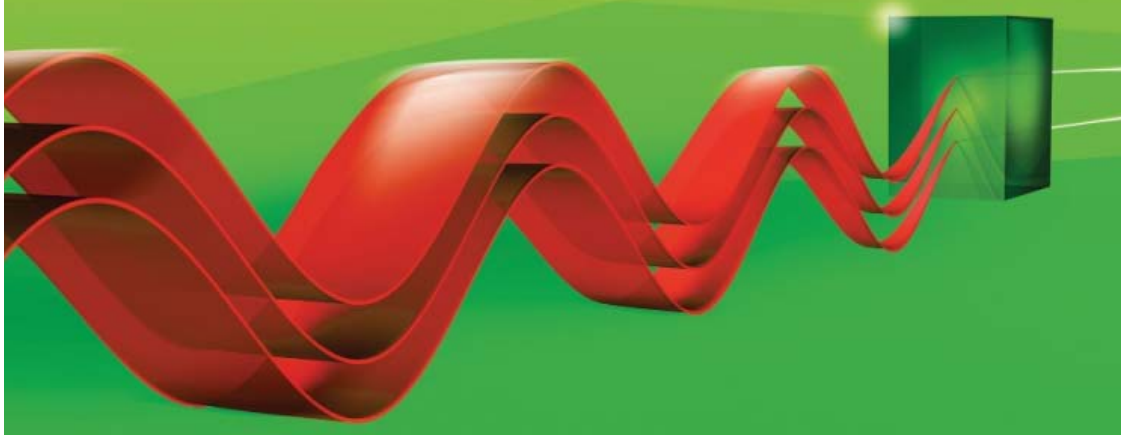

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Another disadvantage of the low side source shunt is the limited ability of an overcurrent protection that can detect a short between two phases only. To extend the protection capabilities to include the detection of a short of a phase to ground, additional high side MOSFET drain shunts have been added together with a summing amplifier and comparators to detect the overcurrent thresholds. Current sensing and overcurrent protection for three phases also need an overall board space of approx. 675mm² (1.04inch²) implemented for the inverter with the silicon MOSFETs.

Figure 7 shows a plot of the deviation of the current measurement of each of the three phases (red, green, blue) of one inverter dependent on the measured current and the pulse width that has been set. The dotted lines show the very wide or very small pulse widths, where the filter either after measuring with all high side or all low side FETs conducting, has not enough time to settle after the current change of the switching and reverse recovery of the body diode excites the ringing.

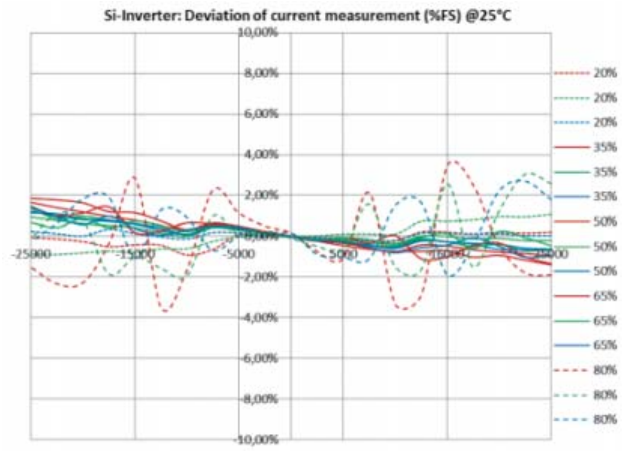


*Figure 7: Accuracy of low side shunt measurement*

Although we managed to keep the DC-link impedance around 10mOhms up to a frequency of 20MHz, below 100mOhms up to 100MHz and below 1Ohm up to 1GHz (measured, not simulated), the ringing of the half bridge can still be found in the DC-link voltage (see Figure 8), but with moderate amplitude. The resulting crosstalk is up to 2.2% of the current of the adjacent phase.

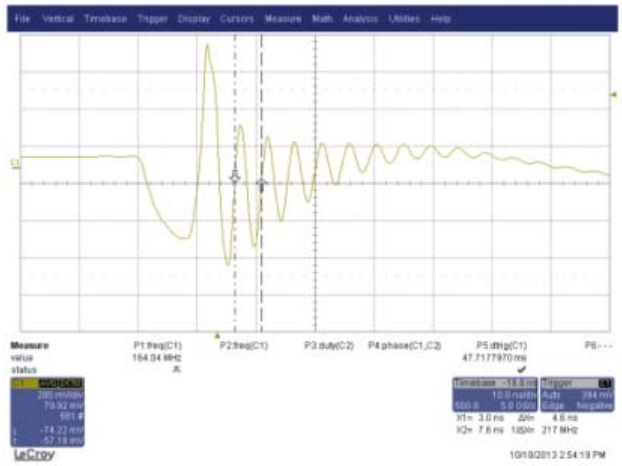

*Figure 8: Ringing in the DC-link supply*

Because our project's senior electronic engineer cowardly refused to build a low side shunt current sensing for the GaN-inverter where transistors were expected to switch faster and the threshold voltages are half that much so that the same common source inductance is in the range of two times as evil, we used the opportunity to make him try a different current measurement approach for the first time at the institute (see Figure 9).

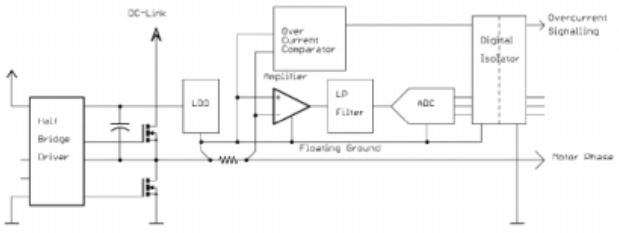


*Figure 9: Current measurement with phase shunt*

Here we use a shunt resistor in the output path of each half bridge. The shunt voltage is monitored by two comparators for overcurrent sensing in both directions and a chopper amplifier with low pass filter followed by a 12 bit AD converter with a 4-channel bidirectional magnetic signal isolator to level shift the AD converter's SPI and the overcurrent signal down to the inverter's ground reference. The shunt evaluation circuit of each half bridge is supplied by its own low noise voltage regulator which is fed from the bootstrap capacitor of the half bridge driver. It was routed using only one single layer and partial vias on the bottom side of the board with a close local ground area underneath directly connected to one side of the shunt. The required board space for this current measurement is approx. 880mm² (1.4inch²).

Although this circuit is hopping from 0 to 60V within about 8ns (which is not too far from the limit of the digital isolator) 40.000 times a second the measurement results are much better (see Figure 10). In addition the measurement crosstalk between two phases could be reduced to 0.1%.

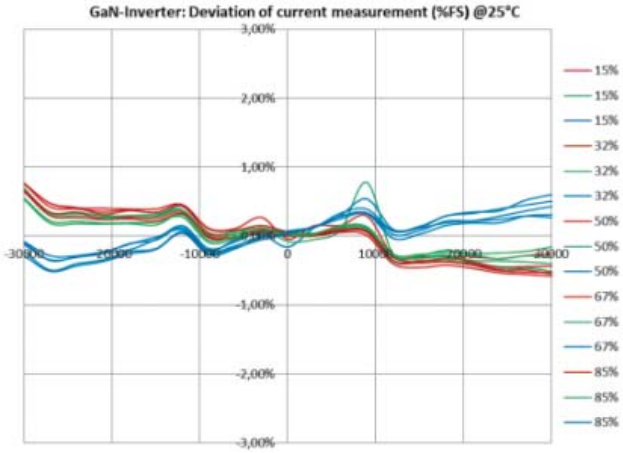


*Figure 10: Accuracy of the phase shunt measurement*

The corner frequency of the low pass filter could be chosen to be 20kHz in contrast to the 3.5MHz bandwidth of the low side shunt bandwidth. Also in this variant two measurements per PWM period are sampled, but now averaged to get a higher resolution and to eliminate a group delay dependent offset that would otherwise occur when undersampling a DC signal with sinusoidal offset only once per period.

The measurement noise vanishes in both variants behind the last bit, because very low noise amplifiers and resistive networks that equal the noise performance of the amplifiers have been used. This is essential because a noise in the current measurement of a robotic arm produces audible noise from the joints.
In addition it has to be noted, that the output voltage from this type of inverter can be higher because here the pulse width range that still allows the current measurement to operate is from 0 to 95%. The upper limit comes from the topology that the bootstrap capacitor also has to supply both the high side MOSFET driver and the current measurement with the bootstrap diode of the bridge driver being too small to supply this higher amount of current when the charging time becomes too small. This will be optimized in further versions.

**Efficiency**
First of all it must be emphasized that the efficiency comparison is not absolutely fair because we compare an 80V inverter with a 100V inverter both operated at 75V for the measurement, but we had no choice - there hasn't been such a thing as an 80V GaN-FET.
The inverter was designed to have its maximum efficiency around the typical robot joint operation point of 4 to 8A that is required for static torque control or slow movement of the system. This ensures low power losses when cooling is critical. As soon as the robot starts moving, higher ammounts of heat can be dissipated due to the better cooling of the arm moving through air.

For the silicon inverter we chose an IRF6646 and for the GaN inverter our loss estimation calculation offered two EPC2001 in parallel. The loss calculation was done for an input voltage of 75V, a voltage vector length of 60V, an output current of 6A, and a gate current of 3A for the silicon and 1.6A for the GaN inverter delivering an estimated efficiency for the power stage alone of 99.58% for Si and 99.67% for GaN, so we assume not to be too far from the optimal transistor choice.

Of course the measurement results differ from these theoretical results, because it's not only the losses in the power stage, but also shunt resistance, connector resistances, ESR of DC-link capacitors, copper losses of PCB traces and output filter losses that occur additionally, and that appeared to be the main loss source.
The peak efficiency of the inverters was measured to 97.7% @ 5A for the silicon type and 98.0% @ 6A for the gallium nitride version. That sounds little but is still a reduction of the losses of 13%.

A small drawback is the switching losses without load, where the GaN FETs cannot play out their advantage of having no reverse recovery losses and lower RDSon. Since we paralleled two transistors for better efficiency at higher currents and have an additional charge at the output of the half bridge generated by the floating ground of the current measurement against DC-link ground, the no load losses are slightly higher than the silicon inverter.

We chose 40kHz switching frequency as a good tradeoff between the switching losses within the inverter and the magnetizing losses within the motor that are mainly generated by eddy currents produced by a changing magnetic field due to the pulsed output voltage that uses the motor winding as storage inductor. For brushless DC motors with less inductance like the ones used for our DLR Hand Arm System higher frequencies of up to 100kHz are used to optimize overall efficiency.



**EMI**

Our project's senior electronic engineer was a little bit worried about the faster switching times of the GaN-FETs in combination with the space (the silicon inverter was first and so the dimensions for the power stage were fixed) and current constrains that didn't allow us to perfectly design as described in the EPC application note for paralleling transistors. Also stealing the restring from poor little vias seemed not to be acceptable for him, so he had to try his own solution.

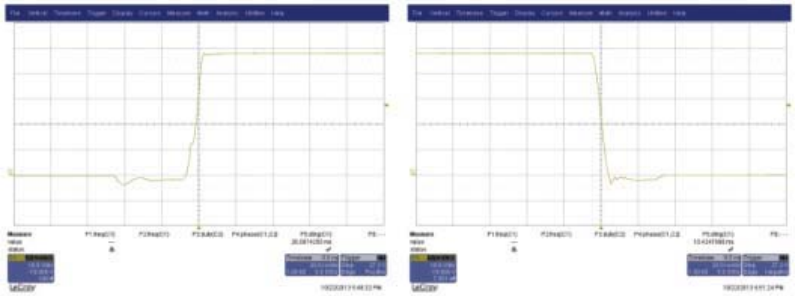

*Figure 11: GaN FET rise and fall times*

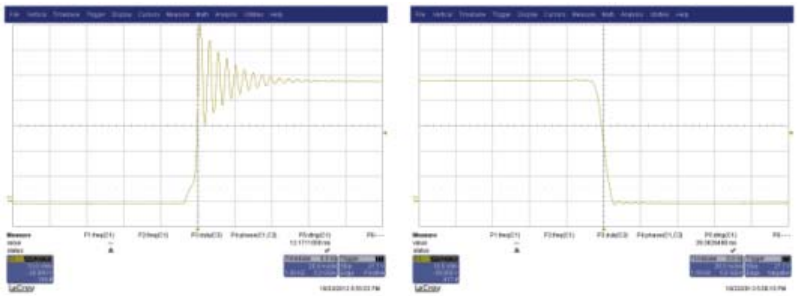

*Figure 12: Silicon MOSFET rise and fall times*

The ringing at the phase output is even lower with the GaN-FETs than with the Si-Transistors, that of course also results from the different current measurement topologies. Figure 11 and Figure 12 show rise and fall times of the inverters. Note that current is flowing out of the phase so the negative voltage over the FETs during the 30ns (the test setup wasn't able to do it any shorter) dead time can be seen.

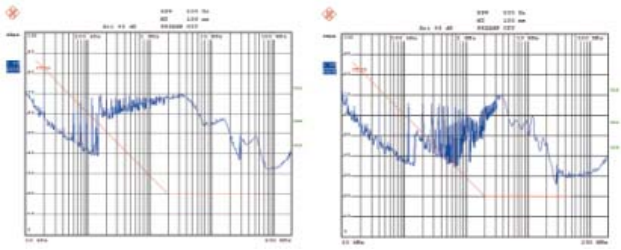

*Figure 13: Common mode noise of industrial inverter (left) and GaN inverter with filter (right)*

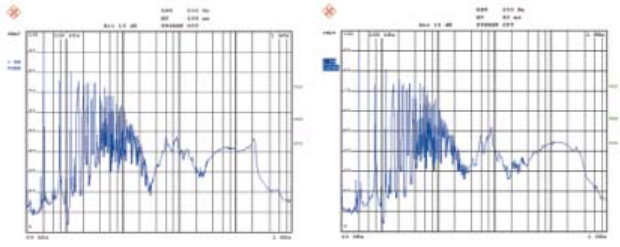

*Figure 14: Interference measured in the DC-link voltage (left: Si, right: GaN)*

With the silicon FETs, the effect is harder to spot in the plot because the beginning and the end of the 200ns dead time lies outside of the measurement window and the body diode forward voltage is lower. Also notice that ringing occurs only during the rising edge. This is when the low side MOSFET is forced to reverse recover its body diode producing a current rise and decay [1] of approx. 15A/ns which is more than the worst case current change caused by switching the load current of approx. 3.5A/ns.

We are planning to use unshielded motor cables since thick cables with shields and small bending radiuses do not match. The estimated rise and fall times of the inverter's half bridges of less than 10ns for both inverter types and the predicted harmonics thereof resulted in a strong urge to implement an output filter, so there is no measurement of the inverters without filter. Instead we compared the GaN-inverter to a compact industrial low voltage inverter (see Figure 13).

To ensure the internal EMC of the complete Joint Control Block we also compared the amounts of noise in the DC-link voltages. Measurements at 10A phase current and 40kHz PWM show no significant difference between the Si and the GaN inverter (see Figure 14).

This was not really unexpected due to the paralleled GaN-FETs, having 16nC total gate charge driven with 1.6A (sourcing) compared to the Si-FETs having 36nC total gate charge driven with 3A, so similar rise and fall times should result.

| | Si | GaN |
|---|---|---|
| Nominal (peak) supply voltage | 20..60V (75V) | 20..80V (95V) |
| Nominal (peak) output current | 25A (35)A | 30A (35A) |
| Nominal output power | 1.5kW | 2.4kW |
| Max. efficiency | 97.7%[1] @ 5A/75V | 98.0%[1] @ 6A/75V |
| PWM frequency | Up to 40kHz | 40 to 100kHz |
| MOSFETs used | IRF6646 | 2xEPC2001 parallel |
| Required board space for power stage (without gate driver) | 242mm² (0.37inch²) | |
| Output for an electromagnetic brake | 12V / 2A | |
| EMI-Filter at Output | included | |
| PCB | 10 layers 70µ (2oz) copper | |
| Size of PCB | 45 x 64mm | |
| Current measurement range | +/-36A | +/- 38A |
| Current measurement topology | Low side source & high side drain shunt | Phase shunt with floating supply and digital isolator |
| Shunt resistance | 2 x 1.5mΩ | 1.5mΩ |
| Current measurement resolution | 12 bit | |
| Current measurement error (25°C) | <5% FS | <0.8% FS |
| Current measurement crosstalk between phases | 2.2% | <0.1% |
| Response time of overcurrent protection | <1µs | <0.5µs |
| Required board space for current measurement | 675mm² (1.04inch²) | 880mm² (1.4inch²). |

1) Including losses of EMI filter, DC-link capacitor ESR, shunts for current measurement, connector resistances and PCB copper losses, without gate driver losses.

*Table 1: Inverter data overview*

**Summary**

The DLR Institute for Robotics and Mechatronics compared silicon with gallium nitride based MOSFET technology for the use in low voltage brushless DC servo motor inverters. It could be demonstrated that it is possible to use GaN-FETs with an increased efficiency and without performance loss regarding output power, EMC and current sensing quality.

**http://dlr.de/rm**

[1] The value has been obtained from a simulation, but measurements on other inverters at the institute show – having 8V drop over the inductance of a bunch of paralleled vias, that were assumed to have 400pH – that this value is not far from reality