**EPC2019 – Enhancement Mode Power Transistor**

\[ V_{DS}, 200 \text{ V} \]
\[ R_{DS(on)} \leq 42 \text{ m\Omega max} \]
\[ I_D, 8.5 \text{ A} \]

Gallium Nitride’s exceptionally high electron mobility and low temperature coefficient allows very low \( R_{DS(on)} \) while its lateral device structure and majority carrier diode provide exceptionally low \( Q_G \) and zero \( Q_{RR} \). The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

**APPLICATION NOTES:**
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source
- Questions: Ask a GaN Expert

<table>
<thead>
<tr>
<th>Maximum Ratings</th>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
<td>Drain-to-Source Voltage (Continuous)</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DS} )</td>
<td>Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)</td>
<td>240</td>
<td></td>
</tr>
<tr>
<td>( I_D )</td>
<td>Continuous ( \left(T_A = 25°C, R_{JA} = 18°C/W\right) )</td>
<td>8.5</td>
<td>A</td>
</tr>
<tr>
<td>( I_D )</td>
<td>Pulsed ( \left(25°C, T_{Pulse} = 300 \mu s\right) )</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-to-Source Voltage</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-to-Source Voltage</td>
<td>-4</td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thermal Characteristics</th>
<th>PARAMETER</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{BJC} )</td>
<td>Thermal Resistance, Junction-to-Case</td>
<td>2.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{BJB} )</td>
<td>Thermal Resistance, Junction-to-Board</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>( R_{BUA} )</td>
<td>Thermal Resistance, Junction-to-Ambient (Note 1)</td>
<td>72</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: \( R_{BUA} \) is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

<table>
<thead>
<tr>
<th>Static Characteristics (( T_J = 25°C ) unless otherwise stated)</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( BVDSS )</td>
<td>Drain-to-Source Voltage</td>
<td>( V_{GS} = 0 \text{ V}, I_D = 125 \mu A )</td>
<td>200</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( IDSS )</td>
<td>Drain-Source Leakage</td>
<td>( V_{GS} = 0 \text{ V}, V_{DS} = 160 \text{ V} )</td>
<td>1</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( IGSS )</td>
<td>Gate-to-Source Forward Leakage</td>
<td>( V_{GS} = 5 \text{ V} )</td>
<td>0.001</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Gate-to-Source Reverse Leakage</td>
<td>( V_{GS} = -4 \text{ V} )</td>
<td>1</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>( V_{GSS(TH)} )</td>
<td>Gate Threshold Voltage</td>
<td>( V_{DS} = V_{GS}, I_D = 1.5 \text{ mA} )</td>
<td>0.8</td>
<td>1.4</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>( R_{DSS(on)} )</td>
<td>Drain-Source On Resistance</td>
<td>( V_{GS} = 5 \text{ V}, I_D = 7 \text{ A} )</td>
<td>22</td>
<td>42</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>( V_{SD} )</td>
<td>Source-Drain Forward Voltage*</td>
<td>( I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V} )</td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Defined by design. Not subject to production test.
### Dynamic Characteristics\(^\#\) (\(T_J = 25^\circ C\) unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{ISS}) Input Capacitance</td>
<td>(V_{GS} = 0\ V, V_{DS} = 100\ V)</td>
<td>254</td>
<td>288</td>
<td></td>
<td>(\text{pF})</td>
</tr>
<tr>
<td>(C_{OSS}) Output Capacitance</td>
<td></td>
<td>1.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{RSS}) Reverse Transfer Capacitance</td>
<td></td>
<td>135</td>
<td>163</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{OSSER}) Effective Output Capacitance, Energy Related (Note 1)</td>
<td>(V_{GS} = 0\ V, V_{DS} = 0\ to 100\ V)</td>
<td>156</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{OSS(TR)}) Effective Output Capacitance, Time Related (Note 2)</td>
<td>(V_{GS} = 0\ V, V_{DS} = 100\ V)</td>
<td>201</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_G) Gate Resistance</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(Q_G) Total Gate Charge</td>
<td>(V_{GS} = 5\ V, V_{DS} = 100\ V, I_D = 7\ A)</td>
<td>2.4</td>
<td>2.9</td>
<td></td>
<td>(\text{nC})</td>
</tr>
<tr>
<td>(Q_{GS}) Gate-to-Source Charge</td>
<td>(V_{DS} = 100\ V, I_D = 7\ A)</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{GD}) Gate-to-Drain Charge</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{GTH}) Gate Charge at Threshold</td>
<td>(V_{GS} = 0\ V, V_{DS} = 100\ V)</td>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{OSS}) Output Charge</td>
<td></td>
<td>20</td>
<td>24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{IRR}) Source-Drain Recovery Charge</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\# Defined by design. Not subject to production test.

---

#### Figure 1: Typical Output Characteristics at 25°C

- \(V_G = 5\ V\)
- \(V_G = 4\ V\)
- \(V_G = 3\ V\)
- \(V_G = 2\ V\)

#### Figure 2: Transfer Characteristics

- \(25^\circ C\)
- \(125^\circ C\)
- \(V_{DS} = 6\ V\)

#### Figure 3: \(R_{DS(on)}\) vs. \(V_G\) for Various Drain Currents

- \(I_D = 3.5\ A\)
- \(I_D = 7.0\ A\)
- \(I_D = 10.5\ A\)
- \(I_D = 14.0\ A\)

#### Figure 4: \(R_{DS(on)}\) vs. \(V_G\) for Various Temperatures

- \(25^\circ C\)
- \(125^\circ C\)
- \(I_D = 7\ A\)
All measurements were done with substrate shortened to source.
Figure 10: Normalized Threshold Voltage vs. Temperature

Normalized Threshold Voltage (V)

T_j – Junction Temperature (°C)

0 25 50 75 100 125 150

Normalized Threshold Voltage

V_{DS} – Drain-Source Voltage (V)

T_j = Max Rated, T_c = +25°C, Single Pulse

Figure 11: Safe Operating Area

Limited by \( I_{D} \)

Pulse Width

100 ms

100 µs

10 µs

Limited by \( R_{DS(on)} \)

Figure 12: Transient Thermal Response Curves

Junction-to-Board

Z_{θJB}, Normalized Thermal Impedance

10^{-4} 10^{-5} 10^{-3} 10^{-2} 10^{-1} 1

1

0.1

0.01

0.001

0.0001

Single Pulse

Duty Cycle:

0.5

0.1

0.05

0.02

0.01

\( P_{DM} \)

\( t_1 \)

\( t_2 \)

Notes:

Duty Factor: \( D = \frac{t_1}{t_2} \)

Peak \( T_j = P_{DM} x Z_{θJB} x R_{θJB} + T_B \)

Junction-to-Case

Z_{θJC}, Normalized Thermal Impedance

10^{-5} 10^{-6} 10^{-4} 10^{-3} 10^{-2} 1

1

0.1

0.01

0.001

0.0001

Single Pulse

Duty Cycle:

0.5

0.2

0.1

0.05

0.02

0.01

\( P_{DM} \)

\( t_1 \)

\( t_2 \)

Notes:

Duty Factor: \( D = \frac{t_1}{t_2} \)

Peak \( T_j = P_{DM} x Z_{θJC} x R_{θJC} + T_C \)
### TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7” reel

![Tape and Reel Configuration Diagram]

#### TAPE AND REEL CONFIGURATION

- **Loaded Tape Feed Direction**
- **Die orientation dot**
- **Gate solder bar is under this corner**
- **Die is placed into pocket solder bar side down (face side down)**

#### TAPE AND REEL CONFIGURATION

**Tape and Reel Configuration**

- **4 mm pitch, 8 mm wide tape on 7” reel**

---

### DIE MARKINGS

- **Die orientation dot**
- **Gate Pad bump is under this corner**

#### DIE MARKINGS

- **2019 YYYY ZZZZ**

---

### DIE OUTLINE

#### Solder Bar View

- **Part Number**
- **Laser Markings**

---

### MICROMETERS

#### Dimension (mm)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Target</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>8.00</td>
<td>7.90</td>
<td>8.30</td>
</tr>
<tr>
<td>b</td>
<td>1.75</td>
<td>1.65</td>
<td>1.85</td>
</tr>
<tr>
<td>c (Note 2)</td>
<td>3.50</td>
<td>3.45</td>
<td>3.55</td>
</tr>
<tr>
<td>d</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>e</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>f (Note 2)</td>
<td>2.00</td>
<td>1.95</td>
<td>2.05</td>
</tr>
<tr>
<td>g</td>
<td>1.50</td>
<td>1.40</td>
<td>1.60</td>
</tr>
</tbody>
</table>

#### Part Number
- **EPC2019**
- **2019 YYYY ZZZZ**

---

### Notes:

- **Note 1**: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.
- **Note 2**: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

---

### DIE OUTLINE

- **Solder Bar View**
- **Side View**

---

### MICROMETERS

#### Dimension (mm)

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>Nominal</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2736</td>
<td>2766</td>
<td>2796</td>
</tr>
<tr>
<td>B</td>
<td>920</td>
<td>950</td>
<td>980</td>
</tr>
<tr>
<td>c</td>
<td>697</td>
<td>700</td>
<td>703</td>
</tr>
<tr>
<td>d</td>
<td>247</td>
<td>250</td>
<td>253</td>
</tr>
<tr>
<td>e</td>
<td>168</td>
<td>183</td>
<td>198</td>
</tr>
<tr>
<td>f</td>
<td>245</td>
<td>250</td>
<td>255</td>
</tr>
<tr>
<td>g</td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>h</td>
<td>450</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>i</td>
<td>235</td>
<td>250</td>
<td>265</td>
</tr>
</tbody>
</table>

#### Pad Connections
- **Pad no. 1 is Gate**
- **Pad no. 3, 5 are Drain**
- **Pad no. 2, 4, 6 are Source**
- **Pad no. 7 is Substrate.**

#### Substrate Pin Connection
- **Substrate pin should be connected to Source**
The land pattern is solder mask defined. Copper is larger than the solder mask opening. Solder mask is 10 µm smaller per side than bump.

Pad no. 1 is Gate
Pad no. 3, 5 are Drain
Pad no. 2, 4, 6 are Source
Pad no. 7 is Substrate*

*Substrate pin should be connected to Source

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content

Additional Resources Available
- Assembly resources available at: https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx
- Library of Altium footprints for production FETs and ICs: https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip
  (for preliminary device Altium footprints, contact EPC)

Note: This datasheet is representative of lots with date code of 2131 or later.