EPC2110 – Dual Common-Source Enhancement-Mode GaN Power Transistor

$V_{DS}$, 120 V
$R_{DS(on)}$, 110 mΩ
$I_D$, 3.4 A

Gallium Nitride’s exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings of Q1 & Q2

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$ (Drain-to-Source Voltage (Continuous))</td>
<td>120</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$ (Continuous ($T_A = 25^\circ C, R_{JA} = 52^\circ C/W$))</td>
<td>3.4</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$ (Pulsed ($25^\circ C, T_{PULSE} = 300 \mu s$))</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$V_{GS}$ (Gate-to-Source Voltage)</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>$T_J$ (Operating Temperature)</td>
<td>–40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

EPC2110 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 1.35 mm x 1.35 mm

Applications
- Ultra High Frequency DC-DC Conversion
- Wireless Power Transfer
- Synchronous Rectification

Benefits
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low $Q_G$
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETsandICs/EPC2110.aspx

Thermal Characteristics of Q1 & Q2

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{BIC}$ (Thermal Resistance, Junction-to-Case)</td>
<td>3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{BIB}$ (Thermal Resistance, Junction-to-Board)</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>$R_{JJA}$ (Thermal Resistance, Junction-to-Ambient (Note 1))</td>
<td>81</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: $R_{JJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Termal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics of Q1 & Q2 ($T_J = 25^\circ C$ unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BV_{DSS}$ (Drain-to-Source Voltage)</td>
<td>$V_{GS} = 0 V, I_D = 0.3 mA$</td>
<td>120</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$ (Drain-Source Leakage)</td>
<td>$V_{DS} = 96 V, V_{GS} = 0 V$</td>
<td>0.01</td>
<td>0.25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{GSS}$ (Gate-to-Source Forward Leakage)</td>
<td>$V_{GS} = 5 V$</td>
<td>0.05</td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{GS(TH)}$ (Gate Threshold Voltage)</td>
<td>$V_{DS} = V_{GS}, I_D = 0.7 mA$</td>
<td>0.8</td>
<td>1.4</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (Drain-Source On Resistance)</td>
<td>$V_{GS} = 5 V, I_D = 4 A$</td>
<td>80</td>
<td>110</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>$V_{SD}$ (Source-Drain Forward Voltage)</td>
<td>$I_S = 0.5 A, V_{GS} = 0 V$</td>
<td></td>
<td>1.9</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
Dynamic Characteristics of Q1 & Q2 (TJ = 25°C unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{ISS}</td>
<td>Input Capacitance</td>
<td>85</td>
<td>100</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{RSS}</td>
<td>Reverse Transfer Capacitance</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{OSS}</td>
<td>Output Capacitance</td>
<td>45</td>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{OSS(ER)}</td>
<td>Effective Output Capacitance, Energy Related (Note 2)</td>
<td>54</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{OSS(TR)}</td>
<td>Effective Output Capacitance, Time Related (Note 3)</td>
<td>67</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{G}</td>
<td>Gate Resistance</td>
<td>0.6</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Q_{G}</td>
<td>Total Gate Charge</td>
<td>0.8</td>
<td>1.1</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{GS}</td>
<td>Gate to Source Charge</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q_{GD}</td>
<td>Gate to Drain Charge</td>
<td>0.18</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q_{G(TH)}</td>
<td>Gate Charge at Threshold</td>
<td>0.16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q_{OSS}</td>
<td>Output Charge</td>
<td>4</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q_{RR}</td>
<td>Source-Drain Recovery Charge</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% B_{VDS}.  
Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% B_{VDS}. 

EPC2110 – Detailed Schematic

Note: The EPC2110 can be connected in parallel or used as independent FETs with common source.
Figure 1 (Q1 & Q2): Typical Output Characteristics at 25°C

Figure 2 (Q1 & Q2): Transfer Characteristics

Figure 3 (Q1 & Q2): $R_{\text{DS(\text{on})}}$ vs. $V_{\text{GS}}$ for Various Drain Currents

Figure 4 (Q1 & Q2): $R_{\text{DS(\text{on})}}$ vs. $V_{\text{GS}}$ for Various Temperatures

Figure 5a (Q1 & Q2): Capacitance (Linear Scale)

Figure 5b (Q1 & Q2): Capacitance (Log Scale)
Figure 10 (Q1 & Q2): Normalized Threshold Voltage vs. Temperature

![Normalized Threshold Voltage vs. Temperature](image)

- **Normalized Threshold Voltage vs. Temperature**
- **TJ – Junction Temperature (°C)**
- **Id = 0.7 mA**

Figure 9 (Q1 & Q2): Normalized On-State Resistance vs. Temperature

![Normalized On-State Resistance vs. Temperature](image)

- **Normalized On-State Resistance R_{DS(on)}**
- **TJ – Junction Temperature (°C)**
- **Id = 4 A**
- **VGS = 5 V**
- **VDS = 60 V**

Figure 8: Reverse Drain-Source Characteristics

![Reverse Drain-Source Characteristics](image)

- **ISD – Source-to-Drain Current (A)**
- **VSD – Source-to-Drain Voltage (V)**
- **25˚C**
- **125˚C**
- **VGS = 0 V**
- **VDS = 3 V**
- **Id = 4 A**
- **VDS = 60 V**

Figure 7 (Q1 & Q2): Gate Charge

![Gate Charge](image)

- **QG – Gate Charge (pC)**
- **VGS – Gate-to-Source Voltage (V)**
- **QG = 4 A**
- **VGS = 60 V**

Figure 6 (Q1 & Q2): Output Charge and C_{oss} Stored Energy

![Output Charge and C_{oss} Stored Energy](image)

- **QOSS – Output Charge (nC)**
- **EOSS – C_{oss} Stored Energy (µJ)**
- **VDS – Drain-to-Source Voltage (V)**
- **QOSS = 4 A**
- **VDS = 60 V**

Figure 6a: Output Charge and COSS Stored Energy

![Output Charge and COSS Stored Energy](image)

- **QOSS – Output Charge (nC)**
- **EOSS – COSS Stored Energy (µJ)**
- **VDS – Drain-to-Source Voltage (V)**
- **QOSS = 4 A**
- **VDS = 60 V**

Figure 5: Reverse Drain-Source Characteristics

![Reverse Drain-Source Characteristics](image)

- **ID – Source-to-Drain Current (A)**
- **VSD – Source-to-Drain Voltage (V)**
- **25˚C**
- **125˚C**
- **VGS = 0 V**
- **VSD = 3 V**
- **Id = 4 A**
- **VDS = 60 V**

Figure 4: Gate Charge

![Gate Charge](image)

- **QG – Gate Charge (pC)**
- **VGS – Gate-to-Source Voltage (V)**
- **QG = 4 A**
- **VGS = 60 V**

Figure 3: Normalized Output Charge

![Normalized Output Charge](image)

- **QOSS – Output Charge (nC)**
- **EOSS – COSS Stored Energy (µJ)**
- **VDS – Drain-to-Source Voltage (V)**
- **QOSS = 4 A**
- **VDS = 60 V**

Figure 2: Normalized Gate Charge

![Normalized Gate Charge](image)

- **QG – Gate Charge (pC)**
- **VGS – Gate-to-Source Voltage (V)**
- **QG = 4 A**
- **VGS = 60 V**

Figure 1: Normalized Drain Current vs. Temperature

![Normalized Drain Current vs. Temperature](image)

- **ID – Source-to-Drain Current (A)**
- **VSD – Source-to-Drain Voltage (V)**
- **25˚C**
- **125˚C**
- **VGS = 0 V**
- **VSD = 3 V**
- **Id = 4 A**
- **VDS = 60 V**

Figure 1: Normalized Drain Current vs. Temperature

![Normalized Drain Current vs. Temperature](image)

- **ID – Source-to-Drain Current (A)**
- **VSD – Source-to-Drain Voltage (V)**
- **25˚C**
- **125˚C**
- **VGS = 0 V**
- **VSD = 3 V**
- **Id = 4 A**
- **VDS = 60 V**
Notes:
- Duty Factor: $D = \frac{t_1}{t_2}$
- Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Notes:
- Duty Factor: $D = \frac{t_1}{t_2}$
- Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 11a (Q1 & Q2): Transient Thermal Response Curves (Junction-to-Board)

Figure 11b (Q1 & Q2): Transient Thermal Response Curves (Junction-to-Case)

Figure 12 (Q1 & Q2): Safe Operating Area
**DIE MARKINGS**

Die orientation dot
Pin 1 is under this corner

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Laser Markings</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC2110</td>
<td>2110 YYYY ZZZZ</td>
</tr>
</tbody>
</table>

**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7” reel

<table>
<thead>
<tr>
<th>Dimension (mm)</th>
<th>EPC2110 (note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>8.00  7.90  8.30</td>
</tr>
<tr>
<td>b</td>
<td>1.75  1.65  1.85</td>
</tr>
<tr>
<td>c (see note)</td>
<td>3.50  3.45  3.55</td>
</tr>
<tr>
<td>d</td>
<td>4.00  3.90  4.10</td>
</tr>
<tr>
<td>e</td>
<td>4.00  3.90  4.10</td>
</tr>
<tr>
<td>f (see note)</td>
<td>2.00  1.95  2.05</td>
</tr>
<tr>
<td>g</td>
<td>1.5   1.5   1.6</td>
</tr>
</tbody>
</table>

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.
**DIE OUTLINE**

Solder Bump View

- Pad 1 is Gate 1;
- Pad 7 is Gate 2;
- Pads 2, 3 are Drain 1;
- Pads 8, 9 are Drain 2;
- Pads 4, 6 are Source;
- Pad 5 is Substrate*

*Substrate pin should be connected to Source

**Side View**

Seating Plane

<table>
<thead>
<tr>
<th>DIM</th>
<th>Micrometers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>A</td>
<td>1320</td>
</tr>
<tr>
<td>B</td>
<td>1320</td>
</tr>
<tr>
<td>c</td>
<td>450</td>
</tr>
<tr>
<td>d</td>
<td>210</td>
</tr>
<tr>
<td>e</td>
<td>187</td>
</tr>
</tbody>
</table>

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**RECOMMENDED LAND PATTERN**

(measurements in µm)

- The land pattern is solder mask defined
- Solder mask is 10 µm smaller per side than bump

**RECOMMENDED STENCIL DRAWING**

(measurements in µm)

- Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

- Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.


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EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

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