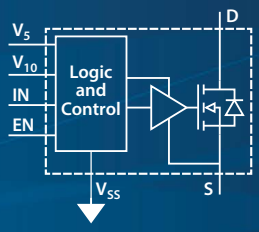
# EPC21702 – eToF™ Laser Driver IC

100 V

30 A Peak

PRELIMINARY




EFFICIENT POWER CONVERSION

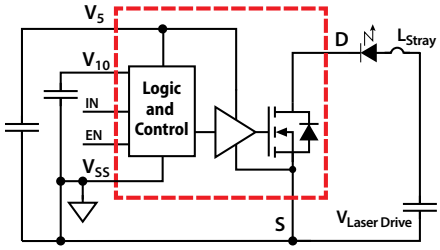
RoHS Halogen-Free

The EPC21702 is a laser driver that is controlled using 3.3 V logic at high frequencies of up to 10 MHz to modulate laser driving currents of up to 30 Amps. Full driver integration is achieved using EPC's proprietary GaN IC technology.

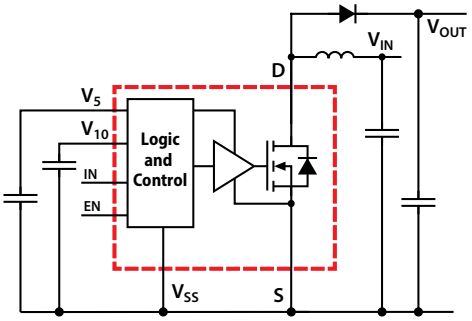
Wafer-level chip-scale packaging is used resulting in a BGA package that measures only 1.66 x 1.46 mm. The BGA package has low inductance and lays out very well with the laser system.

The EPC21702 uses 5 V and 10 V logic supplies and is capable of interfacing to digital controllers.

### Typical Connection Diagram




Laser Driver




Boost Converter

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to $V_{SS}$ = S unless indicated otherwise.

| Symbol | Definition | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_D$ | Drain Voltage (to Source) | | 100 | V |
| $V_5$ | 5 V Supply Voltage | -0.3 | 5.5 | |
| $V_{10}$ | 10 V Supply Voltage | -0.3 | 11 | |
| IN | Logic Input | -0.3 | 5 | |
| $I_D$ | Average Drain Current | | 7.4 | A |
| $T_J$ | Operating Junction Temperature | -40 | 125 | °C |
| $T_{STG}$ | Storage Temperature | -40 | 150 | |

## ESD Ratings

| Symbol | Definition | MIN | UNIT |
|---|---|---|---|
| HBW | Human-body model | +/-250 | V |
| CDM | Charged-device model[6] | N/A | |

## Thermal Characteristics

| Symbol | Definition | MIN | UNIT |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 3.0 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 6.6 | |
| $R_{\theta JA\_JEDEC}$ | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB) | 71 | |
| $R_{\theta JA\_EVB}$ | Thermal Resistance, Junction-to-Ambient (using EPC9185 EVB) | 46 | |

Die size: 1.66 x 1.46 mm

**EPC21702** eToF laser driver ICs are supplied in passivated die form with solder bumps.

### Features

- $V_{Laser}$ operating range up to 80 V
- Low current sleep mode with fast enable
- 30 Amp peak current
- Switching frequency greater than 10 MHz
- Typical voltage switching time 1 ns
- 5 V and 10 V nominal logic power supplies
- 3.3 V logic compatible input control
- 1.5 ns minimum output pulse width
- 3.5 ns delay time from input to output

### Applications

- Time of flight measurement
  - Security systems
  - Driver awareness
  - Robotic vision
  - Industrial safety
  - Automotive parking assistance and collision avoidance
- Power Supply
  - Boost control switch
  - Flyback control switch
  - Forward control switch
- Class-E Amplifier

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC21702

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to $V_{SS}$ = S unless indicated otherwise.

| Symbol | Definition | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{Laser}$ | Laser Driver Voltage (to Source) [5] | 5 | | 80 | V |
| $V_5$ | 5 V Supply Voltage [5] | | 5 | | |
| $V_{10}$ | 10 V Supply Voltage [5] | | 10 | | |

## Truth Table

| IN | EN | Laser |
|---|---|---|
| X | 0 | Laser Driver Sleep |
| 0 | 1 | Off |
| 1 | 1 | On |

## Electrical Characteristics

All ratings at $T_J$ = 25°C. $V_{Laser}$ = 50 V, $R_{Load}$ = 2.3 Ω, $V_{IL}$ = 0 V, $V_{IH}$ = 3.3 V, $V_5$ = 5 V, $V_{10}$ = 10 V, enable active unless indicated otherwise.

| Symbol | Definition | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Operating Power Supply, $V_{DD}$** | | | | | |
| $I_{5\ (Off)}$ | $V_5$ Quiescent current with laser driver off | | 35 | 60 | mA |
| $I_{5\ (1\ MHz)}$ | Operating current off $V_5$ | | 39 | | |
| $I_{5(Sleep)}$ | Sleep mode current from $V_5$ (EN = Low) | | | 1 | |
| $I_{10}$ | Operating current from $V_{10}$ | | | 1.5 | |
| **Input Pins** | | | | | |
| $V_{IH}$ | High-level input voltage threshold | 1.9 | | | V |
| $V_{IL}$ | Low-level input voltage threshold | | | 0.5 | |
| $V_{IHyst}$ | Hysteresis between rising and falling threshold | 35 | | | mV |
| $R_{IN}$ | Input pulldown resistance | | 1.25 | | kΩ |
| $R_{EN}$ | Enable pulldown resistance | | 50 | | Ω |
| **Power Stage** | | | | | |
| $R_{DS(on)}$ [1] | Drain to Source Resistance | | 23 | | mΩ |
| $I_{D(peak)}$ [1] | Peak Laser Drive Current Capability | 30 | | | A |
| $C_{OSS}$ [1] | $V_{DS}$ = 50 V, $V_{IN}$ = 0 V | | 107 | | pF |
| $Q_{OSS}$ [1] | $V_{DS}$ = 50 V, $V_{IN}$ = 0 V | | 8.0 | | nC |
| $E_{OSS}$ [1] | $V_{DS}$ = 50 V, $V_{IN}$ = 0 V | | 162 | | nJ |
| $C_{OSS(ER)}$ [1,2] | $V_{DS}$ = 0 to 50 V, $V_{IN}$ = 0 V | | 129 | | pF |
| $C_{OSS(TR)}$ [1,3] | $V_{DS}$ = 0 to 50 V, $V_{IN}$ = 0 V | | 159 | | |
| **Dynamic Characteristics** | | | | | |
| $t_{EN}$ | Time to Enable | | 45 | 100 | ns |
| $t_{D(on)}$ [1] | Turn on delay time | | 3.5 | 6.75 | |
| $t_F$ [1] | Drain fall time | | 0.75 | 1.5 | |
| $t_{D(off)}$ [1] | Turn off delay time | | 5.2 | 7.3 | |
| $t_R$ [1,4] | Drain rise time (refer to figure 9) | | 0.4 | | |
| $t_{dPW}$ [1] | Pulse width distortion | - 2 | -0.24 | 1.6 | |
| $t_{in(min(on))}$ [1] | Minimum input pulse width | | 2.5 | | |
| $t_{D(min(on))}$ [1] | Minimum drain pulse width | | 1.5 | | |
| $t_{On(Max)}$ [1] | Maximum on time | | 500 | | µs |
| PRF [1] | Maximum pulse repetition frequency, 0 °C to 100 °C | | 10 | | MHz |

**Notes:**

1 Guaranteed by design, but not tested

2 $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% max ($V_D$)

3 $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% max ($V_D$)

4 Drain rise time is determined by ZVS charging of the output capacitance

5 See Power Sequencing section in Applications Information for considerations on laser drive voltage

6 Paragraph 2.7 of AEC Q100-011 Rev. D, Jan. 29, 2019 states that CDM specification is not necessary on such a small device

## Pinout Description

| Pin | Description |
|---|---|
| $V_5$ | 5 V Voltage Supply (Decouple to GND with small, low inductance capacitor) |
| $V_{10}$ | 10 V Voltage Supply (Decouple to GND with small, low inductance capacitor) |
| EN | Enable |
| IN | Logic input |
| D | Power Drain |
| S | Power Source |
| $V_{SS}$ | Signal Ground |

## Performance Curves

**Figure 1: Typical Quiescent Current vs. Temperature**

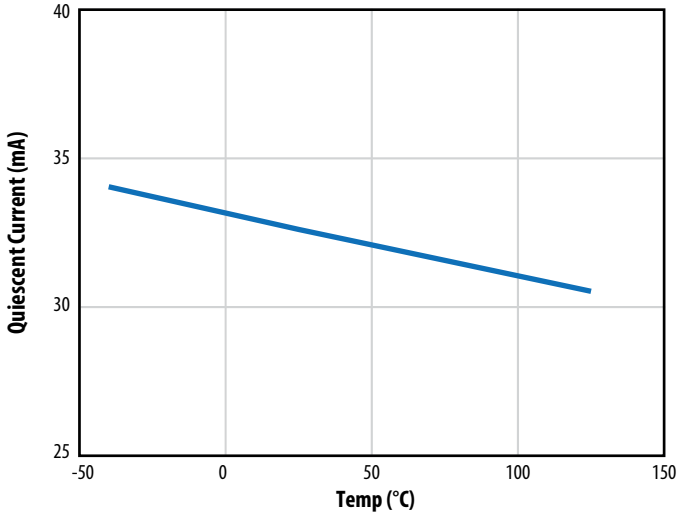



**Figure 2: Typical Turn On Propagation Delay vs. Temperature**

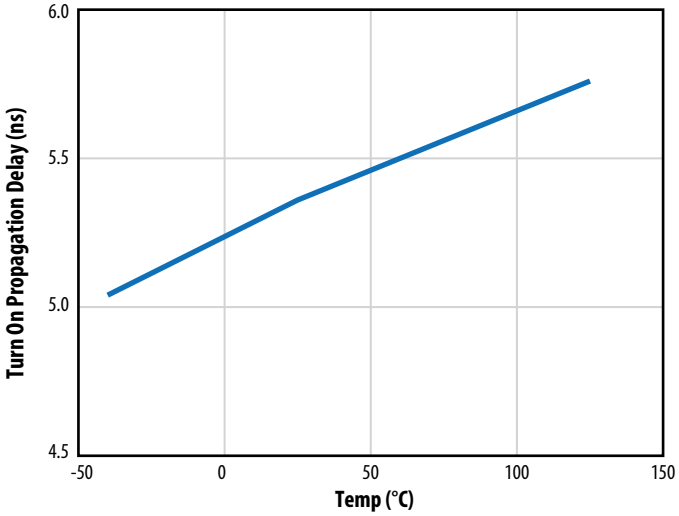



**Figure 3: Typical Turn Off Propagation Delay vs. Temperature**

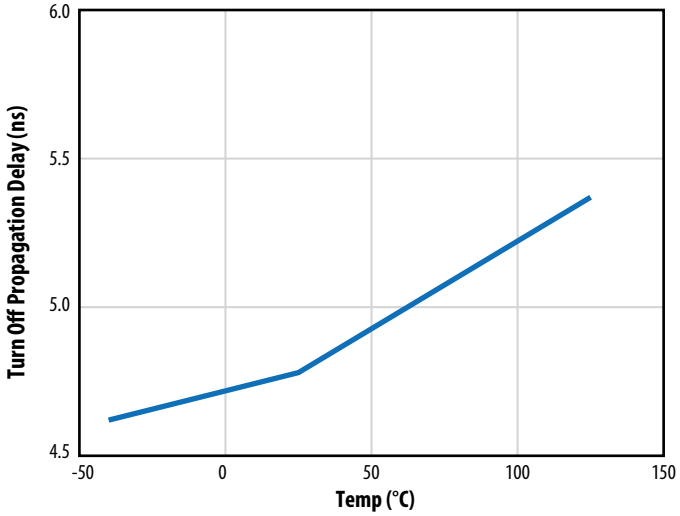



**Figure 4: Typical $C_{OSS}$**

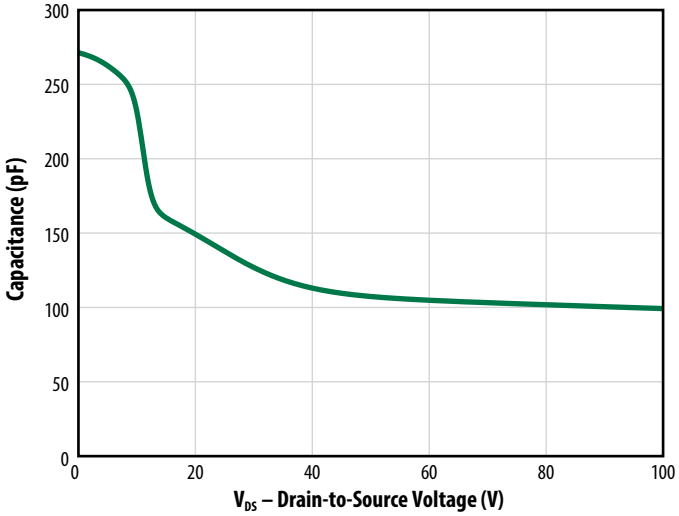



**Figure 5: Typical Output Charge and $C_{OSS}$ Stored Energy**

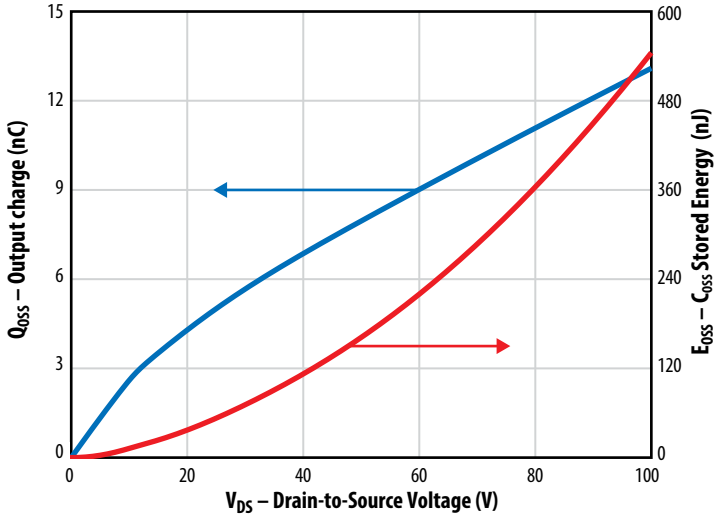
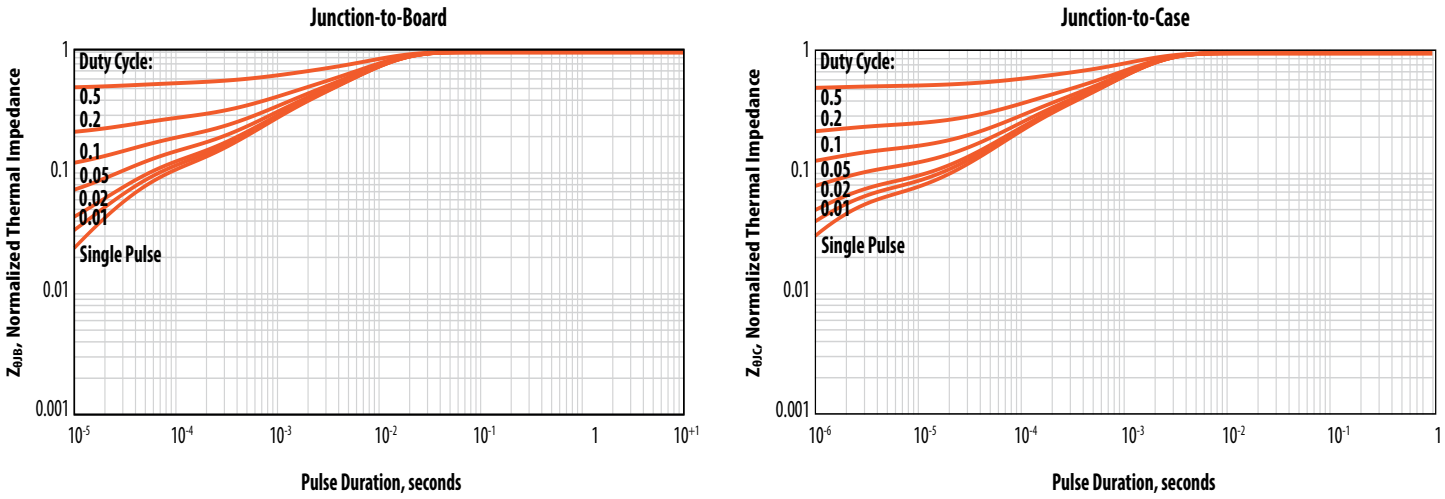


**Figure 6: Transient Thermal Impedance**




## Application Information

### Safety Warning

This device is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

### Power Sequencing

IN must be held low during power up sequence. For power up, $V_5$ and $V_{10}$ must be applied before applying voltage to the drain to prevent possible unwanted turn on of the output. For power down, the order must be reversed.

| Power Up | EN | IN | $V_{10}$ | $V_5$ | Drain |
|---|---|---|---|---|---|
| 1 | Low | Low | 0 V | 0 V | 0 V |
| 2 | Low | Low | 0 V | 5 V | 0 V |
| 3 | Low | Low | 10 V | 5 V | 0 V |
| 4 | Low | Low | 10 V | 5 V | $V_{Laser\ Drive}$ |
| 5 | Active | Low | 10 V | 5 V | $V_{Laser\ Drive}$ |
| 6 | Active | Active | 10 V | 5 V | $V_{Laser\ Drive}$ |
| **Power Down** | **IN** | **IN** | **$V_{DD}$** | **$V_{DD}$** | **Drain** |
| 1 | Low | Low | 10 V | 5 V | $V_{Laser\ Drive}$ |
| 2 | Low | Low | 10 V | 5 V | 0 V |
| 1 | Low | Low | 0 V | 5 V | 0 V |
| 2 | Low | Low | 0 V | 0 V | 0 V |

## Application Information

### Layout and decoupling

Minimizing inductance in both power and gate drive loops is critical. The power loop is primary, and gate drive loop secondary. Short, wide traces are required, and returning in the second layer, using a thin dielectric will cancel much of the inductance. Using multiple ceramic capacitors in parallel will reduce stray inductance and impedance in the power loop. Use high quality NPO or COG capacitors for both power and gate drive. This will increase effective capacitance as capacitors with lower quality materials will lose much more capacitance with voltage. Recommended layout is shown below. Component recommendations for power and gate drive decoupling capacitors are shown in the demonstration board quick start guide.

Turn off current is limited by the energy of the power loop stray inductance transferring to the $C_{OSS}$ of the power FET of the laser driver. $E_{OSS}$ vs. $V_{DS}$ curve is in the datasheet (Figure 5).

### Start up

$V_{DD}$ should be applied before the laser voltage. For applications where the laser voltage is below 10 V and at elevated temperatures, it may take a few pulses before the pulse width stabilizes.

### Output Capacitance

Output capacitance ($C_{OSS}$) is the capacitance between D and $V_{SS}$. Output charge ($Q_{OSS}$) is the integral of output capacitance over voltage. Just like discrete power FETs, output capacitance is charged and discharged with each cycle. This takes time and dissipates power. Please refer to FET application notes to determine impact.

**Figure 7: Power and Gate Drive Turn On Loops**

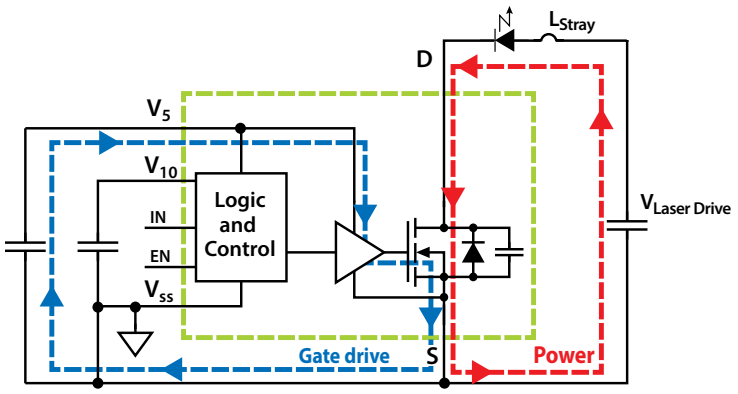
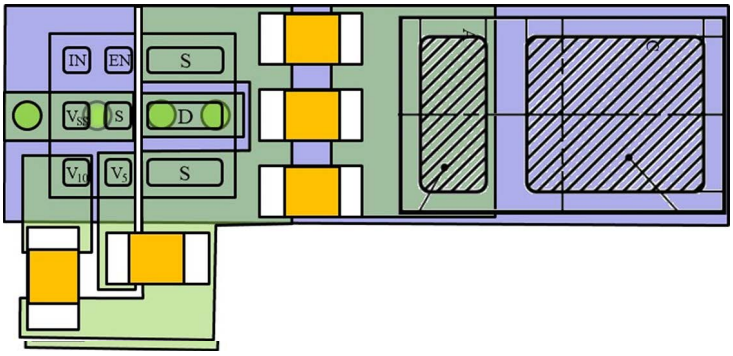



**Figure 8: Recommended Layout**




Cathode to drain connection on second conductor layer

**Figure 9: Parameter Measurement Test Circuits**

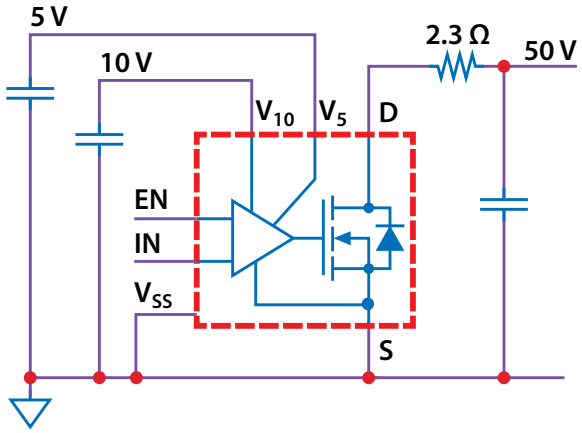
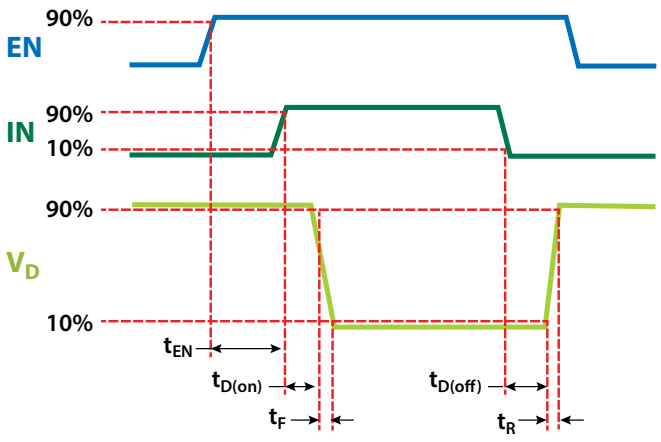
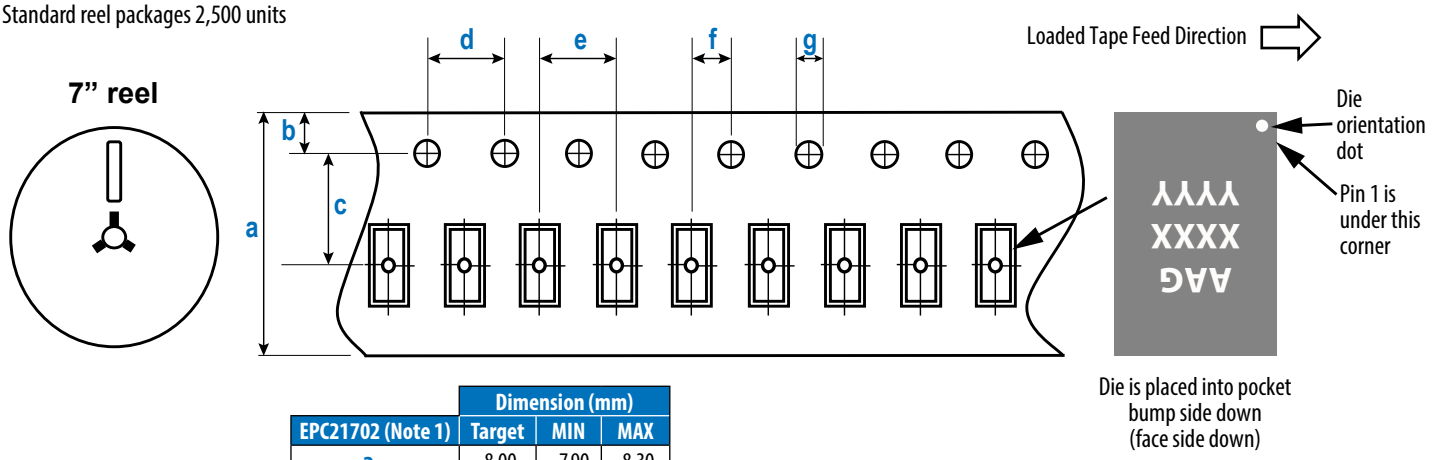



**Figure 10: Parameter Measurement Definitions**



## TAPE AND REEL CONFIGURATION

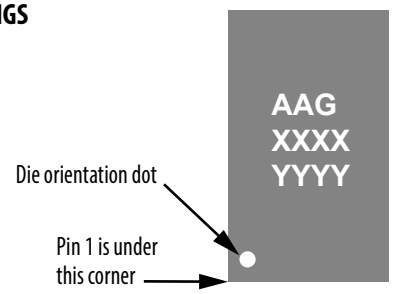
4 mm pitch, 8 mm wide tape on 7" reel
Standard reel packages 2,500 units




| EPC21702 (Note 1) | Dimension (mm) Target | MIN | MAX |
|---|---|---|---|
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

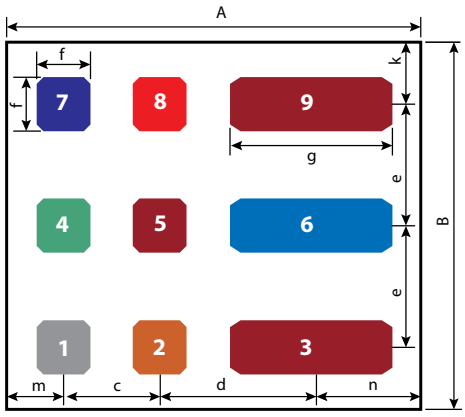
## DIE MARKINGS



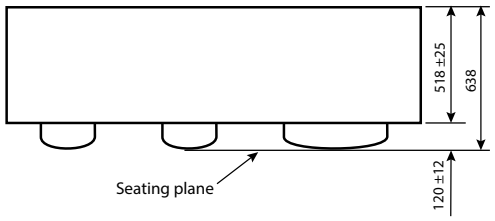

| Part Number | Laser Markings | | |
|---|---|---|---|
| | Part Number Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC21702 | AAG | XXXX | YYYY |

## DIE OUTLINE

Solder Bump View




Side View

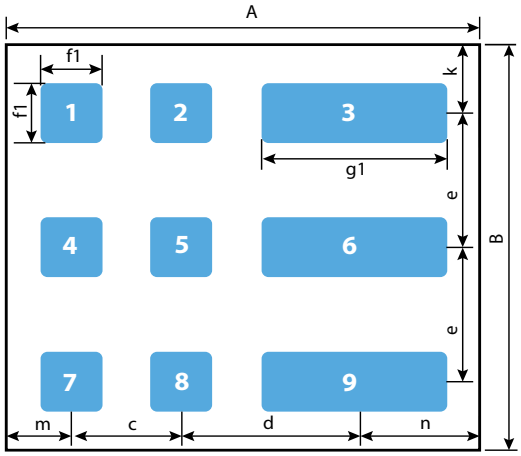



| DIM | MICROMETERS MIN | Nominal | MAX |
|---|---|---|---|
| A | 1630 | 1650 | 1690 |
| B | 1430 | 1460 | 1490 |
| c | | 400 | |
| d | | 622.5 | |
| e | | 500 | |
| f | 205 | 225 | 445 |
| g | 650 | 670 | 690 |
| k | | 230 | |
| m | | 207.5 | |
| n | | 430 | |

Pad 1 is $V_{IN}$
Pad 2 is EN
Pads 3, 5, and 9 are Source
Pad 4 is $A_{GND}$
Pad 6 is D
Pad 7 is $V_{DD10}$ (Final version may undergo improvement to eliminate 10 V)
Pad 8 is $V_{DD5}$

## RECOMMENDED LAND PATTERN

*(units in µm)*

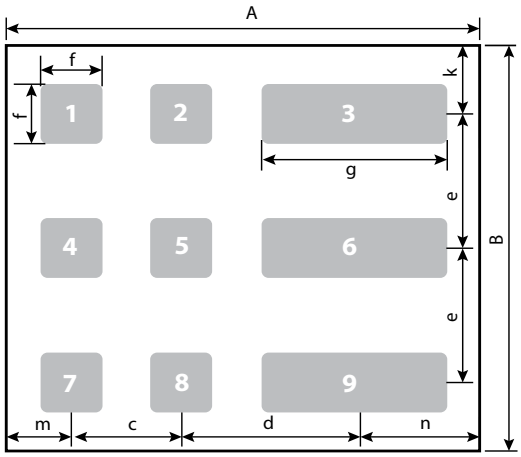



| DIM | MICROMETERS |
|---|---|
| **A** | 1650 |
| **B** | 1460 |
| **c** | 400 |
| **d** | 622.5 |
| **e** | 500 |
| **f** | 205 |
| **g** | 650 |
| **k** | 230 |
| **m** | 207.5 |
| **n** | 430 |

Pad 1 is $V_{IN}$
Pad 2 is EN
Pads 3, 5 and 9 are Source
Pad 4 is $A_{GND}$
Pad 6 is D
Pad 7 is $V_{DD10}$
Pad 8 is $V_{DD5}$

## RECOMMENDED STENCIL DRAWING

*(measurements in µm)*




| DIM | MICROMETERS |
|---|---|
| **A** | 1650 |
| **B** | 1460 |
| **c** | 400 |
| **d** | 622.5 |
| **e** | 500 |
| **f** | 205 |
| **g** | 650 |
| **k** | 230 |
| **m** | 207.5 |
| **n** | 430 |

Recommended stencil should be 4mil (100 µm) thick, must be laser cut, opening per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
https://epc-co.com/epc/design-support/assemblybasics