EPC2204 – Enhancement Mode Power Transistor

\[ \begin{align*} V_{DS}, & \quad 100 \text{ V} \\
R_{DS(on)}, & \quad 6 \text{ m}\Omega \\
I_D, & \quad 29 \text{ A} \end{align*} \]

Gallium Nitride’s exceptionally high electron mobility and low temperature coefficient allows very low \( R_{DS(on)} \) while its lateral device structure and majority carrier diode provide exceptionally low \( Q_G \) and zero \( Q_{RR} \). The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
<td>Drain-to-Source Voltage (Continuous)</td>
<td>100</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Drain-to-Source Voltage (up to 10,000 S ms pulses at 150 °C)</td>
<td>120</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_D )</td>
<td>Continuous ((T_A = 25°C))</td>
<td>29</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pulsed ((25°C, T_{PULSE} = 300 \mu s))</td>
<td>125</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-to-Source Voltage</td>
<td>6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gate-to-Source Voltage</td>
<td>-4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
<td>Drain-to-Source Voltage (Continuous)</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Drain-to-Source Voltage (up to 10,000 S ms pulses at 150 °C)</td>
<td>120</td>
</tr>
<tr>
<td>( I_D )</td>
<td>Continuous ((T_A = 25°C))</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td>Pulsed ((25°C, T_{PULSE} = 300 \mu s))</td>
<td>125</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-to-Source Voltage</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>Gate-to-Source Voltage</td>
<td>-4</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating Temperature</td>
<td>-40 to 150</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>-40 to 150</td>
</tr>
</tbody>
</table>

## Thermal Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{BIC} )</td>
<td>Thermal Resistance, Junction-to-Case</td>
<td>1</td>
</tr>
<tr>
<td>( R_{BBB} )</td>
<td>Thermal Resistance, Junction-to-Board</td>
<td>2.5</td>
</tr>
<tr>
<td>( R_{BJA} )</td>
<td>Thermal Resistance, Junction-to-Ambient ((Note 1))</td>
<td>64</td>
</tr>
</tbody>
</table>

Note 1: \( R_{BJA} \) is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://lead.me/EPC2204
Dynamic Characteristics\(^*\) (\(T_J = 25°C\) unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{iss}) Input Capacitance</td>
<td>(V_{DS} = 50 \text{ V} ), (V_{GS} = 0 \text{ V})</td>
<td>644</td>
<td>851</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(C_{rss}) Reverse Transfer Capacitance</td>
<td></td>
<td>2.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{oss}) Output Capacitance</td>
<td></td>
<td>304</td>
<td>456</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{oss(ER)}) Effective Output Capacitance, Energy Related (Note 2)</td>
<td>(V_{DS} = 0) to (50 \text{ V}), (V_{GS} = 0 \text{ V})</td>
<td>401</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{oss(TR)}) Effective Output Capacitance, Time Related (Note 3)</td>
<td>(V_{DS} = 0 \text{ V} ), (V_{GS} = 0 \text{ V})</td>
<td>501</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_G) Gate Resistance</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(Q_G) Total Gate Charge</td>
<td>(V_{DS} = 50 \text{ V} ), (V_{GS} = 5 \text{ V} ), (I_D = 16 \text{ A})</td>
<td>5.7</td>
<td>7.4</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{gs}) Gate-to-Source Charge</td>
<td>(V_{DS} = 50 \text{ V} ), (V_{GS} = 5 \text{ V} ), (I_D = 16 \text{ A})</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{gd}) Gate-to-Drain Charge</td>
<td>(V_{DS} = 50 \text{ V} ), (I_D = 16 \text{ A})</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{g(th)}) Gate Charge at Threshold</td>
<td>(V_{DS} = 50 \text{ V} ), (I_D = 16 \text{ A})</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{oss}) Output Charge</td>
<td>(V_{DS} = 50 \text{ V} ), (V_{GS} = 0 \text{ V})</td>
<td>25</td>
<td>38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Q_{RR}) Source-Drain Recovery Charge</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\* Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: \(C_{oss(ER)}\) is a fixed capacitance that gives the same stored energy as \(C_{oss}\) while \(V_{DS}\) is rising from 0 to 50% \(BV_{DSS}\).

Note 3: \(C_{oss(TR)}\) is a fixed capacitance that gives the same charging time as \(C_{oss}\) while \(V_{DS}\) is rising from 0 to 50% \(BV_{DSS}\).
Figure 5a: Typical Capacitance (Linear Scale)

- **Capacitance (pF)**
  - **Figure 5a**: Typical Capacitance (Linear Scale)
  - **VDS** – Drain-to-Source Voltage (V)
  - **COSS = CGD + CSD**
  - **CISS = CGD + CGS**
  - **CRSS = CGD**

Figure 5b: Typical Capacitance (Log Scale)

- **Capacitance (pF)**
  - **Figure 5b**: Typical Capacitance (Log Scale)
  - **VDS** – Drain-to-Source Voltage (V)
  - **COSS = CGD + CSD**
  - **CISS = CGD + CGS**
  - **CRSS = CGD**

Figure 6: Typical Output Charge and COSS Stored Energy

- **QOSS – Output Charge (nC)**
- **EOSS – COSS Stored Energy (µJ)**

Figure 7: Typical Gate Charge

- **QG – Gate Charge (nC)**
- **VGS = 0 V**
- **VGS = 5 V**

Figure 8: Reverse Drain-Source Characteristics

- **ISD – Source-to-Drain Current (A)**
- **VSD – Source-to-Drain Voltage (V)**
- **ID = 16 A**
- **VGS = 50 V**

Figure 9: Normalized On-State Resistance vs. Temperature

- **Normalized On-State Resistance RDS(on)**
- **TJ – Junction Temperature (°C)**
- **ID = 16 A**
- **VGS = 5 V**

**Note:** Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.
**Figure 10: Normalized Threshold Voltage vs. Temperature**

[Graph showing normalized threshold voltage vs. temperature with a note: \( I_D = 4 \text{ mA} \)]

**Figure 11: Safe Operating Area**

[Graph showing safe operating area with a note: \( V_{DS} \) - Drain-Source Voltage (V) limited by \( R_{DS(on)} \)]

**Figure 12: Transient Thermal Response Curves**

**Junction-to-Board**

- Duty Cycle: 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- Notes: Duty Factor: \( D = \frac{t_1}{t_2} \)
- Peak \( T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B \)

**Junction-to-Case**

- Duty Cycle: 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- Notes: Duty Factor: \( D = \frac{t_1}{t_2} \)
- Peak \( T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C \)
**Tape and Reel Configuration**

4 mm pitch, 8 mm wide tape on 7” reel

**Die Markings**

Die orientation dot

Gate Pad bar is under this corner

**Die Outline**

Solder Bump View

Seating plane

**Dimension (mm)**

<table>
<thead>
<tr>
<th>EPC2204 (Note 1)</th>
<th>Target</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>8.00</td>
<td>7.90</td>
<td>8.30</td>
</tr>
<tr>
<td>b</td>
<td>1.75</td>
<td>1.65</td>
<td>1.85</td>
</tr>
<tr>
<td>c (Note 2)</td>
<td>3.50</td>
<td>3.45</td>
<td>3.55</td>
</tr>
<tr>
<td>d</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>e</td>
<td>4.00</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>f (Note 2)</td>
<td>2.00</td>
<td>1.95</td>
<td>2.05</td>
</tr>
<tr>
<td>g</td>
<td>1.50</td>
<td>1.50</td>
<td>1.60</td>
</tr>
<tr>
<td>h</td>
<td>0.50</td>
<td>0.45</td>
<td>0.55</td>
</tr>
</tbody>
</table>

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

**Micrometers**

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>Nominal</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2470</td>
<td>2500</td>
<td>2530</td>
</tr>
<tr>
<td>B</td>
<td>1470</td>
<td>1500</td>
<td>1530</td>
</tr>
<tr>
<td>c</td>
<td>1155</td>
<td>1175</td>
<td>1195</td>
</tr>
<tr>
<td>d</td>
<td>1330</td>
<td>1350</td>
<td>1370</td>
</tr>
<tr>
<td>e</td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f</td>
<td>230</td>
<td>250</td>
<td>270</td>
</tr>
<tr>
<td>g</td>
<td>280</td>
<td>300</td>
<td>320</td>
</tr>
<tr>
<td>h</td>
<td>805</td>
<td>825</td>
<td>845</td>
</tr>
<tr>
<td>j</td>
<td>787.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>k</td>
<td>225</td>
<td></td>
<td></td>
</tr>
<tr>
<td>m</td>
<td>250</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Pad 1 is Gate:
Pads 2, 4, 6 are Source;
Pads 3, 5 are Drain

Note: Dimensions d and c are centered.
**RECOMMENDED LAND PATTERN**  
(Units in µm)

Land pattern is solder mask defined

<table>
<thead>
<tr>
<th>DIM</th>
<th>Nominal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2500</td>
</tr>
<tr>
<td>B</td>
<td>1500</td>
</tr>
<tr>
<td>c1</td>
<td>1155</td>
</tr>
<tr>
<td>d1</td>
<td>1330</td>
</tr>
<tr>
<td>e</td>
<td>500</td>
</tr>
<tr>
<td>f1</td>
<td>230</td>
</tr>
<tr>
<td>g1</td>
<td>280</td>
</tr>
<tr>
<td>h1</td>
<td>805</td>
</tr>
<tr>
<td>j</td>
<td>787.5</td>
</tr>
<tr>
<td>k</td>
<td>225</td>
</tr>
<tr>
<td>m</td>
<td>250</td>
</tr>
</tbody>
</table>

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at [https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx](https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx)