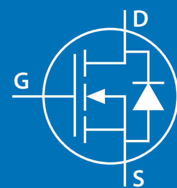
EPC2207 – Enhancement Mode Power Transistor

V_{DS} , 200 V
$R_{DS(on)}$, 22 mΩ
I_D , 14 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised July 15, 2022

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

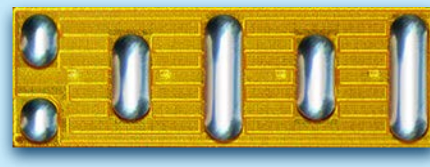
Maximum Ratings			
	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous (T_A = 25°C)	14	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	54	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
	PARAMETER	TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	1.4	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	5.1	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	72	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.2 mA	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 160 V		0.05	0.16	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	1.3	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.16	2.9	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.05	0.16	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 14 A		15	22	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

Defined by design. Not subject to production test.



Die Size: 2.8 x 0.9 mm

EPC2207 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC converters
- BLDC motor drives
- Sync rectification for AC/DC and DC-DC
- Multi-level AC/DC power supplies
- Wireless power
- Solar micro-inverters
- Robotics
- Class-D audio

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2207

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		454	600	pF
C_{RSS}	Reverse Transfer Capacitance			0.7		
C_{OSS}	Output Capacitance			130	195	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 100 V, V_{GS} = 0 V		186		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			234		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 5 V, I_D = 14 A		4.5	5.9	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 100 V, I_D = 14 A		1.3		
Q_{GD}	Gate-to-Drain Charge			0.7		
$Q_{G(TH)}$	Gate Charge at Threshold			0.8		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		23	35	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

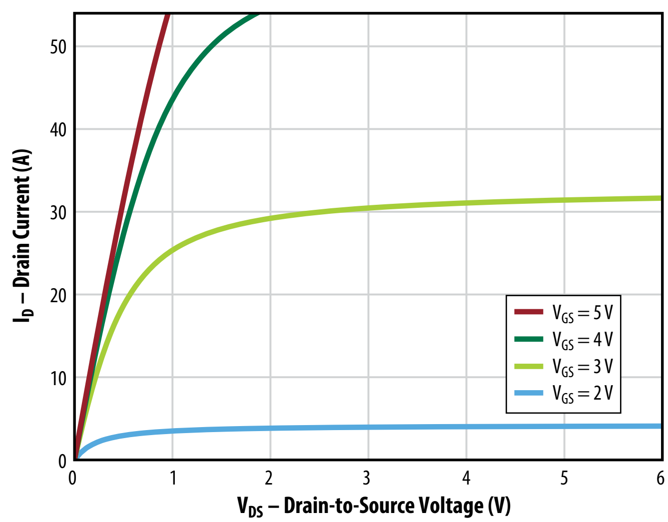


Figure 2: Typical Transfer Characteristics

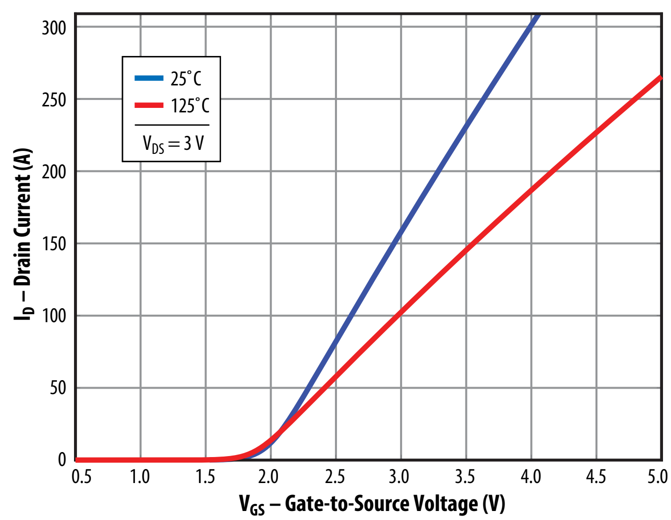


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

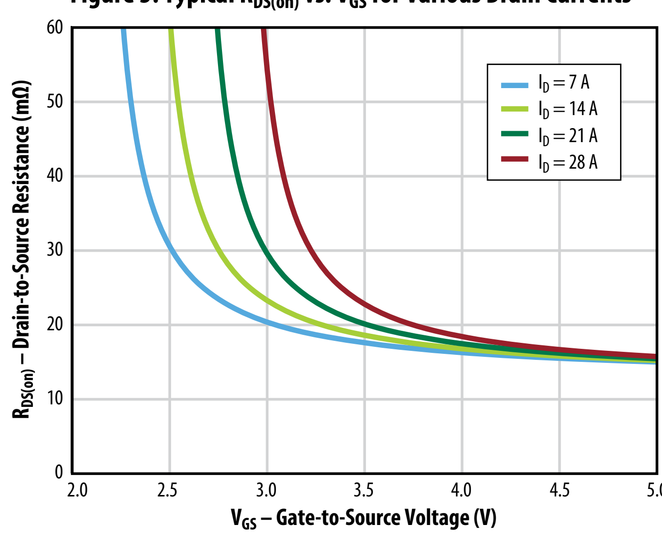


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

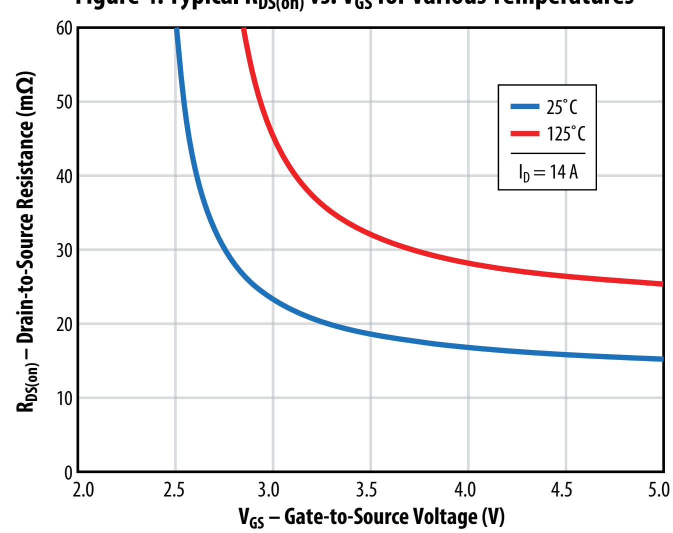


Figure 5a: Typical Capacitance (Linear Scale)

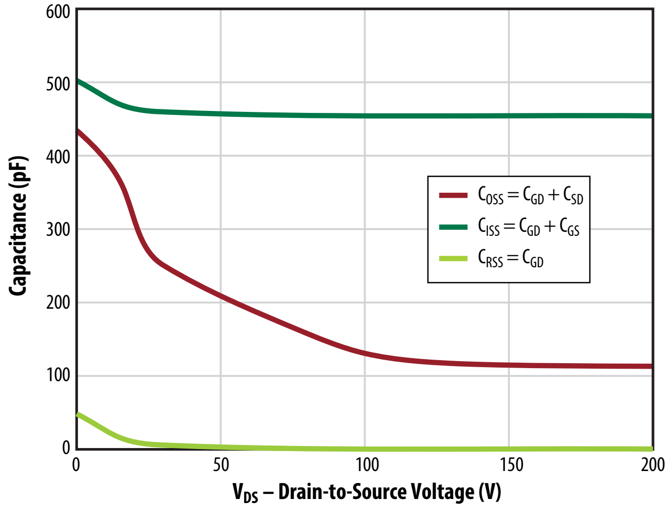


Figure 5b: Typical Capacitance (Log Scale)

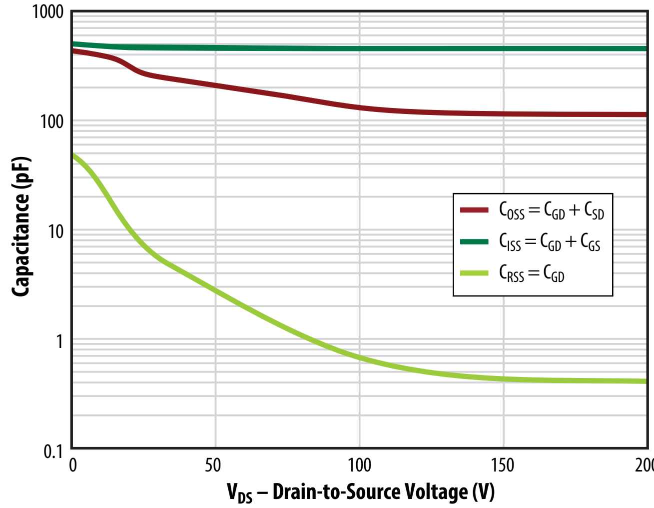


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

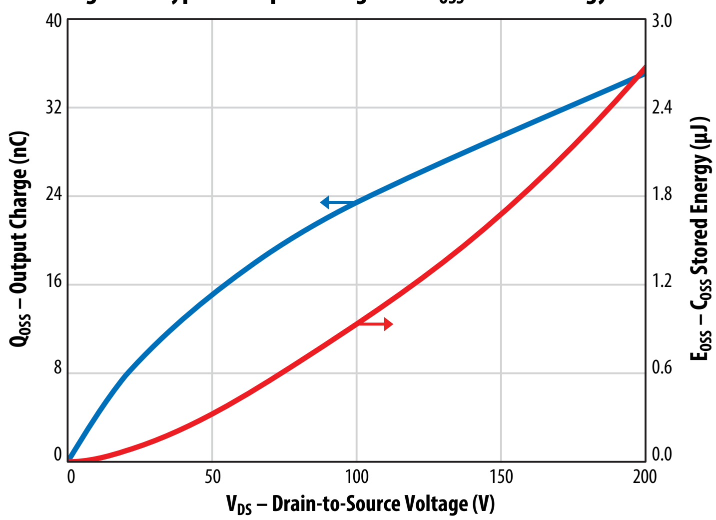


Figure 7: Typical Gate Charge

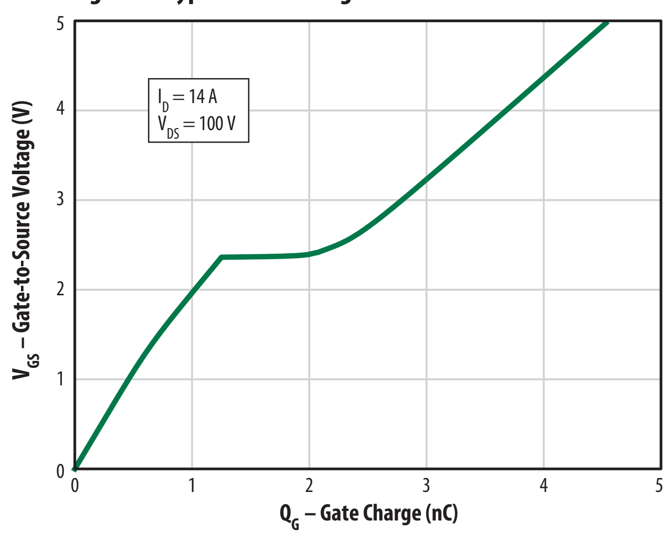
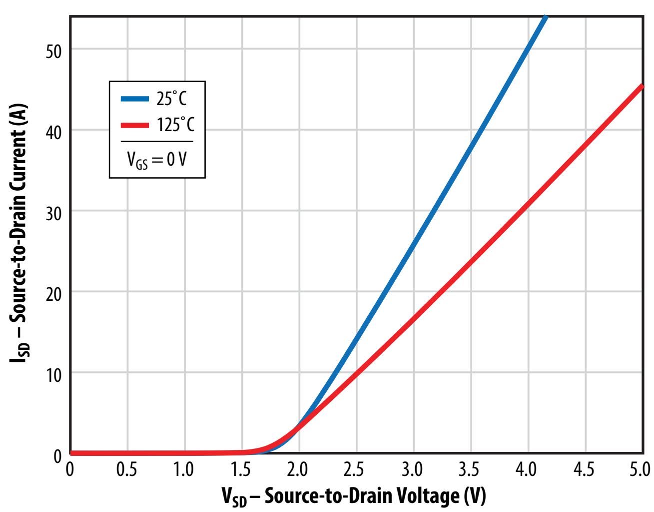


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

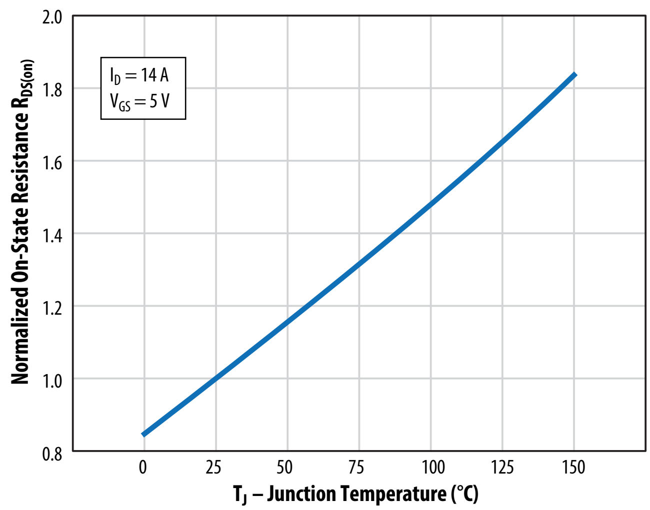


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

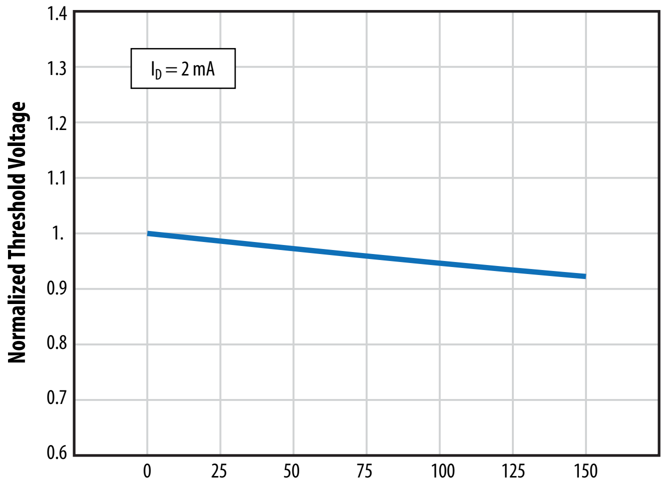
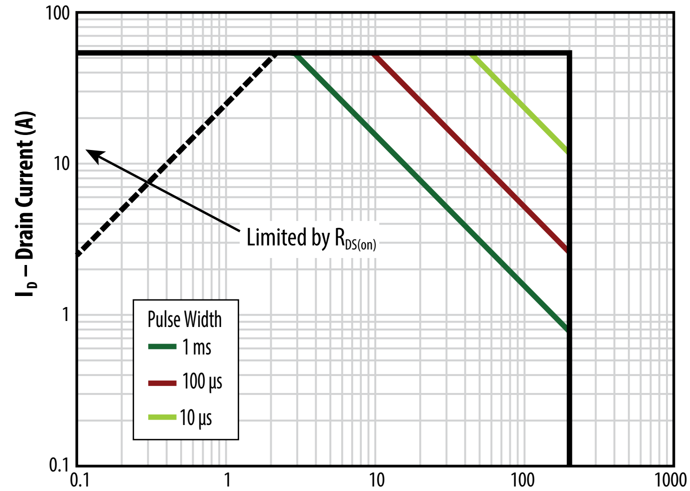


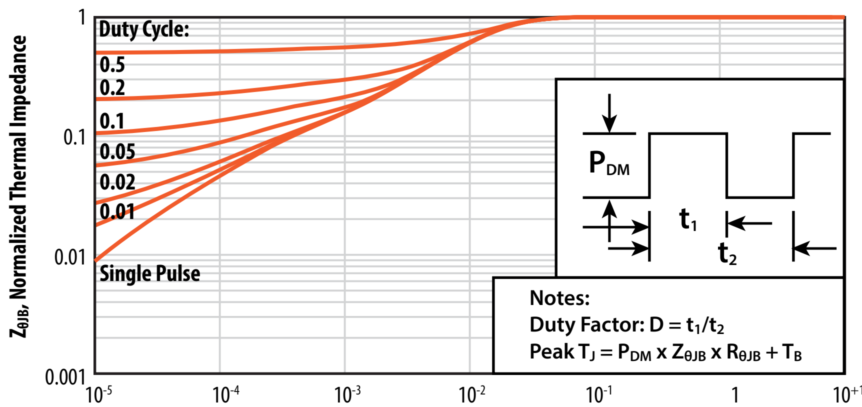
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

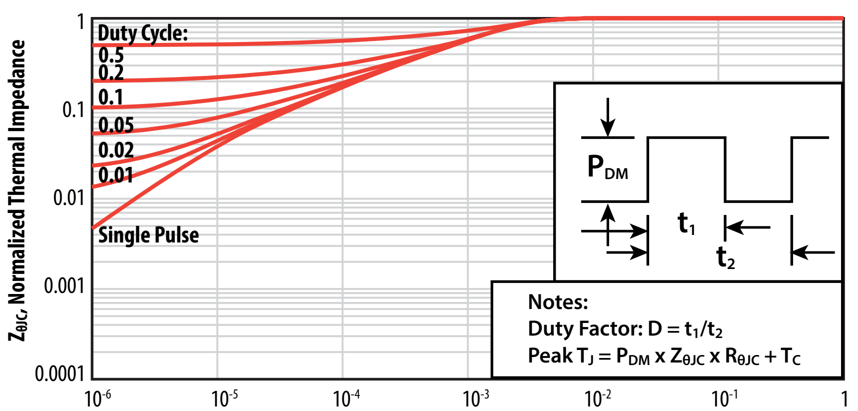
Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board



t_1, Rectangular Pulse Duration, seconds

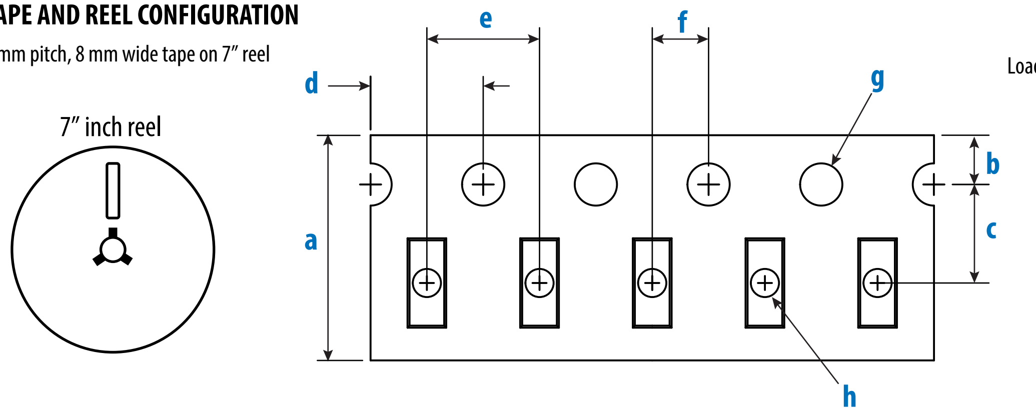
Junction-to-Case

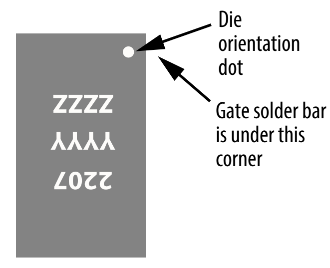


t_1, Rectangular Pulse Duration, seconds

TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel





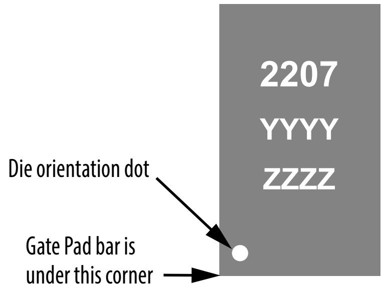
Die is placed into pocket solder bar side down (face side down)

EPC2207 (Note 1)	Dimension (mm) Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.00	1.00	1.25

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

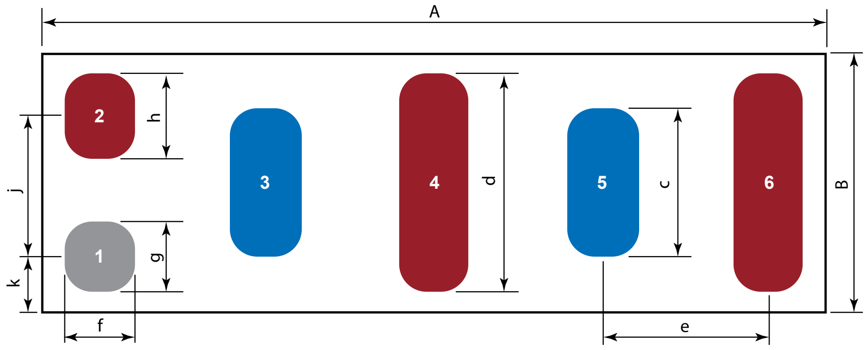
DIE MARKINGS



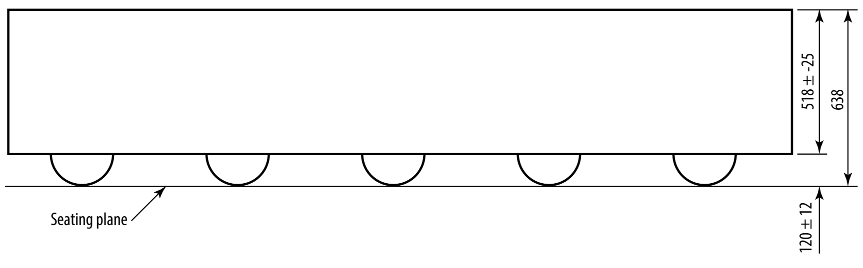
Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2207	2207	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



Side View



DIM	Micrometers MIN	Nominal	MAX
A	2770	2800	2830
B	895	925	955
c		535	
d		775	
e		600	
f		250	
g		250	
h		300	
j		500	
k		200	

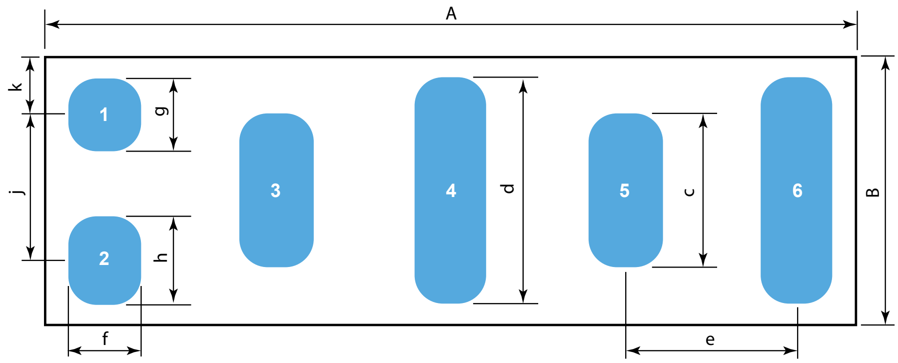
Pad 1 is Gate;

Pads 2 ,4, 6 are Source;

Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined.

DIM	Nominal
A	2800
B	925
c	535
d	775
e	600
f	250
g	250
h	300
j	500
k	200

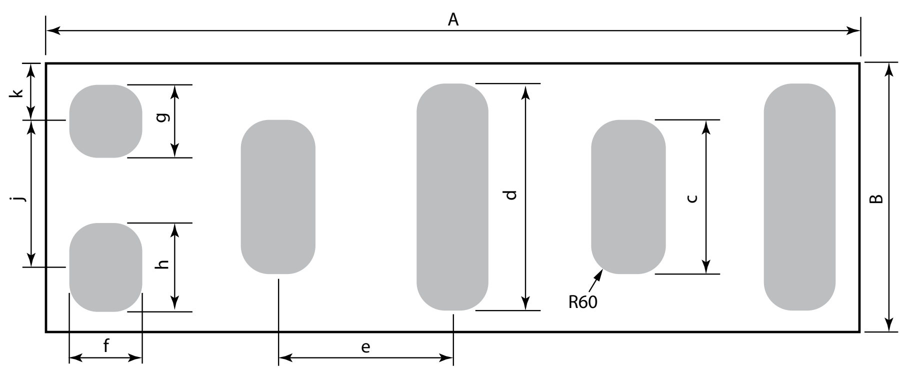
Pad 1 is Gate;

Pads 2 ,4, 6 are Source;

Pads 3, 5 are Drain

RECOMMENDED STENCIL DRAWING

(units in µm)



DIM	Nominal
A	2800
B	925
c	535
d	775
e	600
f	250
g	250
h	300
j	500
k	200

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at https://epc-co.com/epc/design-support