eGaN® FET DATASHEET

EPC2215 – Enhancement Mode Power Transistor

$V_{DS}$, 200 V
$R_{DS(on)}$, 8 mΩ
$I_D$, 32 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

### Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$ Drain-to-Source Voltage (Continuous)</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$ Continuous ($T_A = 25°C$)</td>
<td>32</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed ($25°C$, $T_{PULSE} = 300 \mu s$)</td>
<td>162</td>
<td></td>
</tr>
<tr>
<td>$V_{GS}$ Gate-to-Source Voltage</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Gate-to-Source Voltage</td>
<td>-4</td>
<td></td>
</tr>
<tr>
<td>$T_J$ Operating Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$ Storage Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Thermal Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OJC}$ Thermal Resistance, Junction-to-Case</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{OJB}$ Thermal Resistance, Junction-to-Board</td>
<td>2.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{OJA}$ Thermal Resistance, Junction-to-Ambient (Note 1)</td>
<td>52</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: $R_{OJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

### Static Characteristics ($T_J = 25°C$ unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B V_{DSS}$ Drain-to-Source Voltage</td>
<td>$V_{GS} = 0 V, I_D = 0.6 mA$</td>
<td>200</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{SSS}$ Drain-Source Leakage</td>
<td>$V_{GS} = 0 V, V_{DS} = 160 V$</td>
<td></td>
<td>0.15</td>
<td>0.48</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{GS}$ Gate-to-Source Forward Leakage</td>
<td>$V_{GS} = 5 V$</td>
<td></td>
<td>0.03</td>
<td>3.8</td>
<td></td>
</tr>
<tr>
<td>Gate-to-Source Forward Leakage*</td>
<td>$V_{GS} = 5 V, T_J = 125°C$</td>
<td></td>
<td>0.5</td>
<td>8.7</td>
<td></td>
</tr>
<tr>
<td>Gate-to-Source Reverse Leakage</td>
<td>$V_{GS} = -4 V$</td>
<td></td>
<td>0.15</td>
<td>0.48</td>
<td></td>
</tr>
<tr>
<td>$V_{GS(TH)}$ Gate Threshold Voltage</td>
<td>$V_{DS} = V_{GS}, I_D = 6 mA$</td>
<td>0.8</td>
<td>1.1</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$ Drain-Source On Resistance</td>
<td>$V_{GS} = 5 V, I_D = 20 A$</td>
<td></td>
<td>6</td>
<td>8</td>
<td>mΩ</td>
</tr>
<tr>
<td>$V_{SD}$ Source-Drain Forward Voltage</td>
<td>$I_S = 0.5 A, V_{GS} = 0 V$</td>
<td></td>
<td>1.6</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

* Defined by design. Not subject to production test.
Dynamic Characteristics (TJ = 25°C unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>Typ</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ciss</td>
<td>VDS = 100 V, VGS = 0 V</td>
<td>1356</td>
<td>1790</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Cress</td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cooss</td>
<td></td>
<td>390</td>
<td>585</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cooss(ER)</td>
<td>VDS = 0 to 100 V, VGS = 0 V</td>
<td>556</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cooss(TR)</td>
<td></td>
<td>699</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RG</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>QG</td>
<td>VDS = 100 V, VGS = 5 V, ID = 20 A</td>
<td>13.6</td>
<td>17.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Qgs</td>
<td></td>
<td>3.3</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Qgd</td>
<td>VDS = 100 V, ID = 20 A</td>
<td>2.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Qg(TH)</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Qoss</td>
<td>VDS = 100 V, VGS = 0 V</td>
<td>69</td>
<td>104</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Qrr</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# Defined by design. Not subject to production test.

Note 2: Cooss(ER) is a fixed capacitance that gives the same stored energy as Cooss while VGS is rising from 0 to 50% BVDS.

Note 3: Cooss(TR) is a fixed capacitance that gives the same charging time as Cooss while VGS is rising from 0 to 50% BVDS.
Figure 5a: Capacitance (Linear Scale)

\[ V_{DS} \rightarrow \text{Drain-to-Source Voltage (V)} \]

\[ \text{Capacitance (pF)} \]

\[ \begin{array}{c}
0 & 200 \\
100 & 1200 \\
150 & 1400 \\
200 & 1600 \\
\end{array} \]

\[ C_{OSS} = C_{GD} + C_{DS} \]
\[ C_{ISS} = C_{GD} + C_{GS} \]
\[ C_{RSS} = C_{GD} \]

Figure 5b: Capacitance (Log Scale)

\[ V_{DS} \rightarrow \text{Drain-to-Source Voltage (V)} \]

\[ \text{Capacitance (pF)} \]

\[ \begin{array}{c}
0 & 1000 \\
100 & 10000 \\
150 & 100000 \\
200 & 1000000 \\
\end{array} \]

Figure 6: Output Charge and \( C_{OSS} \) Stored Energy

\[ V_{DS} \rightarrow \text{Drain-to-Source Voltage (V)} \]

\[ Q_{OSS} \rightarrow \text{Output Charge (nC)} \]

\[ E_{OSS} \rightarrow \text{COSS Stored Energy (µJ)} \]

Figure 7: Gate Charge

\[ V_{GS} \rightarrow \text{Gate-to-Source Voltage (V)} \]

\[ Q_{G} \rightarrow \text{Gate Charge (nC)} \]

\[ \begin{array}{c}
0 & 5 \\
1 & 4 \\
2 & 3 \\
3 & 2 \\
4 & 1 \\
\end{array} \]

\[ \begin{array}{c}
0 & 1.6 \\
1.0 & 2.0 \\
1.5 & 3.2 \\
2.0 & 4.8 \\
2.5 & 6.4 \\
3.0 & 8.0 \\
\end{array} \]

ID = 20 A
V_{DS} = 100 V

Figure 8: Reverse Drain-Source Characteristics

\[ V_{DS} \rightarrow \text{Source-to-Drain Voltage (V)} \]

\[ I_{SD} \rightarrow \text{Source-to-Drain Current (A)} \]

\[ \begin{array}{c}
0 & 0.5 \\
0.5 & 1.0 \\
1.0 & 1.5 \\
1.5 & 2.0 \\
2.0 & 2.5 \\
2.5 & 3.0 \\
3.0 & 3.5 \\
3.5 & 4.0 \\
4.0 & 4.5 \\
4.5 & 5.0 \\
\end{array} \]

\[ \begin{array}{c}
0 & 20 \\
0.5 & 40 \\
1.0 & 60 \\
1.5 & 80 \\
2.0 & 100 \\
2.5 & 120 \\
3.0 & 140 \\
3.5 & 160 \\
\end{array} \]

ID = 20 A
V_{DS} = 0 V

Figure 9: Normalized On-State Resistance vs. Temperature

\[ \begin{array}{c}
0 & 25 \\
25 & 50 \\
50 & 75 \\
75 & 100 \\
100 & 125 \\
125 & 150 \\
\end{array} \]

\[ \begin{array}{c}
0 & 0.8 \\
0.5 & 1.0 \\
1.0 & 1.2 \\
1.5 & 1.4 \\
2.0 & 1.6 \\
\end{array} \]

\[ \begin{array}{c}
ID = 20 A \quad V_{GS} = 5 V \\
\end{array} \]
Figure 10: Normalized Threshold Voltage vs. Temperature

Figure 11: Safe Operating Area

Figure 12: Transient Thermal Response Curves

- **Junction-to-Board**
  
  - **Notes:**
    - Duty Factor: \( D = \frac{t_1}{t_2} \)
    - Peak \( T_J = P_{DM} \times Z_{θJB} \times R_{θJB} + T_B \)

- **Junction-to-Case**
  
  - **Notes:**
    - Duty Factor: \( D = \frac{t_1}{t_2} \)
    - Peak \( T_J = P_{DM} \times Z_{θJC} \times R_{θJC} + T_C \)
**DIE MARKINGS**

Die orientation dot

Gate Pad bump is under this corner

**Part Number**

<table>
<thead>
<tr>
<th>Laser Markings</th>
<th>Part # Marking Line 1</th>
<th>Lot_Date Code Marking Line 2</th>
<th>Lot_Date Code Marking Line 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC2215</td>
<td>2215</td>
<td>YYYY</td>
<td>ZZZZ</td>
</tr>
</tbody>
</table>

**Die Outline**

Solder Bump View

Seating plane

**Tape and Reel Configuration**

4 mm pitch, 12 mm wide tape on 7" reel

**Die Outline**

Solder Bump View

Seating plane

**Dimension (mm)**

<table>
<thead>
<tr>
<th>EPC2215 (Note 1)</th>
<th>Target</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>12.00</td>
<td>11.90</td>
<td>12.30</td>
</tr>
<tr>
<td>b</td>
<td>1.75</td>
<td>1.65</td>
<td>1.85</td>
</tr>
<tr>
<td>c (Note 2)</td>
<td>5.50</td>
<td>5.45</td>
<td>5.55</td>
</tr>
<tr>
<td>d</td>
<td>4.00</td>
<td>3.90</td>
<td>4.00</td>
</tr>
<tr>
<td>e</td>
<td>4.00</td>
<td>3.90</td>
<td>4.00</td>
</tr>
<tr>
<td>f (Note 2)</td>
<td>2.00</td>
<td>1.95</td>
<td>2.05</td>
</tr>
<tr>
<td>g</td>
<td>1.50</td>
<td>1.50</td>
<td>1.60</td>
</tr>
<tr>
<td>h</td>
<td>1.50</td>
<td>0.95</td>
<td>1.05</td>
</tr>
</tbody>
</table>

Note 1: A moisture sensitivity level (MSL) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.
**RECOMMENDED LAND PATTERN**

(units in µm)

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**Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.**

The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at [https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx](https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx)

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**DIM**

<table>
<thead>
<tr>
<th></th>
<th>Nominal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4600</td>
</tr>
<tr>
<td>B</td>
<td>1600</td>
</tr>
<tr>
<td>c</td>
<td>1210</td>
</tr>
<tr>
<td>d</td>
<td>1450</td>
</tr>
<tr>
<td>e</td>
<td>1000</td>
</tr>
<tr>
<td>f</td>
<td>275</td>
</tr>
<tr>
<td>g</td>
<td>450</td>
</tr>
<tr>
<td>h</td>
<td>700</td>
</tr>
<tr>
<td>j</td>
<td>875</td>
</tr>
</tbody>
</table>

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**RECOMMENDED STENCIL DRAWING**

(units in µm)

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