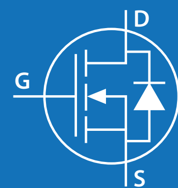
EPC2218A – Automotive 80 V (D-S) Enhancement Mode Power Transistor

V_{DS} , 80 V
$R_{DS(on)}$, 3.2 mΩ max
I_D , 60 A
AEC-Q101



EFFICIENT POWER CONVERSION

RoHS   Halogen-Free

Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate
- Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Recommended dead time (half bridge circuit) ≤ 30 ns for best efficiency
- Top of FET (back side) is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	96	
I_D	Continuous (T_A = 25°C)	60	A
	Pulsed (25°C, T_{PULSE} = 10 µs)	309	
	Pulsed (125°C, T_{PULSE} = 10 µs)	247	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

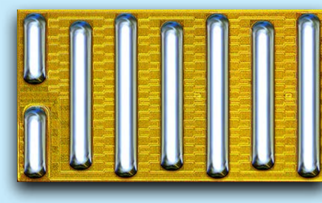
Thermal Characteristics

	PARAMETER	TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	0.5	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	1.4	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	53	

Static Characteristics (T_J = 25°C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.35 mA	80			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.08	0.35	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.02	2.3	
	Gate-to-Source Forward Leakage	V_{GS} = 6 V		0.2	2.3	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.6	9	
	Gate-to-Source Forward Leakage#	V_{GS} = 6 V, T_J = 125°C		1	9	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.06	0.4	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A		2.4	3.2	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.



Die Size: 3.5 x 1.95 mm

EPC2218A eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC converters
- BLDC motor drives
- Sync rectification for AC/DC and DC-DC
- Point of load converters
- USB-C
- Automotive lidar/ToF
- Class-D audio
- LED lighting
- eMobility

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2218A

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		1189	1570	pF
C_{RSS}	Reverse Transfer Capacitance			4.3		
C_{OSS}	Output Capacitance			562	843	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		740		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			925		
R_G	Gate Resistance			0.45		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 25 A		10.5	13.6	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 25 A		3.2		
Q_{GD}	Gate-to-Drain Charge			1.5		
$Q_{G(TH)}$	Gate Charge at Threshold			1.9		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		46	69	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C*

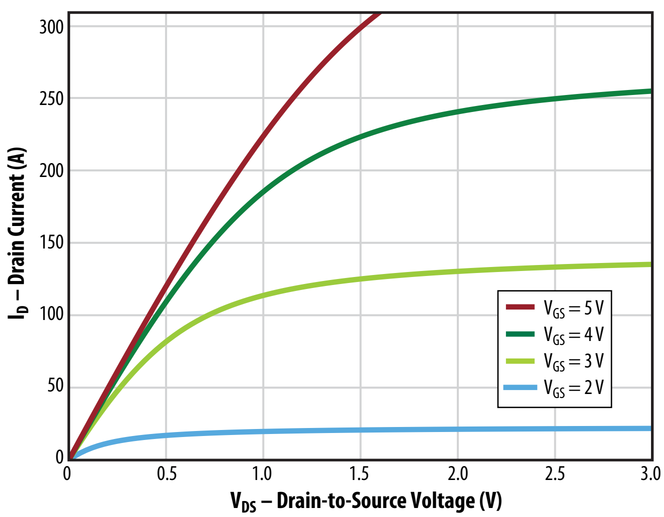


Figure 2: Typical Transfer Characteristics*

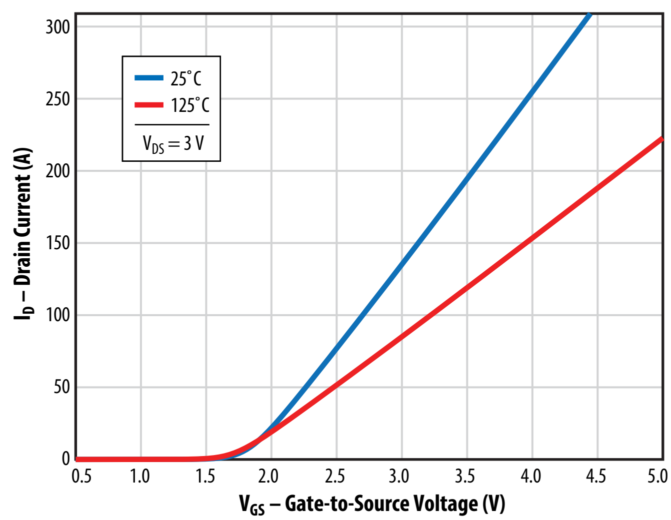


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

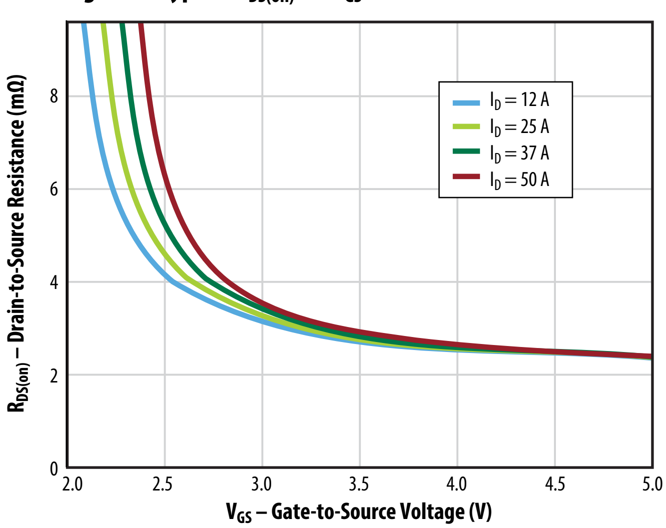
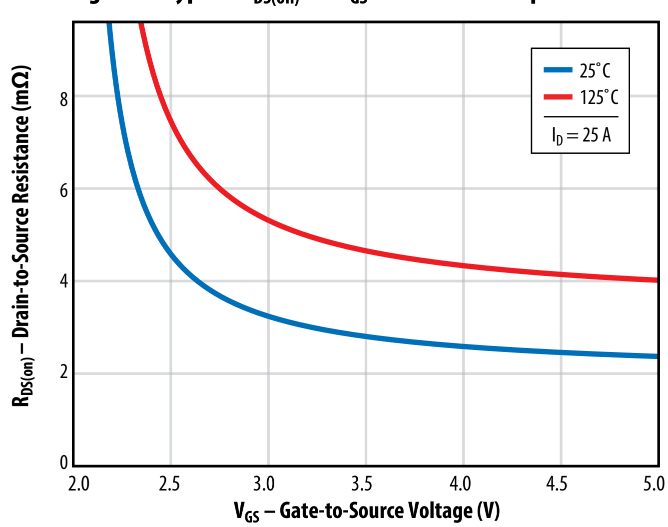


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures



* Generated based on a pulse width of 300 µs.

Figure 5a: Typical Capacitance (Linear Scale)

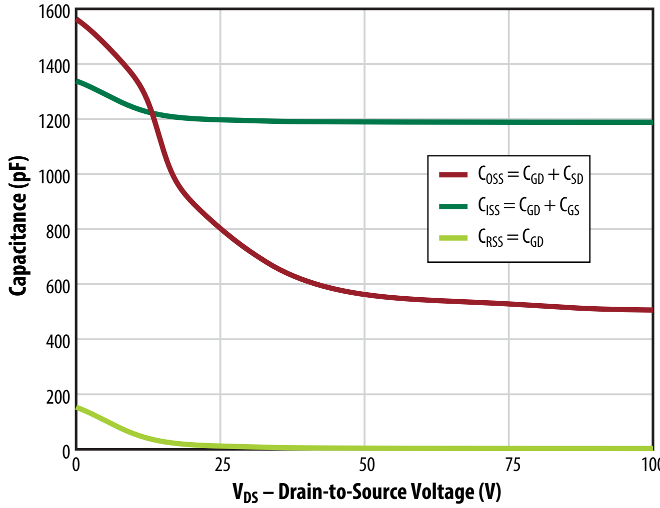


Figure 5b: Typical Capacitance (Log Scale)

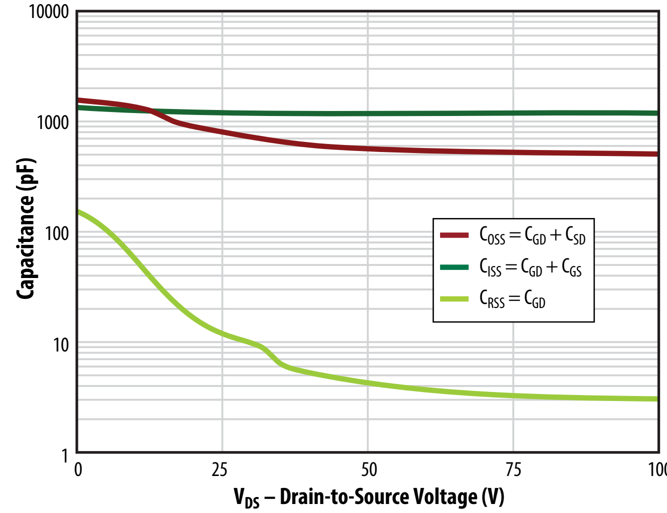


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

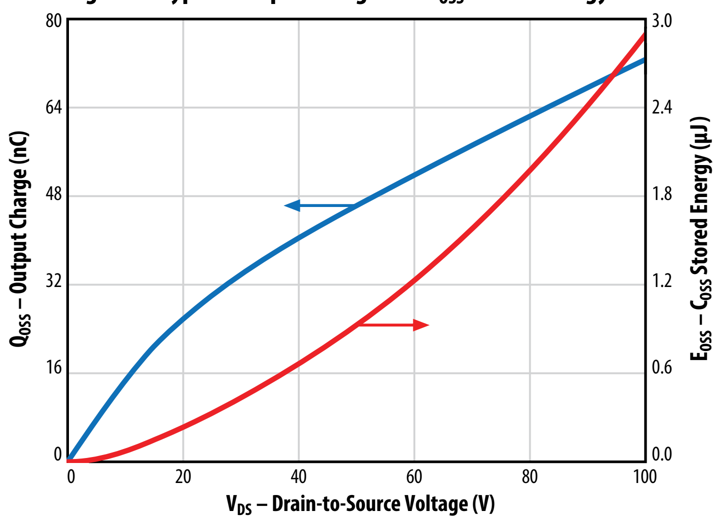


Figure 7: Typical Gate Charge

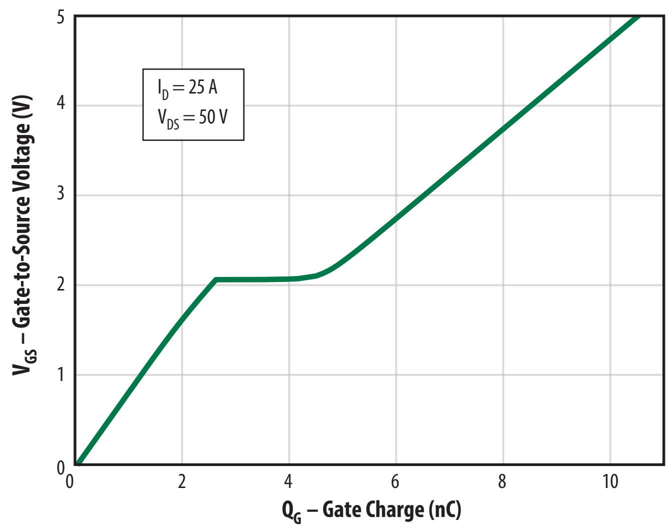
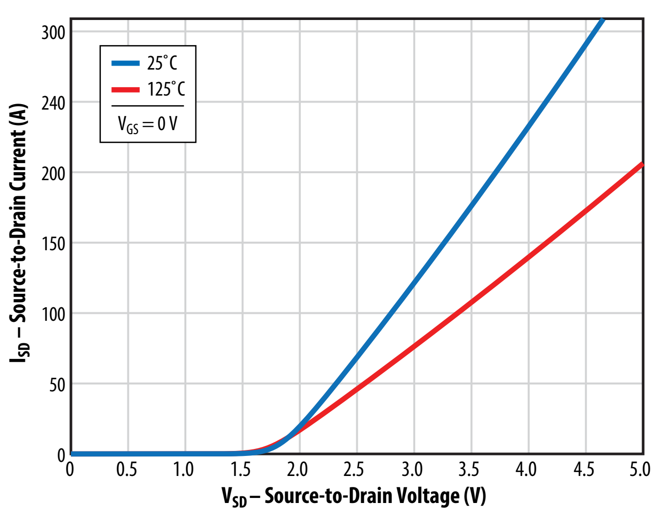


Figure 8: Typical Reverse Drain-Source Characteristics*



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.
* Generated based on a pulse width of 300 µs.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

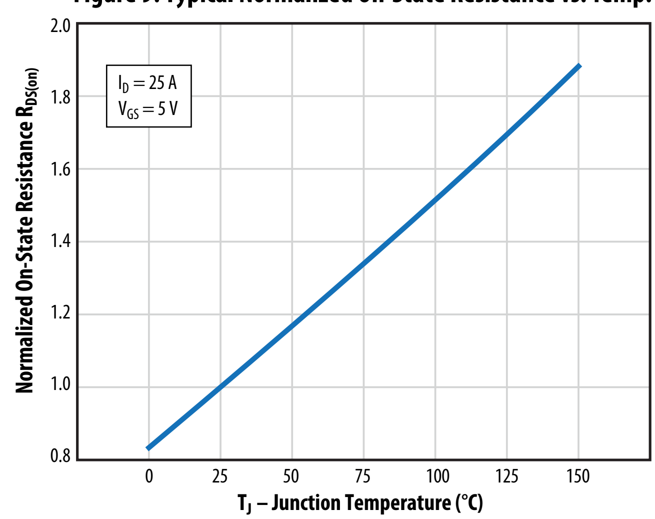


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

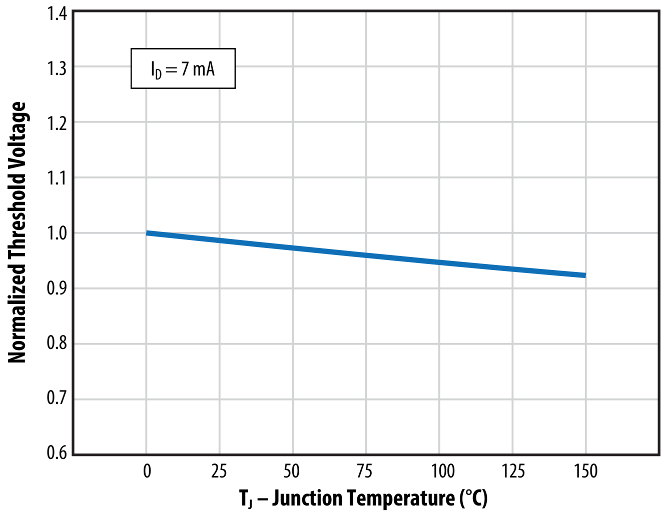
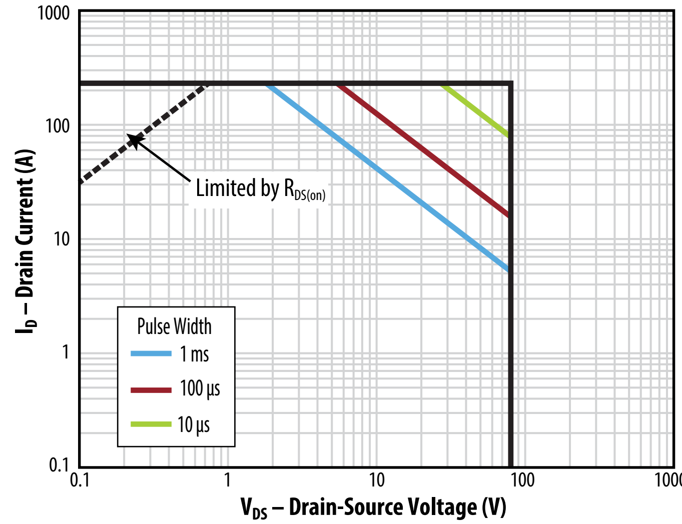


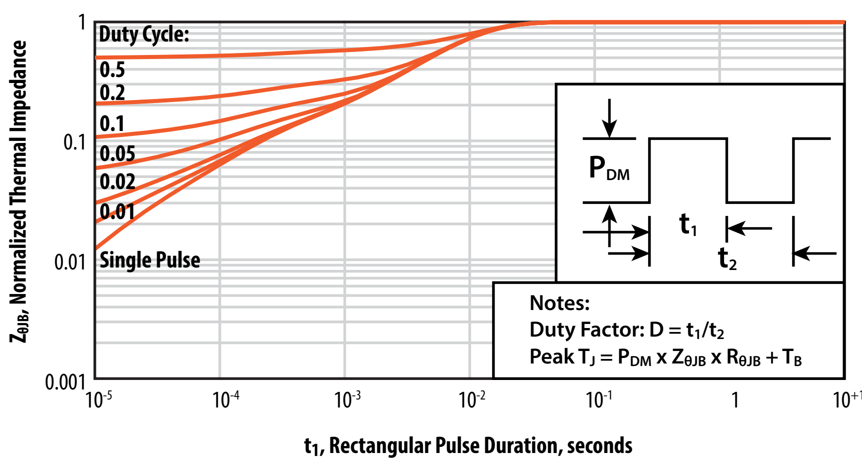
Figure 11: Safe Operating Area



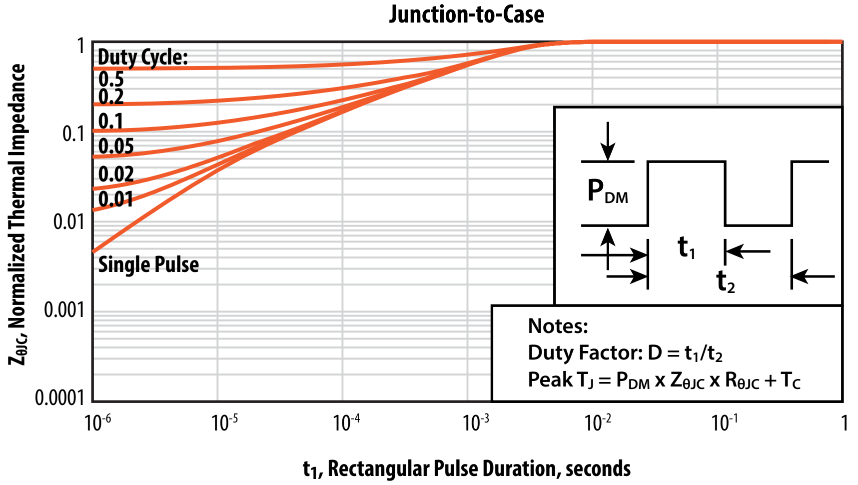
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board



Junction-to-Case



LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, or next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The **EPC90123 Half-Bridge Development Board Using EPC2218** implements our recommended vertical inner layout.

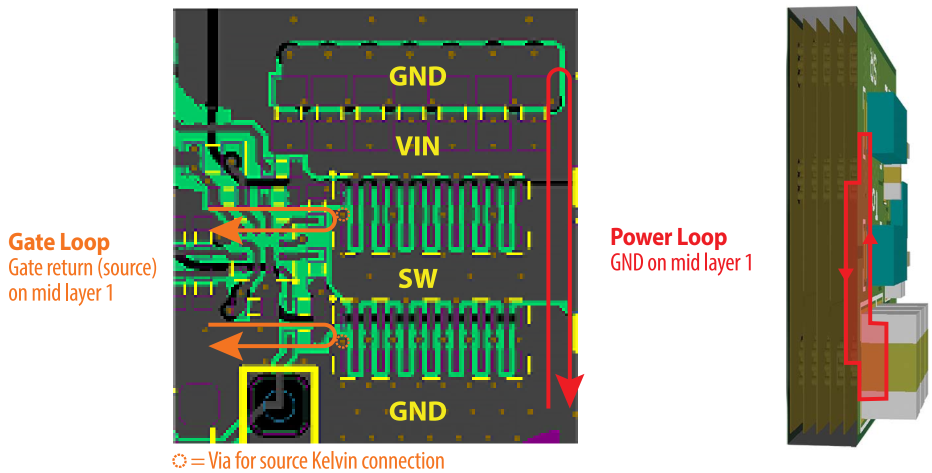


Figure 13: Inner vertical layout for power and gate loops from EPC90123

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**

TYPICAL SWITCHING BEHAVIOR

The following typical switching waveforms are captured in these conditions:

- **EPC90123 Half-Bridge Development Board Using EPC2218**
- Gate driver: uP1966E with 0.4 Ω/0.7 Ω pull-down/pull-up resistance
- External R_G(ON) = 1 Ω, R_G(OFF) = 0 Ω
- V_{IN} = 48 V, I_L = 25 A

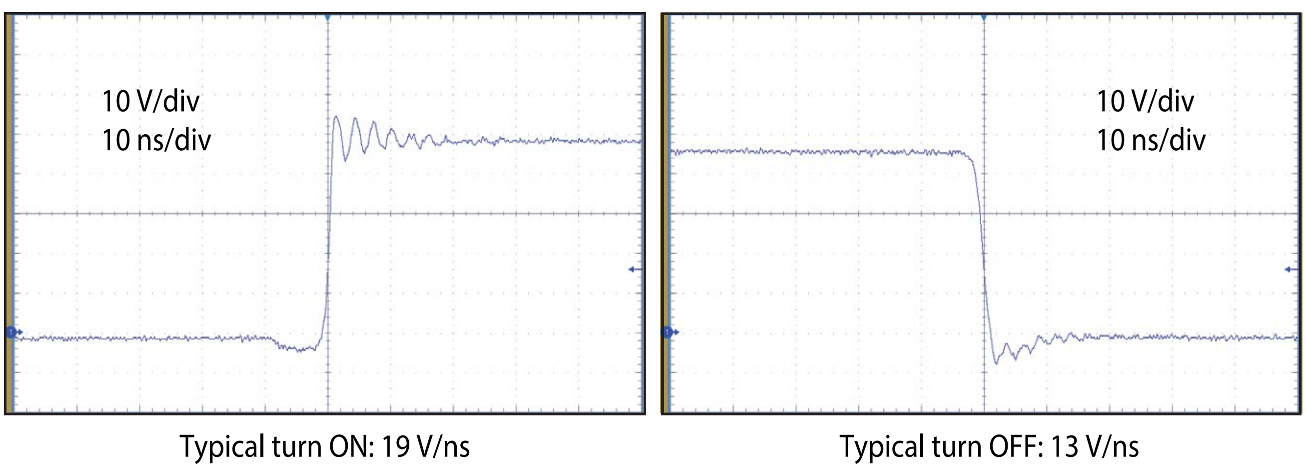


Figure 14: Typical half-bridge voltage switching waveforms

See the **EPC90123 Quick Start Guide (QSG)** for more information.

TYPICAL THERMAL CONCEPT

The EPC2088 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

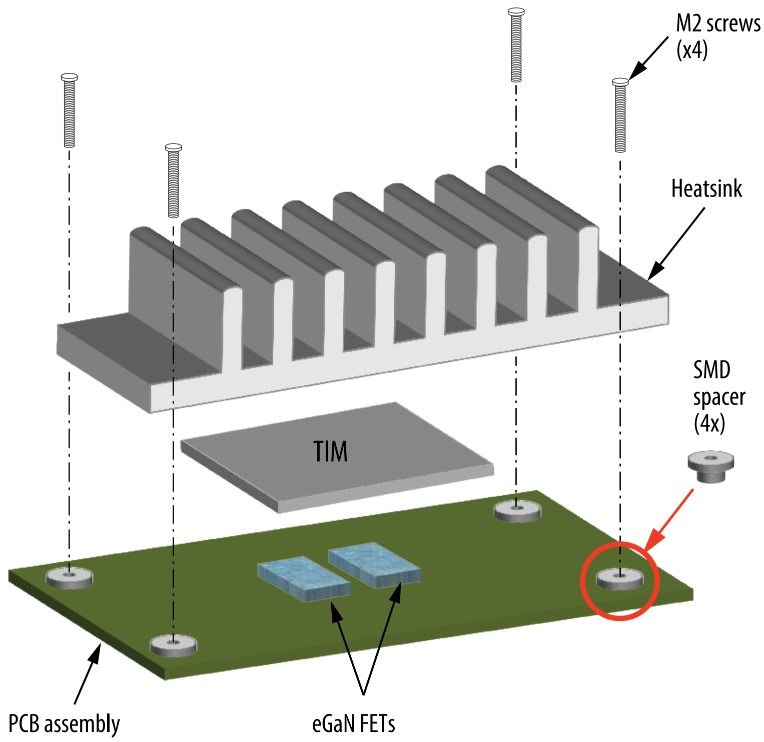


Figure 15: Exploded view of heatsink assembly using screws

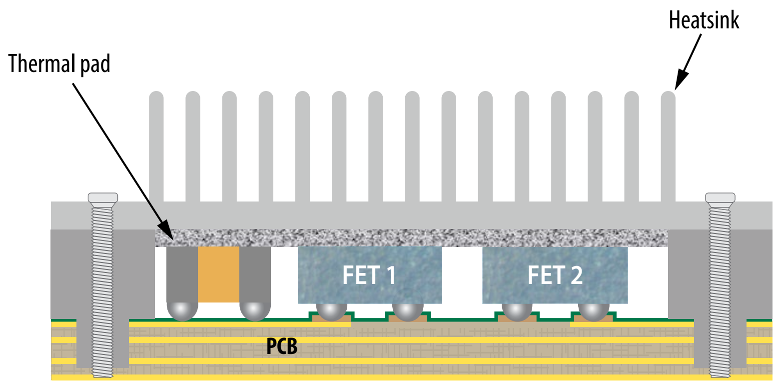


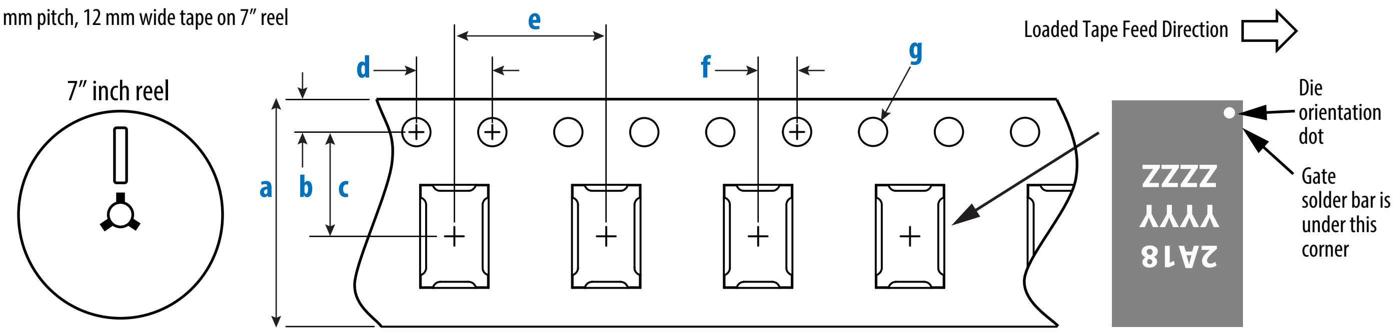
Figure 16: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

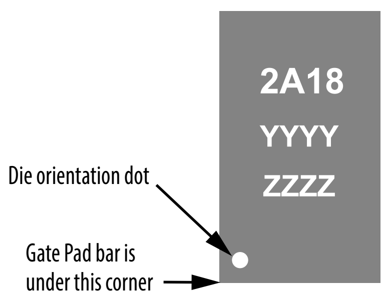


	Dimension (mm)		
EPC2218A (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

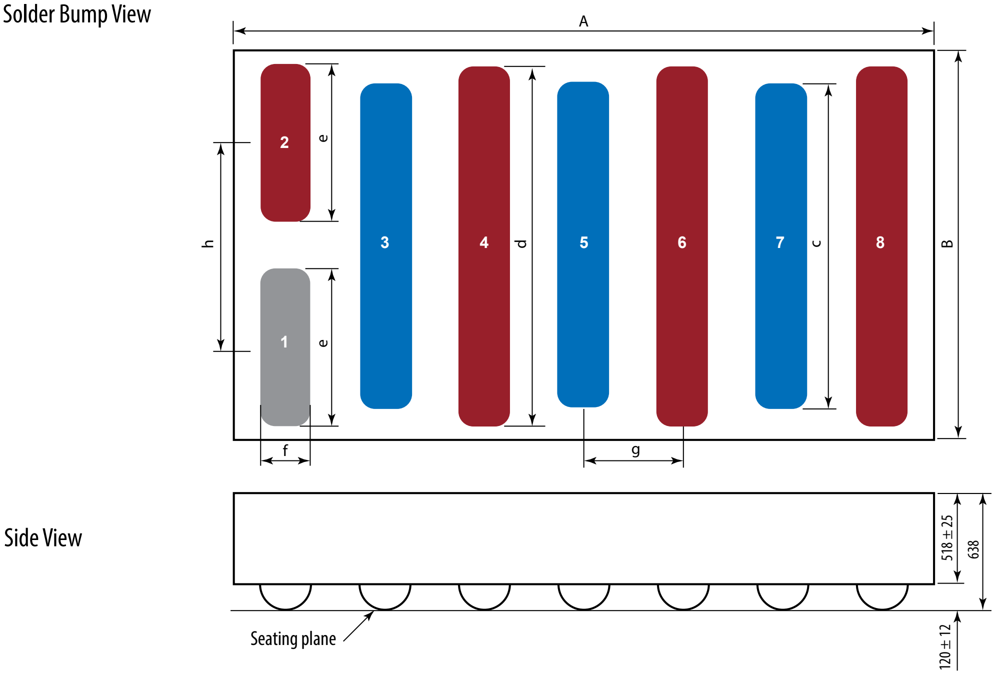
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2218A	2A18	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	3470	3500	3530
B	1920	1950	1980
c		1625	
d		1800	
e		775	
f		250	
g		500	
h		1025	

Pad 1 is Gate;

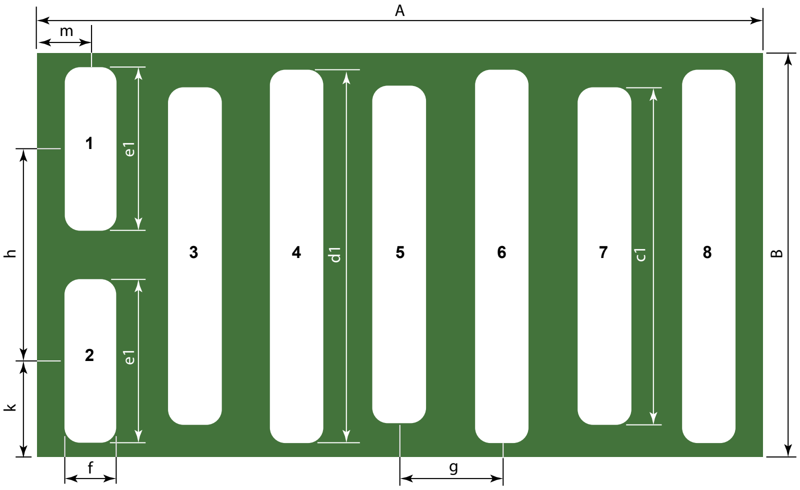
Pads 2 ,4, 6, 8 are Source;

Pads 3, 5, 7 are Drain

Substrate (top side) connected to Source

RECOMMENDED LAND PATTERN

(units in µm)



Solder mask
(for solder mask defined pads)

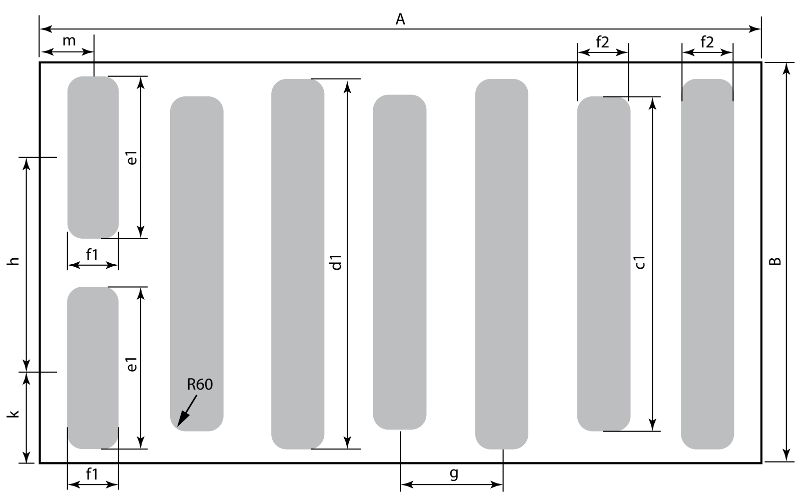
Land pattern is solder mask defined.

DIM	Nominal
A	3500
B	1950
c1	1605
d1	1780
e1	755
f	230
g	500
h	1025
k	462.5
m	250

Pad 1 is Gate;
Pads 2 ,4, 6, 8 are Source;
Pads 3, 5, 7 are Drain

RECOMMENDED STENCIL DRAWING

(units in µm)



DIM	Nominal
A	3500
B	1950
c1	1605
d1	1780
e1	755
f1	230
f2	210
g	500
h	1025

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Solder mask defined pads are recommended for best reliability.

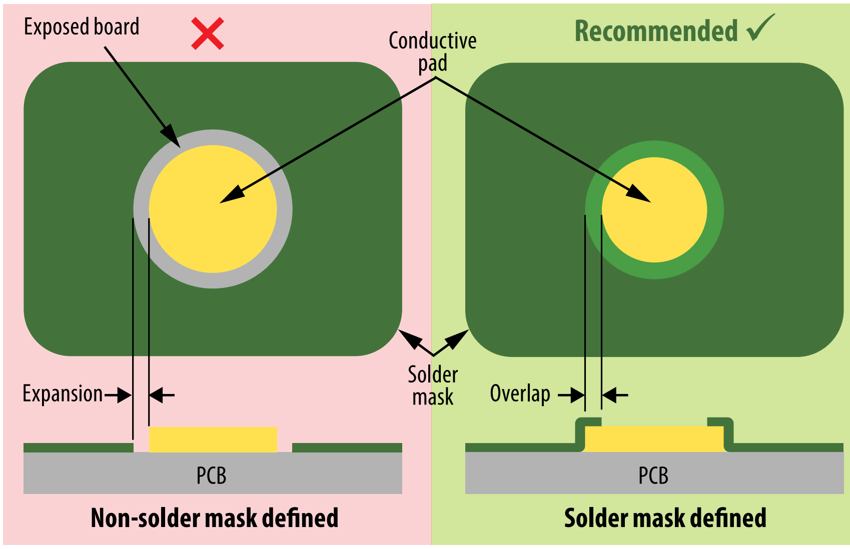


Figure 17: Solder mask defined versus non-solder mask defined pad

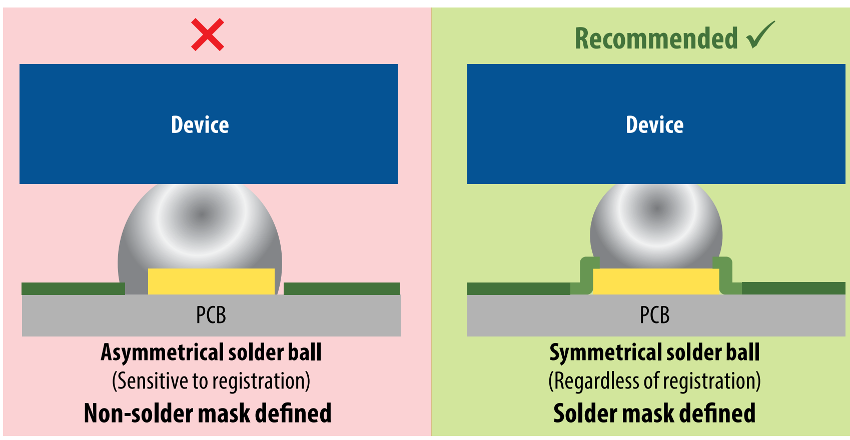


Figure 18: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)