General Description

The EPC2302 is a 1.8 mΩ max $R_{DS(on)}$ 100 V eGaN® power transistor in a low inductance 3 x 5 mm QFN package with exposed top for excellent thermal management. It is tailored to high frequency DC-DC applications to/from 40 V–60 V and 48 V BLDC motor drives.

The thermal resistance to case top is ~0.2 °C/W, resulting in excellent thermal behavior and easy cooling. The device features an enhanced PQFN “Thermal-Max” package. The exposed top enhances top-side thermal management and the side-wettable flanks guarantee that the complete side-pad surface is wetted with solder during the reflow soldering process, which protects the copper and allows soldering to occur on this external flank area for easy optical inspection.

Compared to a Si MOSFET, the footprint of 15 mm$^2$ is less than half of the size of the best-in-class Si MOSFET with similar $R_{DS(on)}$ and voltage rating, $Q_G$ and $Q_{GD}$ are significantly smaller and $Q_{RR}$ is 0. This results in lower switching losses and lower gate driver losses. Moreover, EPC2302 is very fast and can operate with deadtime less than 10 ns for higher efficiency and $Q_{RR} = 0$ is a big advantage for reliability and EMI. In summary, EPC2302 allows the highest power density due to enhanced efficiency, smaller size, and higher switching frequency for smaller inductor and fewer capacitors.

The EPC2302 enables designers to improve efficiency and save space. The excellent thermal behavior enables easier and lower cost cooling. The ultra-low capacitance and zero reverse recovery of the eGaN® FET enables efficient operation in many topologies. Performance is further enhanced due to the small, low inductance footprint.

Application notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$ Continuous ($T_A = 25^\circ$C)</td>
<td>101</td>
<td>A</td>
</tr>
<tr>
<td>$V_{GS}$ Gate-to-Source Voltage</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>$T_J$ Operating Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$ Storage Temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>
## Static Characteristics (T<sub>J</sub> = 25°C unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV&lt;sub&gt;DSS&lt;/sub&gt;</td>
<td>Drain-to-Source Voltage</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ID&lt;sub&gt;S&lt;/sub&gt;</td>
<td>Drain-Source Leakage</td>
<td>1</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IGSS</td>
<td>Gate-to-Source Forward Leakage</td>
<td>0.01</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;GSE(TH)&lt;/sub&gt;</td>
<td>Gate Threshold Voltage</td>
<td>0.8</td>
<td>1.3</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>RDS(on)</td>
<td>Drain-Source On Resistance</td>
<td>1.4</td>
<td>1.8</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>V&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>Source-to-Drain Forward Voltage</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

# Defined by design. Not subject to production test.

## Dynamic Characteristics (T<sub>J</sub> = 25°C unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sub&gt;ISS&lt;/sub&gt;</td>
<td>Input Capacitance</td>
<td>3200</td>
<td>4800</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;RSS&lt;/sub&gt;</td>
<td>Reverse Transfer Capacitance</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;OSS&lt;/sub&gt;</td>
<td>Output Capacitance</td>
<td>1000</td>
<td>1200</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>C&lt;sub&gt;OSS(ER)&lt;/sub&gt;</td>
<td>Effective Output Capacitance, Energy Related (Note 1)</td>
<td>1300</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;OSS(TR)&lt;/sub&gt;</td>
<td>Effective Output Capacitance, Time Related (Note 2)</td>
<td>1700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RG</td>
<td>Gate Resistance</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q&lt;sub&gt;G&lt;/sub&gt;</td>
<td>Total Gate Charge</td>
<td>23</td>
<td>29</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q&lt;sub&gt;Gs&lt;/sub&gt;</td>
<td>Gate-to-Source Charge</td>
<td>8.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q&lt;sub&gt;GD&lt;/sub&gt;</td>
<td>Gate-to-Drain Charge</td>
<td>2.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q&lt;sub&gt;G(TH)&lt;/sub&gt;</td>
<td>Gate Charge at Threshold</td>
<td>6.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q&lt;sub&gt;OSS&lt;/sub&gt;</td>
<td>Output Charge</td>
<td>85</td>
<td>94</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q&lt;sub&gt;RR&lt;/sub&gt;</td>
<td>Source-Drain Recovery Charge</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# Defined by design. Not subject to production test.

Note 1: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Note 2: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.
Figure 1: Typical Output Characteristics at 25°C

![Graph showing typical output characteristics at 25°C.](image)

- $I_D$ – Drain Current (A)
- $V_D$ – Drain-to-Source Voltage (V)

Figure 2: Typical Transfer Characteristics

![Graph showing typical transfer characteristics.](image)

- $I_D$ – Drain Current (A)
- $V_G$ – Gate-to-Source Voltage (V)

Figure 3: Typical $R_{DS(on)}$ vs. $V_G$ for Various Drain Currents

![Graph showing $R_{DS(on)}$ vs. $V_G$ for various drain currents.](image)

- $R_{DS(on)}$ – Drain-to-Source Resistance (mΩ)
- $V_G$ – Gate-to-Source Voltage (V)

Figure 4: Typical $R_{DS(on)}$ vs. $V_G$ for Various Temperatures

![Graph showing $R_{DS(on)}$ vs. $V_G$ for various temperatures.](image)

- $R_{DS(on)}$ – Drain-to-Source Resistance (mΩ)
- $V_G$ – Gate-to-Source Voltage (V)

Figure 5a: Typical Capacitance (Linear Scale)

![Graph showing typical capacitance (linear scale).](image)

- $C$ – Capacitance (pF)
- $V_D$ – Drain-to-Source Voltage (V)

Figure 5b: Typical Capacitance (Log Scale)

![Graph showing typical capacitance (log scale).](image)

- $C$ – Capacitance (pF)
- $V_D$ – Drain-to-Source Voltage (V)
Figure 12: Transient Thermal Response Curves

**Junction-to-Board**

- **Duty Factors:**
  - 0.5
  - 0.2
  - 0.1
  - 0.05
  - 0.02
  - 0.01

- **Single Pulse**

\[ Z_{\theta JB} \text{, Normalized Thermal Impedance} \]

\[ t_p - \text{Rectangular Pulse Duration (s)} \]

\[ \text{Notes:} \]

\[ \text{Duty Factor} = \frac{t_p}{T} \]

\[ \text{Peak } T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B \]

**Junction-to-Case**

- **Duty Factors:**
  - 0.5
  - 0.2
  - 0.1
  - 0.05
  - 0.02
  - 0.01

- **Single Pulse**

\[ Z_{\theta JC} \text{, Normalized Thermal Impedance} \]

\[ t_p - \text{Rectangular Pulse Duration (s)} \]

\[ \text{Notes:} \]

\[ \text{Duty Factor} = \frac{t_p}{T} \]

\[ \text{Peak } T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C \]
### TAPE AND REEL
(units in mm)

<table>
<thead>
<tr>
<th>Type</th>
<th>A</th>
<th>N</th>
<th>C</th>
<th>D</th>
<th>w1</th>
<th>w2</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>8MM</td>
<td>Ø330±2</td>
<td>Ø100±2</td>
<td>Ø13.1±0.2</td>
<td>5.6±0.5</td>
<td>8.4±1.5</td>
<td>14.4</td>
<td>2.1±0.5</td>
</tr>
<tr>
<td>12MM</td>
<td>Ø330±2</td>
<td>Ø100±2</td>
<td>Ø13.1±0.2</td>
<td>5.6±0.5</td>
<td>12.4±1.5</td>
<td>18.4</td>
<td>2.1±0.5</td>
</tr>
<tr>
<td>16MM</td>
<td>Ø330±2</td>
<td>Ø100±2</td>
<td>Ø13.1±0.2</td>
<td>5.6±0.5</td>
<td>16.4±1.5</td>
<td>22.4</td>
<td>2.1±0.5</td>
</tr>
<tr>
<td>24MM</td>
<td>Ø330±2</td>
<td>Ø100±2</td>
<td>Ø13.1±0.2</td>
<td>5.6±0.5</td>
<td>24.4±1.5</td>
<td>30.4</td>
<td>2.1±0.5</td>
</tr>
</tbody>
</table>
Notes:
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metatization.
**PIN** | **Description**
--- | ---
1 | Gate
2 | Source
3 | Drain
4 | Source
5 | Drain
6 | Source
7 | Drain

**TRANSPARENT VIEW**

**RECOMMENDED LAND PATTERN**

*Legend:*
- Part outline
- Mask Opening

Radius = 0.05

Land pattern is solder mask defined

**RECOMMENDED STENCIL DRAWING**

*Legend:*
- Part outline
- Stencil opening

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.
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Information subject to change without notice.
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**RECOMMENDED COPPER DRAWING**
(units in mm)

![Copper Drawing](image)

**Legend:**
- **Part outline**
- **Lead frame**
- **Paste**
- **Mask**
- **Copper**

**Radius = 0.05**

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**3D COMPOSITE**

![3D Composite](image)

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**Additional resources available:**
  (for preliminary device Altium footprints, contact EPC)