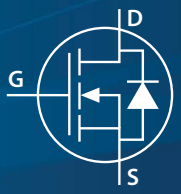
# EPC7003 – Enhancement Mode Power Transistor

$V_{DS}$, 100 V
$R_{DS(on)}$, 30 mΩ max
$I_D$, 42 A
95% Pb / 5% Sn Solder

Preliminary




EFFICIENT POWER CONVERSION

Halogen-Free

Rad Hard eGaN® transistors have been specifically designed for critical applications in the high reliability or commercial satellite space environments. GaN transistors offer superior reliability performance in a space environment because there are no minority carriers for a single event, and as a wide band semiconductor there is less displacement for protons and neutrons, and additionally, there is no oxide to breakdown. These devices have exceptionally high electron mobility and a low-temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for a very low gate charge ($Q_G$) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies, and more compact designs.

| Maximum Ratings | | | |
|---|---|---|---|
| PARAMETER | | VALUE | UNIT |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 100 | V |
| | Drain-to-Source Voltage (up to 10,000 5ms pulses at 150˚C) | 120 | |
| $I_D$ | Continuous | 10 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 42 | |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | -55 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -55 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Case TOP) | 2.8 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board (Case BOTTOM) | 5.6 | |
| $R_{\theta JA\_JEDEC}$ | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB) | 130 | |
| $R_{\theta JA\_EVB}$ | Thermal Resistance, Junction-to-Ambient (EPC9006C EVB) | 88 | |

**EPC7003** eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 1.7 x 1.1 mm

### Applications

- Space Applications: DC-DC power, motor drives, lidar, ion thrusters
- Commercial satellite EPS & avionics
- Deep space probes
- High frequency rad hard DC-DC conversion
- Rad hard motor drives

### Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$, $Q_G$, $Q_{GD}$, $Q_{OSS}$, and 0 $Q_{RR}$
- Ultra small footprint
- Light weight
- Total dose
  - Rated > 1 Mrad
- Single event
  - SEE immunity for LET of 85 MeV/(mg/cm$^2$) with $V_{DS}$ up to 100% of rated breakdown
- Neutron
  - Maintains pre-rad specification for up to 3 x 10$^{15}$ neutrons/cm$^2$
- Superior radiation and electrical performance vs. rad hard MOSFETs: smaller, lighter, and greater radiation hardness

| Static Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 100 µA | 100 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | 0.5 | 100 | µA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.001 | 0.6 | mA |
| | Gate-to-Source Forward Leakage# | $V_{GS}$ = 5 V, $T_J$ = 125°C | | 0.1 | 1.3 | |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 0.5 | 100 | µA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.4 mA | 0.8 | 1.4 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 6 A | | 18 | 30 | mΩ |
| $V_{SD}$ | Source-to-Drain Forward Voltage# | $I_S$ = 0.5 A, $V_{GS}$ = 0 V | | 1.7 | | V |

# Defined by design. Not subject to production test.

| Dynamic Characteristics# ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 230 | 313 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 0.6 | | |
| $C_{OSS}$ | Output Capacitance | | | 119 | 143 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 1) | $V_{DS}$ = 0 to 50 V, $V_{GS}$ = 0 V | | 144 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 2) | | | 188 | | |
| $R_G$ | Gate Resistance | | | 1.3 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 6 A | | 1.8 | 2.5 | nC |
| $Q_{GS}$ | Gate-to-Source Charge | $V_{DS}$ = 50 V, $I_D$ = 6 A | | 0.6 | | |
| $Q_{GD}$ | Gate-to-Drain Charge | | | 0.3 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 0.4 | | |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 9.4 | 11 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

All measurements were done with substrate connected to source.
# Defined by design. Not subject to production test.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.

**Figure 1: Typical Output Characteristics at 25 °C**

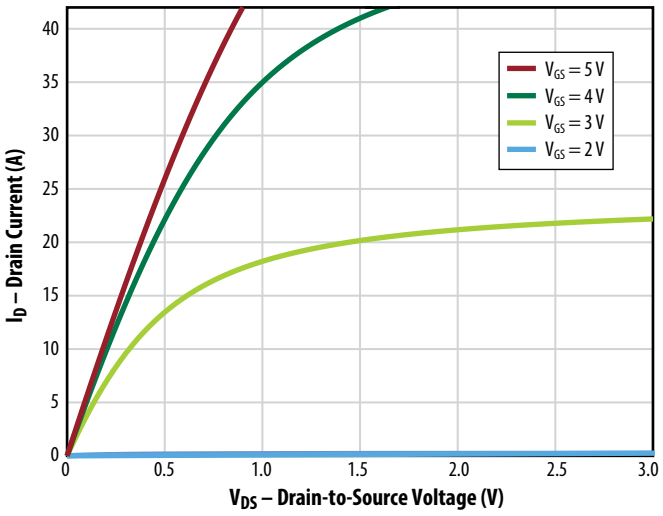



**Figure 2: Typical Transfer Characteristics**

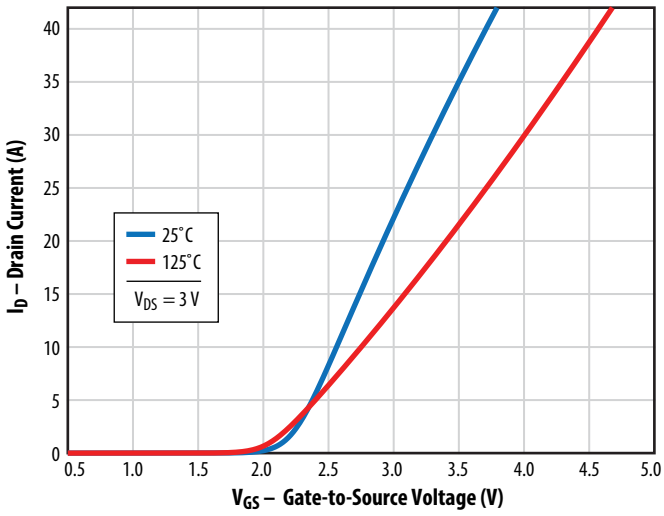



**Figure 3: $R_{DS(on)}$ vs. $V_{GS}$ for Various Drain Currents**

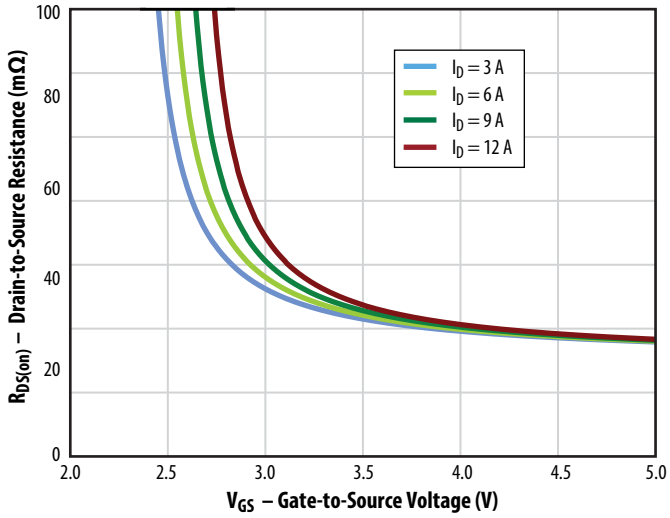



**Figure 4: $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures**

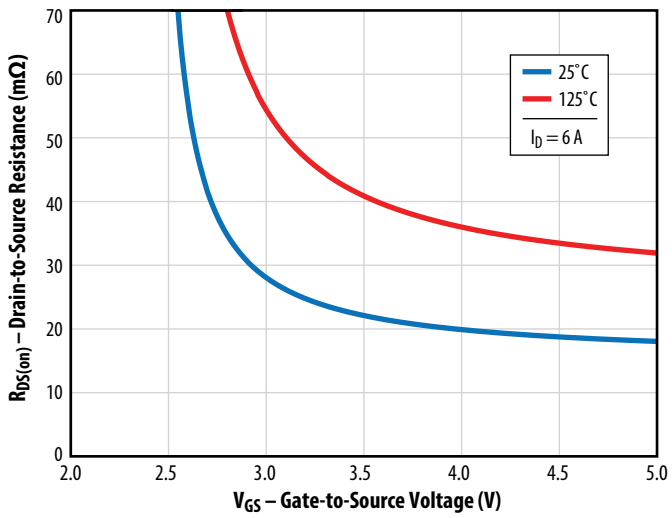


**Figure 5a: Typical Capacitance (Linear Scale)**

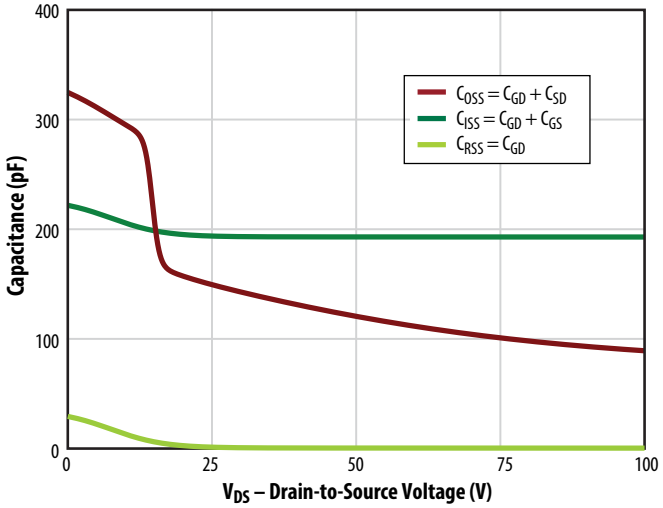



**Figure 5b: Typical Capacitance (Log Scale)**

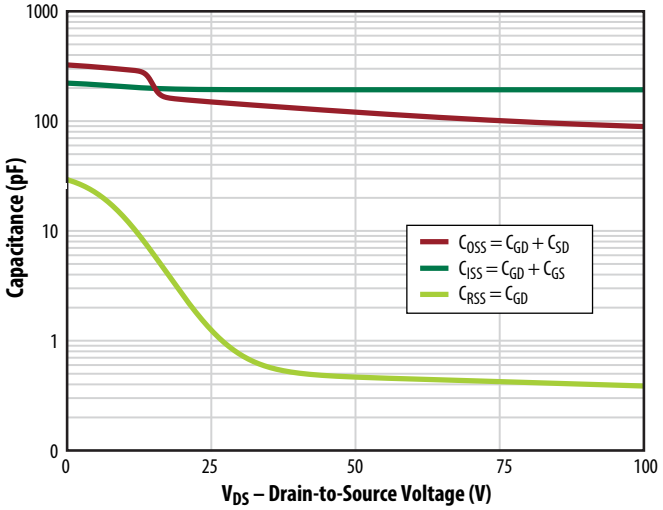



**Figure 6: Typical Output Charge and $C_{OSS}$ Stored Energy**

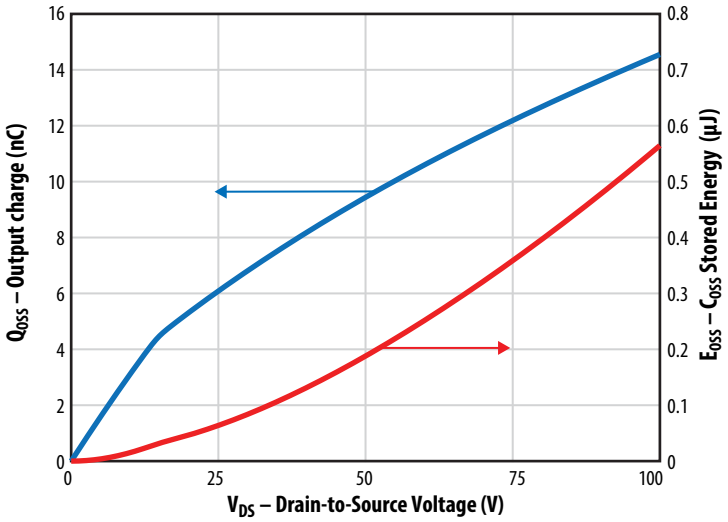



**Figure 7: Typical Gate Charge**

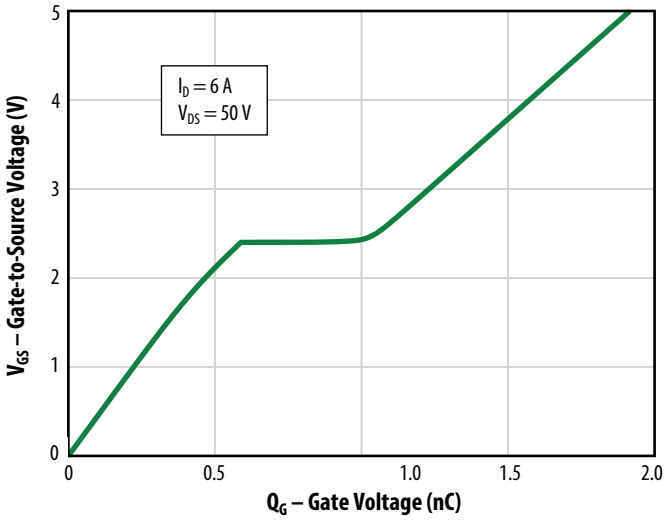



**Figure 8: Reverse Drain-Source Characteristics**

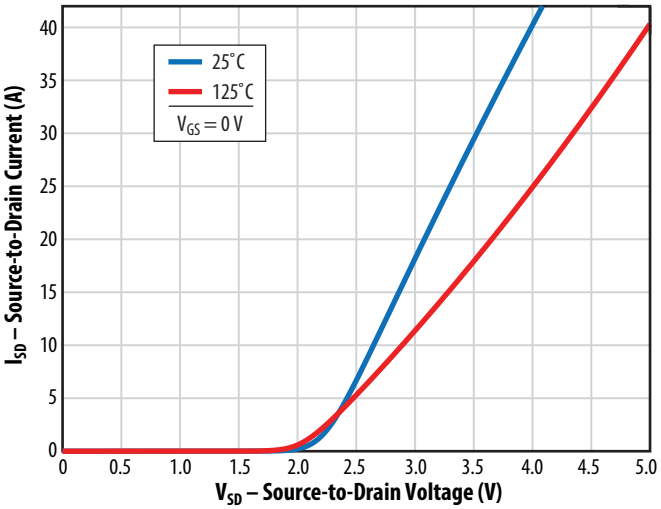
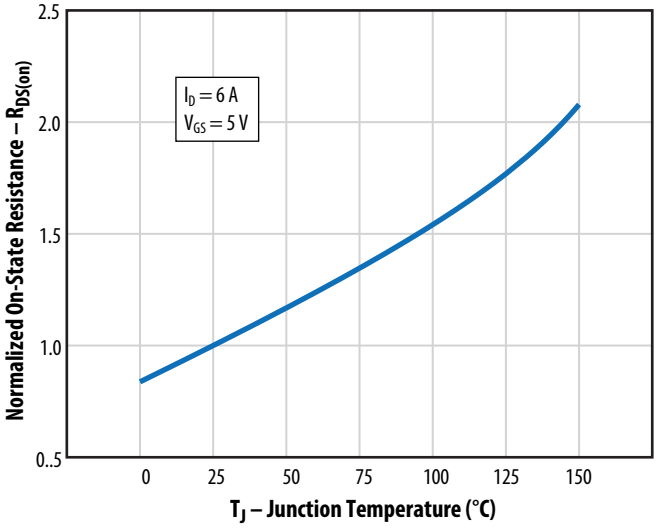



**Figure 9: Normalized On-State Resistance vs. Temperature**




**Note:** Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

**Figure 10: Normalized Threshold Voltage vs. Temperature**

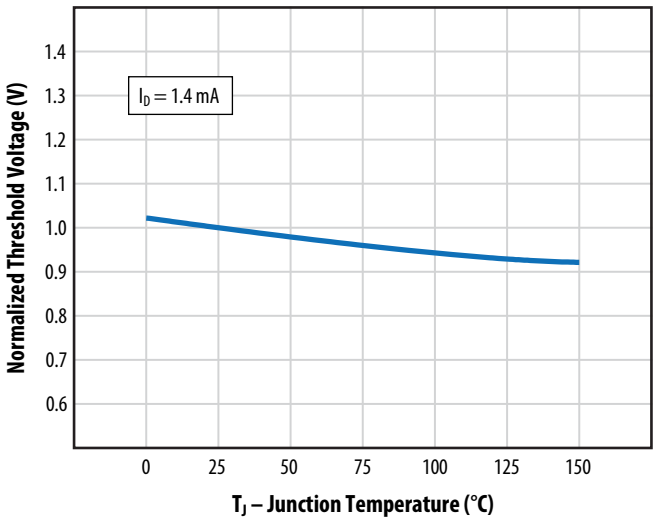
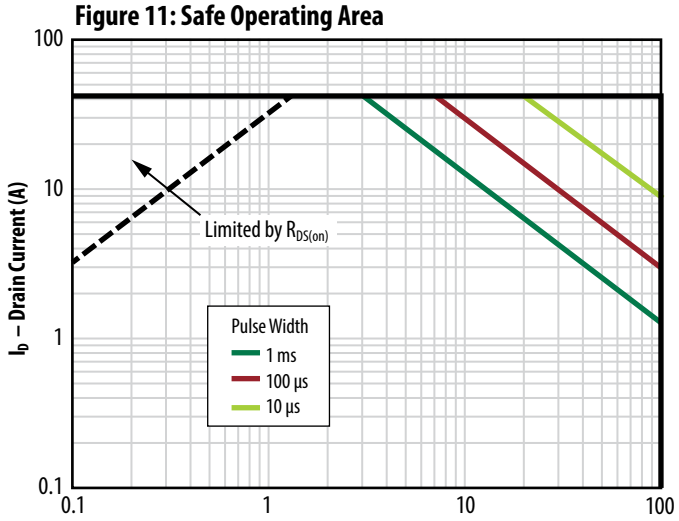
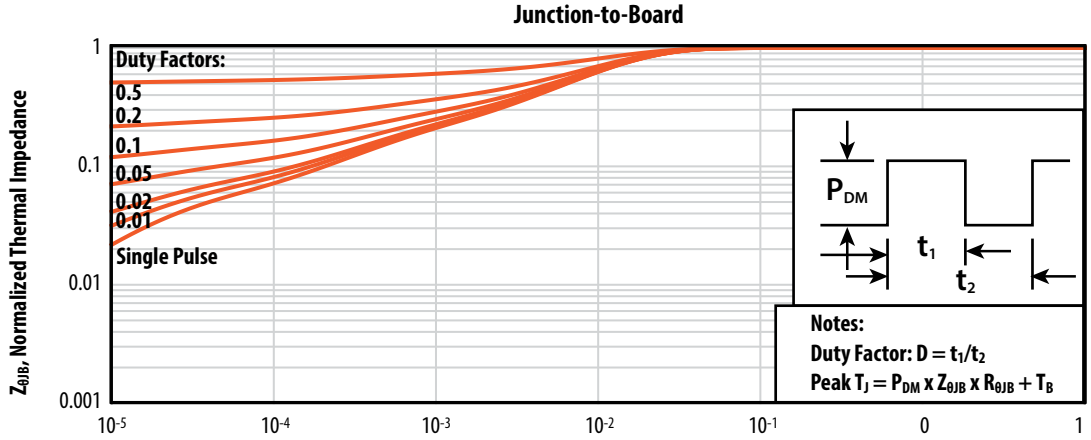


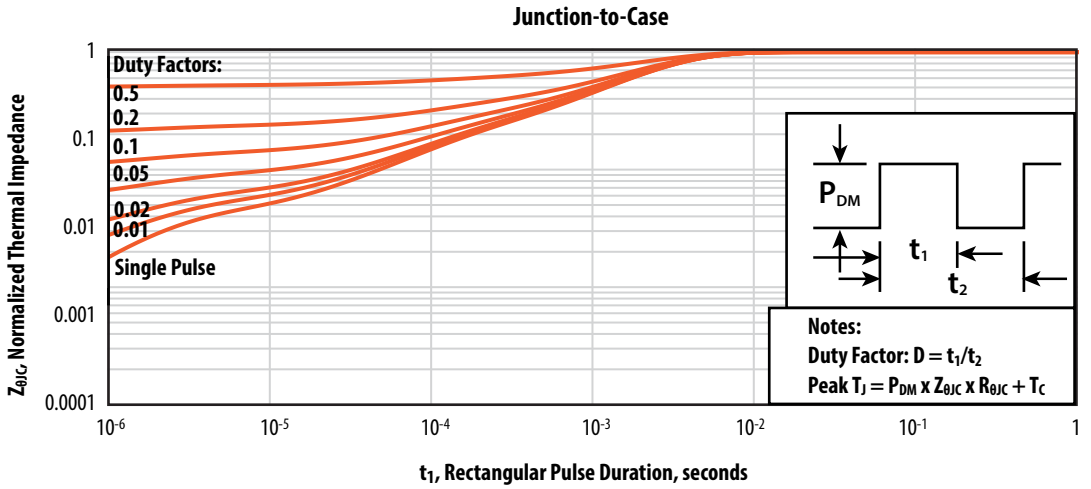

**Figure 11: Safe Operating Area**




$T_J$ = Max Rated, $T_C$ = +25°C, Single Pulse

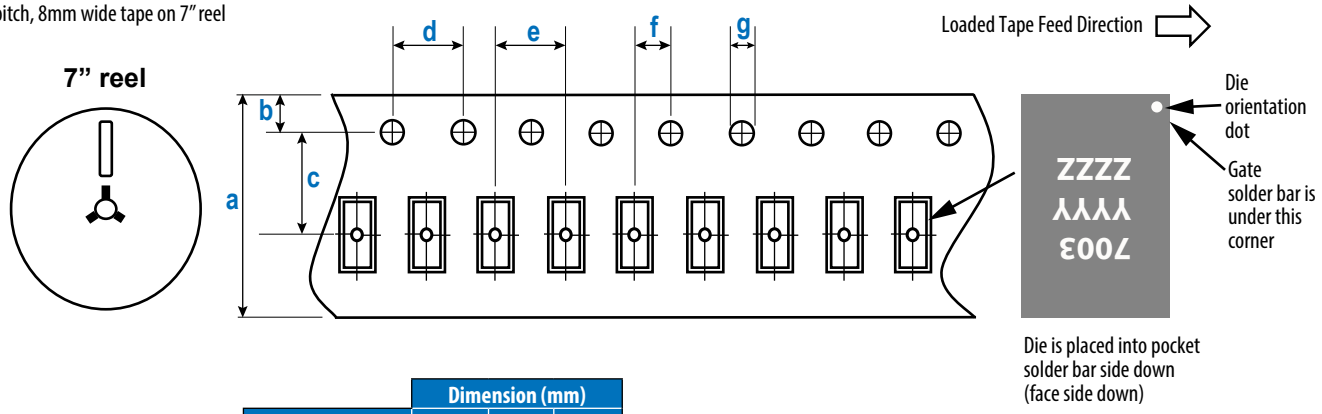
**Figure 12: Transient Thermal Response Curves**



## TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

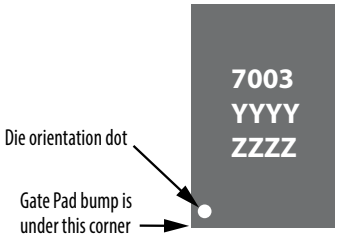



| | Dimension (mm) | | |
|---|---|---|---|
| EPC7003 (Note 1) | Target | MIN | MAX |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

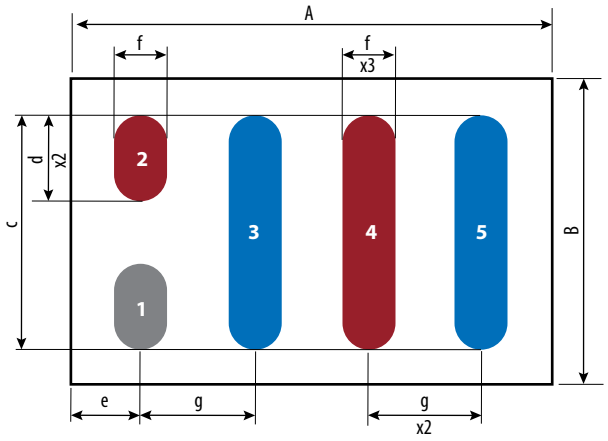
## DIE MARKINGS



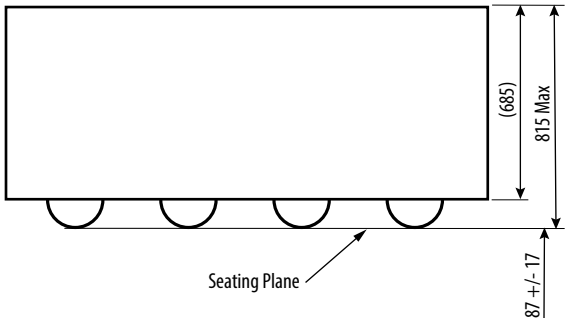

| Part Number | Laser Markings | | |
|---|---|---|---|
| | Part Number Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC7003 | 7003 | YYYY | ZZZZ |

## DIE OUTLINE

Solder Bar View




Side View



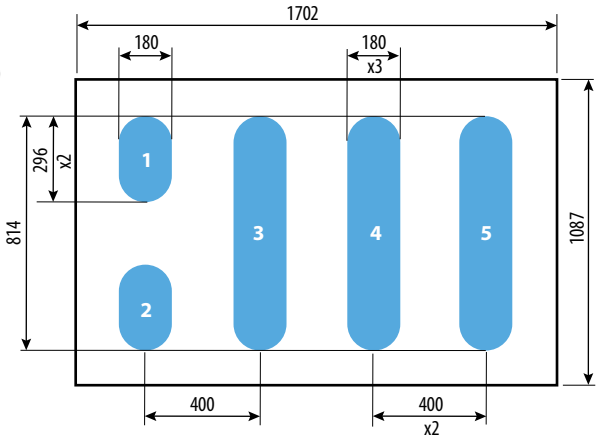

| DIM | MICROMETERS | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 1672 | 1702 | 1732 |
| B | 1057 | 1087 | 1117 |
| c | 829 | 834 | 839 |
| d | 311 | 316 | 321 |
| e | 235 | 250 | 265 |
| f | 195 | 200 | 205 |
| g | 400 | 400 | 400 |

**Pad no. 1 is Gate;**
**Pads no. 2 and 4 are Source;**
**Pads no. 3 and 5 are Drain**

Substrate (top side) connected to Source

## RECOMMENDED LAND PATTERN

*(measurements in µm)*




The land pattern is solder mask defined

Pad no. 1 is Gate;
Pads no. 2 and 4 are Source;
Pads no. 3 and 5 are Drain