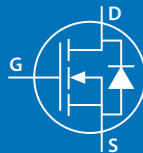


EPC7014 – Rad Hard Power Transistor

 V_{DS} , 60 V $R_{DS(on)}$, 340 mΩ I_D , 4 A pulse

95% Pb / 5% Sn solder

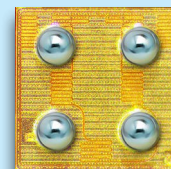


Revised October 3, 2023

Rad Hard eGaN® transistors have been specifically designed for critical applications in the high reliability or commercial satellite space environments. GaN transistors offer superior reliability performance in a space environment because there are no minority carriers for single event, and as a wide band semiconductor there is less displacement for protons and neutrons, and additionally there is no oxide to breakdown.

These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact designs.

Questions:
Ask a GaN
Expert



Die size: 0.9 x 0.9 mm

EPC7014 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

- Commercial satellite EPS & avionics
- Deep space probes
- High frequency rad-hard DC-DC conversion
- Rad-hard motor drives

Features

- Ultra high efficiency
- Ultra low Q_G
- Ultra small footprint
- Light weight
- Total dose
 - Rated > 1 Mrad
- Single event
 - SEE immunity for LET of 85 MeV/(mg/cm²) with V_{DS} up to 100% of rated breakdown
- Neutron
 - Maintains pre-rad specification for up to 3×10^{15} Neutrons/cm²

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC7014>

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	60	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	2.4	A
	Pulsed (25°C, $T_{PULSE} = 300 \mu\text{s}$)	4	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	7.1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	25	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	104	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}, I_D = 0.1 \text{ mA}$	60			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}, V_{DS} = 60 \text{ V}$		0.0001	0.1	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.001	0.5	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5 \text{ V}, T_J = 125^\circ\text{C}$		0.05	1	
	Gate-to-Source Reverse Leakage	$V_{GS} = -3 \text{ V}$		0.05	1.1	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.14 \text{ mA}$	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}, I_D = 0.50 \text{ A}$		240	340	mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$V_{GS} = 0 \text{ V}, I_S = 0.1 \text{ A}$		1.9		V

[#] Defined by design. Not subject to production test.

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		16	22	pF
C_{RSS}	Reverse Transfer Capacitance			0.1		
C_{OSS}	Output Capacitance			17	26	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }30\text{ V}, V_{GS} = 0\text{ V}$		21		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			26		
R_G	Gate Resistance			12.6		Ω
Q_G	Total Gate Charge	$V_{DS} = 30\text{ V}, V_{GS} = 5\text{ V}, I_D = 0.5\text{ A}$		142	184	pC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 30\text{ V}, I_D = 0.5\text{ A}$		43		
Q_{GD}	Gate-to-Drain Charge			25		
$Q_{G(TH)}$	Gate Charge at Threshold			35		
Q_{OSS}	Output Charge	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		764	1146	
Q_{RR}	Source-Drain Recovery Charge			0		

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

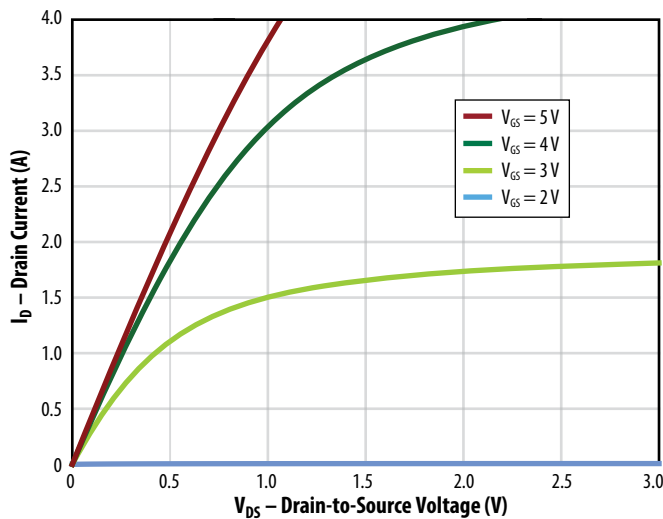
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Typical Transfer Characteristics

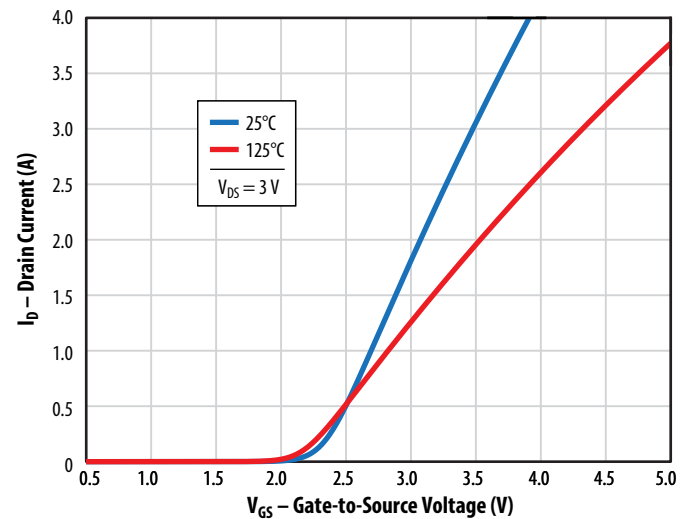
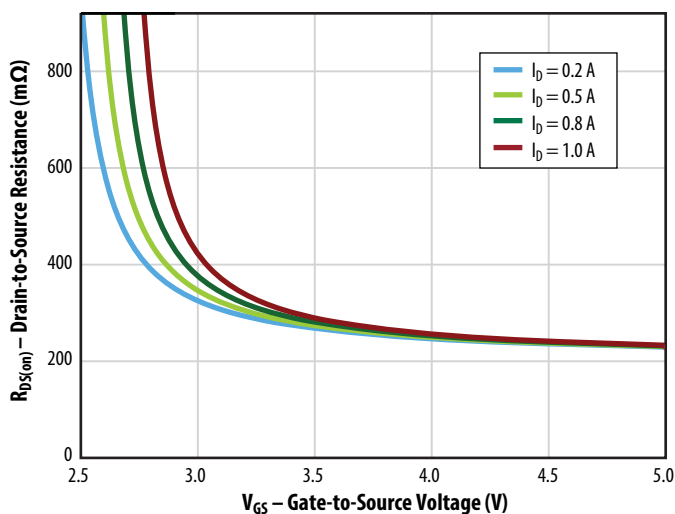
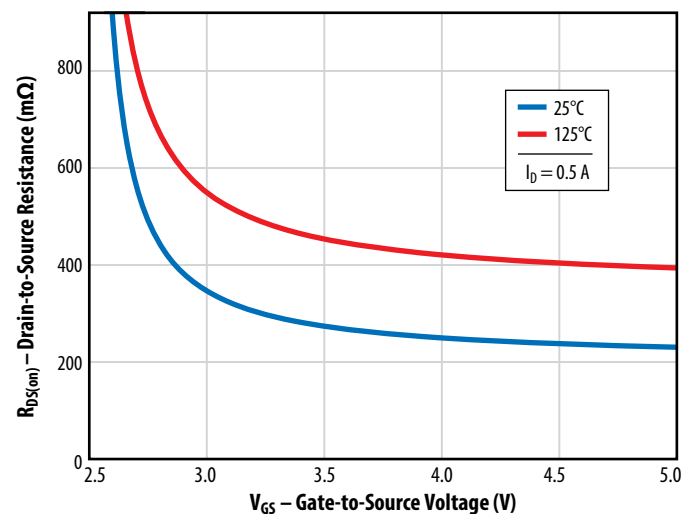
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

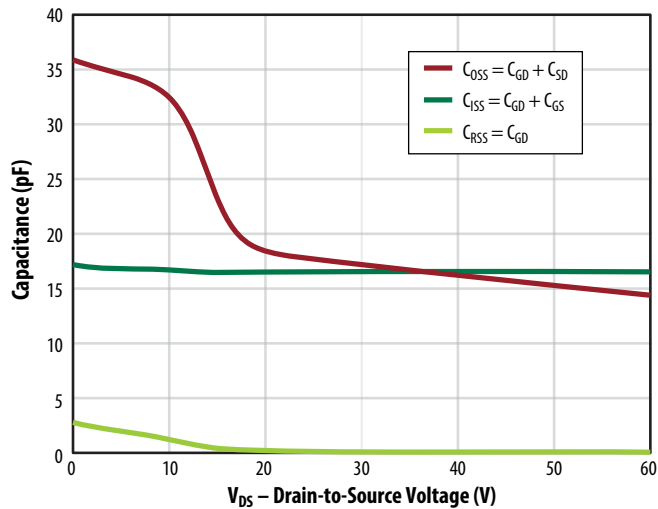


Figure 5b: Typical Capacitance (Log Scale)

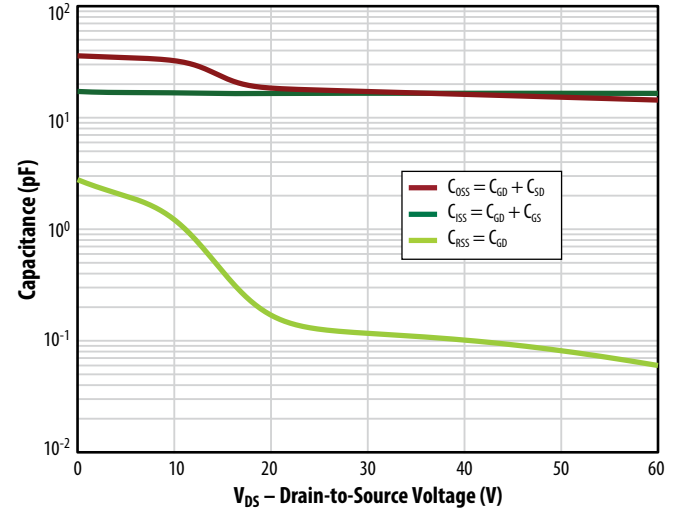
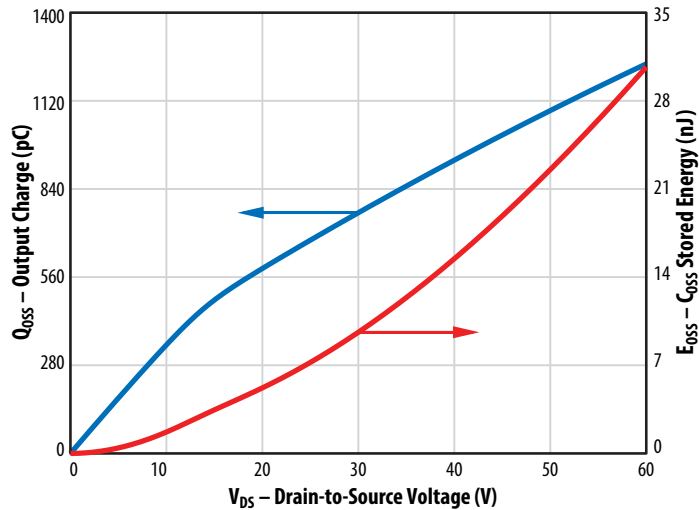
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

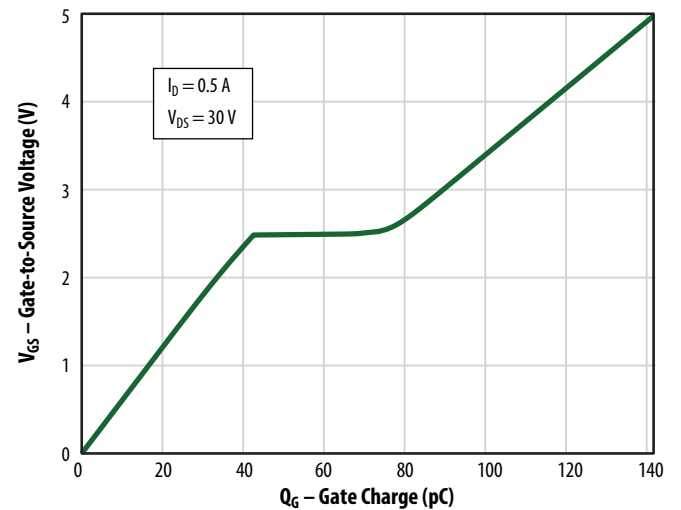


Figure 8: Typical Reverse Drain-Source Characteristics

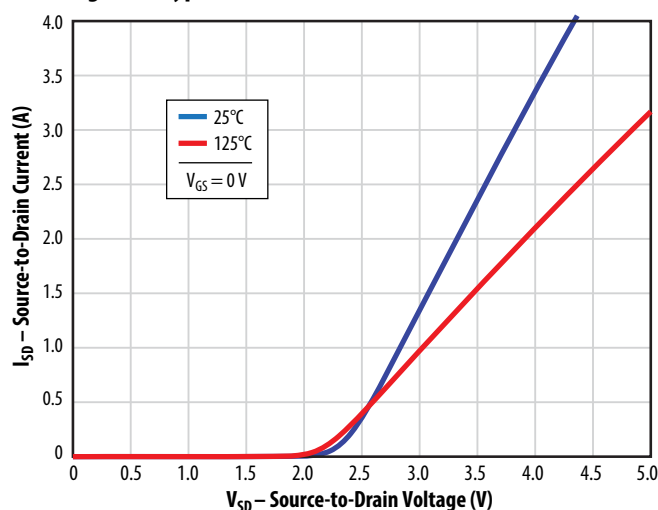
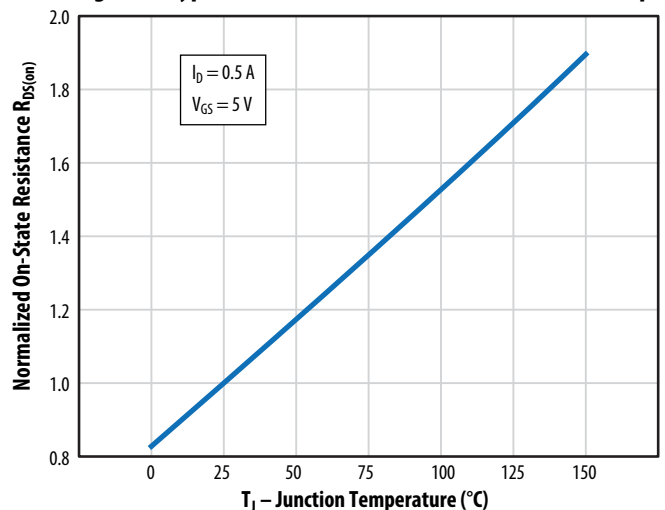


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

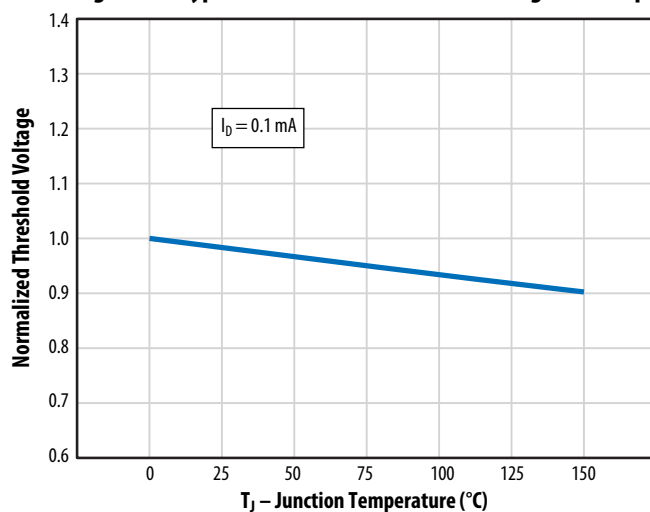


Figure 11: Safe Operating Area

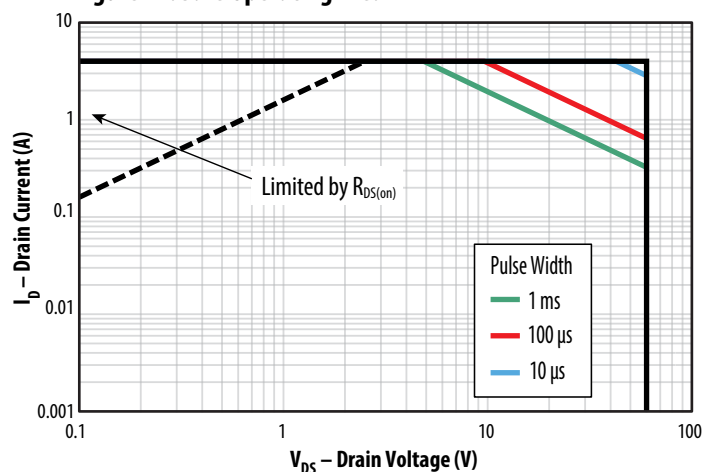
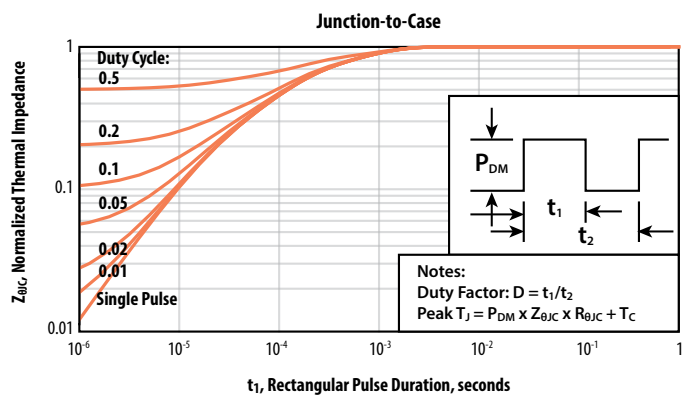
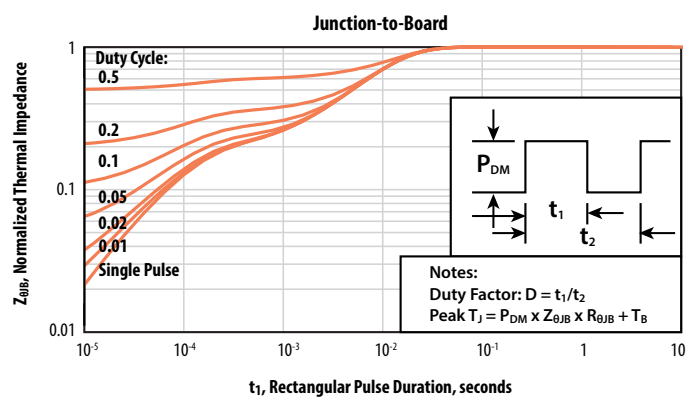
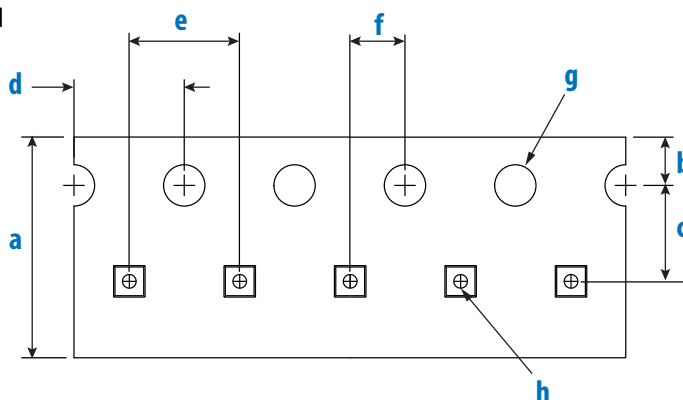
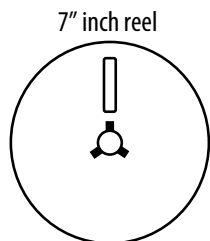


Figure 12: Typical Transient Thermal Response Curves

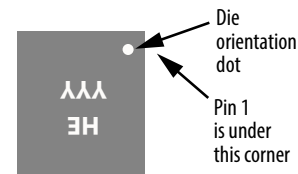


TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



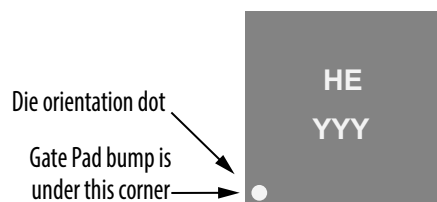
Die is placed into pocket solder bump side down (face side down)

EPC7014 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



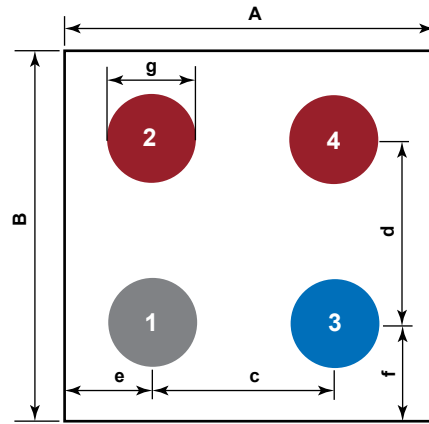
Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC7014	HE	YYY

ORDERING INFORMATION

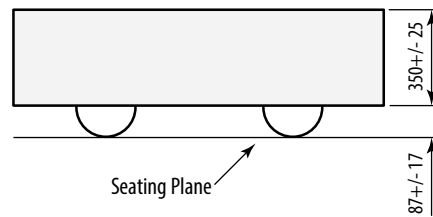
EPC7014	EPC7014 die without Radiation Data and without Single Event (SEE) certification report
EPC7014_DT	EPC7014 die with Radiation Data and Single Event (SEE) Certification report

DIE OUTLINE

Solder Bump View
(measurements in μm)



Side View



DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

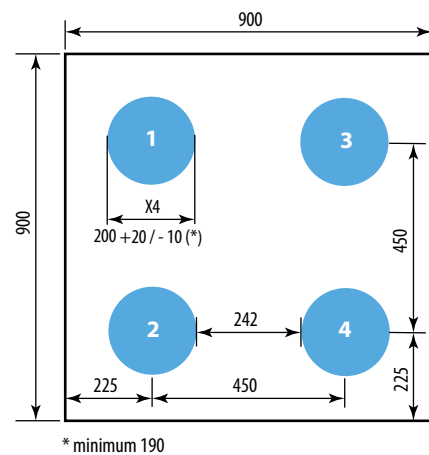
Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

**RECOMMENDED
LAND PATTERN**

(measurements in μm)



The land pattern is solder mask defined.

Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

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