#### eGaN<sup>®</sup> FET DATASHEET

# EPC2152 – ePower™ Stage IC

V<sub>IN</sub> , 80 V I<sub>Load</sub> , 15 A



RoHS M

# Rev. 2, November 26, 2024

Halogen-Free

The ePower<sup>™</sup> Stage IC Product Family integrates input logic interface, high-side level shifting, synchronous bootstrap charging and gate drivers along with eGaN output FETs into one monolithic integrated-circuit using EPC's proprietary GaN IC technology. The result is a Power Stage IC that translates logic level control signals into a high voltage and high current power stage that is simpler to design, smaller in size and easier to manufacture while being more efficient to operate.

Questions: Ask a GaN Expert

Key Parameters		
PARAMETER	VALUE	UNIT
Power Stage Load Current (1 MHz) <sup>(1)</sup>	15	A
Operating PWM Frequency (Maximum) <sup>(2)</sup>	3	MHz
Absolute Maximum Input Voltage	80	
Operating Input Voltage Range	60	V
Nominal Bias Supply Voltage	12	

Output Current and PWM Frequency Ratings are specified at ambient temperature of 25°C. See Application Information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

Device Information					
PART NUMBER	Rated R <sub>DS(on)</sub> for HS and LS FETs at 25 °C	CSP Package Size (mm)			
EPC2152	$10 \text{ m}\Omega + 10 \text{ m}\Omega$	2.59 x 3.85			

(1) Achieved when using proper heatsink. Output current and PWM frequency ratings are function of operating conditions, see "Load current rating" in the application section for more information.

(2) Operating PWM switching frequency range is a function of power dissipation, maximum allowed junction temperature and minimum duty cycle.

#### **Figure 1: Performance Curves**



Buck Converter,  $V_{IN} = 48$  V,  $V_{OUT} = 12$  V, Deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, with heatsink attached, airflow = 400 LFM, TA = 25°C, using **EPC90120 evaluation board**.



Package size: 2.59 x 3.85 mm EPC2152 ePower<sup>™</sup> Stage IC

#### Applications

- Buck, boost, buck-boost converters
- Half-bridge, full bridge LLC converters
- Motor drive inverter
- Class D audio amplifier

#### Features

- Integrated high side eGaN<sup>®</sup> FET with internal gate driver and level shifter
- 3.3 V or 5 V CMOS input logic levels
- Independent high side and low side control inputs
- Logic lockout commands both FETs off when inputs are both high at same time
- Internally regulated gate drive voltage
- Tuned to 1.5 ns switching time
- Controlled over-voltage transient at switching node
- Robust level shifter operation for hard and soft switching conditions
- False trigger immunity from fast switching transients
- Synchronous charging for high-side bootstrap supply
- Undervoltage lockout for high side and low side power supplies

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



https://bit.ly/EPC2152

# Figure 2: EPC2152 Chip Scale Package

(transparent top view)



## **EPC2152 Pinout Description**

Pin	Pin Name	Pin Type	Description
1	V <sub>BOOT</sub>	S	Floating bootstrap power supply referenced to SW. Connect an external bootstrap capacitor, $C_{BOOT}$ , between $V_{BOOT}$ and SW.
2	V <sub>DD</sub>	S	Internal power supply referenced to GND, connect an external bypass capacitor from $V_{\text{DD}}$ to GND.
3	HS <sub>IN</sub>	L	High-side PWM logic input referenced to GND. Internal pull-down resistor is connected between HS <sub>IN</sub> and GND.
4	LS <sub>IN</sub>	L	Low-side PWM logic input referenced to GND. Internal pull-down resistor is connected between LS <sub>IN</sub> and GND.
5, 9	V <sub>IN</sub>	Р	Power bus input. Connected to drain terminal of internal high side eGaN FET. Connect power loop capacitors from V <sub>IN</sub> to GND
6, 7, 10 ,11	SW	Р	Output switching node. Connected to output of half-bridge power stage. SW pin connects the source terminal of high-side eGaN FET to the drain terminal of the low-side eGaN FET.
8, 12	GND	р	Power ground. Connected to low side eGaN FET source terminal. The operating power supply, $V_{DD}$ , is also referenced to GND. Connect bypass capacitors between operating bias supply, $V_{DD}$ , to GND, and power loop bypass capacitor from $V_{IN}$ to GND.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs

# Figure 3: Functional Block Diagram



# **Absolute Maximum Ratings**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Absolute Maximum Ratings						
SYMBOL	PARAMETER	MIN	MAX	UNITS		
V <sub>IN</sub>	Input voltage		80			
SW (continuous)	Output switching node (SW to GND), continuous		80			
V <sub>DD</sub>	Internal low side supply voltage		14	V		
V <sub>BOOT</sub> – SW	Internal high side supply voltage (V <sub>BOOT</sub> to SW)		14			
HS <sub>IN</sub> , LS <sub>IN</sub>	PWM logic inputs	-1	5.5			
Tj	Junction temperature	-40	125	ŝ		
T <sub>STG</sub>	Storage temperature	-55	150			

#### **ESD Ratings**

ESD Ratings					
SYMBOL	PARAMETER	MIN	МАХ	UNITS	
НВМ	Human-body model (JEDEC JS-001)	+/-500		N	
CDM	Charged-device model (JEDEC JESD22-C101)	+/-1000		v	

#### **Thermal Characteristics**

R<sub>0JA\_JEDEC</sub> is defined according to JESD51-2 standard. Based on this standard, the device is placed on 4-layer PCB with 2 oz copper for outer layers and 1 oz copper for inner layers. This assembly is placed in a 1 cubic foot enclosure with no forced air cooling, only natural convection.

R<sub>0JA\_EVB</sub> is based on EPC90120, a real evaluation board with no forced air cooling. This thermal resistance is more indicative of an actual application environment.

 $R_{\theta JA}$  is determined with the device mounted on 1 in<sup>2</sup> of copper pad, single layer 2 oz copper on FR4 board.

Thermal Characteristics					
SYMBOL	PARAMETER	ТҮР	UNITS		
R <sub>θJC_Top</sub>	Thermal Resistance, Junction-to-Case (Top surface of exposed die substrate)	0.47			
$R_{\theta JB\_Bottom}$	Thermal Resistance, Junction-to-Board (At solder joints of $V_{IN}$ and SW PCB pads)	3			
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	43	°C/W		
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90142 EVB)	25			
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	46			

#### **Recommended Operating Conditions**

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Recommended Operating Conditions						
SYMBOL	PARAMETER	MIN	ТҮР	MAX	UNITS	
V <sub>IN</sub>	Input voltage	0		60		
SW (Q3 Mode)	Output switch node, 3 <sup>rd</sup> quadrant mode	-2.5		V <sub>IN</sub> + 2.5		
SW (pulse2ns)	Output switch node, transient PW < 2 ns	-10		V <sub>IN</sub> +10		
V <sub>DD</sub>	Internal low side supply voltage	11	12	13	V	
V <sub>BOOT</sub> – SW	Internal high side supply voltage (V <sub>BOOT</sub> to SW)	11	12	13		
HS <sub>IN</sub> , LS <sub>IN</sub>	PWM logic inputs	0		5		
T <sub>J, op</sub>	Operating Junction Temperature	-40		125	°C	

## **Electrical Characteristics**

Nominal  $V_{IN} = 48 \text{ V}$ ,  $V_{DD} = 12 \text{ V}$  and  $(V_{BOOT} - SW) = 12 \text{ V}$ . All typical ratings are specified at  $T_A = 25^{\circ}\text{C}$  unless otherwise indicated. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.<sup>(1)</sup>

SYMBORPRAMETERTEST CONDITIONSMINTYPMAXUNTSPower SUPOff state total queiscent currentHSp., /LSm. = 0.V./Un. = 12V, SM floating[]12]lobdubTotal operating current @1 MHzPWM = 1 MHz, S0% On-Time, includes bootstrap current[]237]lobdubTotal operating current @3 MHzPWM = 1 MHz, S0% On-Time, includes bootstrap current[][][][]][]]][][]][]	Electrical Characteristics						
Power Supply   U     lon_, uwit   Cold algoerating current @1 MHz   HS <sub>M</sub> /LS <sub>M</sub> to V/Loo 12V, SM floating   14   21   7     lon_, uwit   Total operating current @1 MHz   PWM = 1 MHz, 50% On-Time, includes bootstrap current   28   40     Bootstrap   State bootstrap supply current @1 MHz   PWM = 1 MHz, 50% On-Time, includes bootstrap current   28   40     Bootstrap   State bootstrap supply current @1 MHz   HS PWM = 1 00 kHz, 50% On-Time   12   17   mA     loo_t_state   Bootstrap supply current @1 MHz   HS PWM = 1 00 kHz, 50% On-Time   10   24   0     Vinc. towit   Bootstrap supply current @1 MHz   HS PWM = 1 00 kHz, 50% On-Time   16   20   24   0     Vinc. towit   U/O One sistance of Synch-boot FET   lync. towit   16   20   24   0     Vinc. towit   U/O One parating inyteresis   LS <sub>m</sub> = 5 V. Vino Ramps Up   6.25       Vinc. towit   U/O One parating inyteresis   LS <sub>m</sub> = 5 V. Vinor Ramps Up   6.25       Vinc. UNO Or Tip Level (Vinor Time Vinor Massing ML   HS <sub>m</sub> = 5 V. Vinor Ramp	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
bp.o.   Off state total quiescent current   H Styr LS <sub>M</sub> = 0 V, Vboo 12 V. SM floating   I   I   I   I     float.lower   Total operating current @1 MHz   PWM = 1 MHz, S0% On-Time, includes bootstrap current   25   37     Mon.SWW   Total operating current @3 MHz   PWM = 1 MHz, S0% On-Time, includes bootstrap current   9   12.5   400     Boor.SWW   Bootstrap supply current @3 MHz   HS PWM = 100 HZ, S0% On-Time   17   24   7     Mon.TAMU   Bootstrap supply current @3 MHz   HS PWM = 100 HZ, S0% On-Time   17   24   7     Mon.TAMU   Bootstrap supply current @3 MHz   HS PWM = 100 HZ, S0% On-Time   17   24   7     Mon.TAMU   Dotstrap supply current @3 MHz   HS PWM = 1 MHz, S0% On-Time   320   400   400     Vanc.TAMU   Dotstrap supply current @1 MHz   HS PWM = 1 MHz, S0% On-Time   320   400   400     Vanc.TAMU   Discover Signet-hobot FET   Ipw.Ecor = 20 mA   6.5   -   7   10   24   10   0.5   -   7   10   KD   7   7   10<	<b>Power Supply</b>						
	I <sub>DD_Q</sub>	Off state total quiescent current	$HS_{IN}$ /LS <sub>IN</sub> = 0 V, $V_{DD}$ = 12 V, SW floating		14	21	
bps_met   Total operating current @3 MHz   PWM = 1 MHz, 50% On-Time, includes bootstrap current   28   40     Bootstrap supplex   United operating current @3 MHz   PSWM = 100 kHz, 50% On-Time   9   12.5     Incor, a.W.   Of state bootstrap supply current @1 MHz   HS PWM = 100 kHz, 50% On-Time   12   17   24     Name, Cabop   Voltage across Synch-boot FET   Issue, goot = 20 mA   320   400   480   mV     Ngncy, SW, BOO   On resistance of Synch-boot FET   Issue, goot = 20 mA   320   400   480   mV     Vgncy, SW, BOO   On resistance of Synch-boot FET   Issue, goot = 20 mA   160   20   24   Q     Undervoltage across Synch-boot FET   Issue, goot = 20 mA   160   20   24   Q     Undervoltage across Synch-boot FET   Issue, goot = 20 mA   0.05   C   P     Vgn_D, mort   UVIC Or Trip Level (Vgoor SWI Rising   LSsue 5 V, Vgoor Ramps Down   0.05   C     Vacor swot   UVIC Vigo-Sall Bing Hysteresis   LSsue 5 V, Vgoor Ramps Down   0.05   C     Vgn, Min   High side on pr	I <sub>DD_1MHz</sub>	Total operating current @1 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		25	37	mA
Bootstrap supply current with HS, = 0V, (V <sub>BOOT</sub> - V <sub>SW</sub> ) = 5V   9   12.5   m     boor_nawa   Bootstrap supply current @ MHz   HS PWM = 100 kHz, 50% On-Time   17   24     boor_nawa   Bootstrap supply current @ MHz   HS PWM = 100 kHz, 50% On-Time   17   24     V <sub>SNC, ROP</sub> Voltage across Synch-boot FET   I <sub>SNC, BOOT</sub> = 20 mA   320   400   480   mV     Materiotage   Location   Strap supply current @ MHz   HS PWM = 100 kHz, 50% On-Time   16   20   440   480   mV     Materiotage   Location   Strap supply current @ MLZ   HS PWM = 100 kHz, 50% On-Time   5.5   17   24   10   12   17   24     Vance strap supply current @ MLZ   LS = 5 V, V <sub>DOD</sub> Ramps Down   0.5   1   10 <td>I<sub>DD_3MHz</sub></td> <td>Total operating current @3 MHz</td> <td>PWM = 1 MHz, 50% On-Time, includes bootstrap current</td> <td></td> <td>28</td> <td>40</td> <td></td>	I <sub>DD_3MHz</sub>	Total operating current @3 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		28	40	
$ \begin{array}{                                    $	Bootstrap Pov	wer Supply					
$ \begin{array}{                                    $	I <sub>BOOT_Q</sub>	Off state bootstrap supply current	$HS_{IN} = 0 V$ , $(V_{BOOT} - V_{SW}) = 5 V$		9	12.5	
	I <sub>BOOT_1MHz</sub>	Bootstrap supply current @1 MHz	HS PWM = 100 kHz, 50% On-Time		12	17	mA
Vsmc_book   Voltage across Synch-boot FET   lsmc_boot   20mA   320   400   480   mV     Row_served   On resistance of Synch-boot FET   lsmc_boot   20mA   16   20   24   Ω     Undervolge   UVLO Trip Level Vop Rising   LSm_5 5 V, Vop Ramps Up   6.5	I <sub>BOOT_3MHz</sub>	Bootstrap supply current @3 MHz	HS PWM = 1 MHz, 50% On-Time		17	24	
	V <sub>SYNC_DROP</sub>	Voltage across Synch-boot FET	I <sub>SYNC_BOOT</sub> = 20 mA	320	400	480	mV
Undervoltage LockoutVb_D_UNLobUVLO Trip Level V <sub>000</sub> RisingLSm 5 V, V <sub>000</sub> Ramps Up6.5	R <sub>ON_SYNC_BOOT</sub>	On resistance of Synch-boot FET	I <sub>SYNC_BOOT</sub> = 20 mA	16	20	24	Ω
VDD_UNLO+ VDD_UVLOUVLO Trip Level VDD RisingLSM = 5 V, VDD Ramps Down6.5V 0.5VBOD_UND- VBODT_SUD-UVLO VD Trip Level (VBDOT - SW) RisingHSM = 5 V, VDD Ramps Down0.5V 0.5VBODT_UND- VBODT_SUD-UVLO VD Trip Level (VBDOT - SW) RisingHSM = 5 V, VDD Ramps Down0.5VUVLO VD (VBOT - SW) Falling HysteresisHSM = 5 V, VDD Ramps Down0.5VUVLO VBD (VBDOT - SW) Falling HysteresisUVLO VBDOT RAMPS Down0.5VVMHigh-level Logic ThresholdHSM, LSM Rising2.4VVMLow-level Logic ThresholdHSM, LSM Falling0.5VVMSTLogic Threshold HysteresisVH, Rising - VL Falling0.5VVMSTLogic Threshold HysteresisVH, Rising - VL Falling0.5VVMSTLogic Threshold HysteresisVH, Rising - VL Falling0.5VT_delay, S_ORHigh side on propagation delaySW = 0V and LS FET turn-on30VL_delay, S_ORHigh side off propagation delaySW = 0V and LS FET turn-onff30VL_delay, S_ORHigh side off propagation delaySW = 0V and LS FET turn-onff30VL_delay, S_ORHigh side off propagation delaySW = 0V and LS FET turn-onff30VL_delay, S_ORLow side off propagation delaySW = 0V and LS FET turn-off30VL_delay, S_ORHigh side FET RDSONLS LUT-Off to HS turn-on rHS turn-off to LS turn-on0VMushonDelay matching HSOFF to LSONHS	Undervoltage	2 Lockout					
$ \begin{array}{ c c c } \hline V_{DO,MOA} & UVLO V_{OD} Falling Hysteresis & LS_{NI} = 5 V, V_{OD} Ramps Down & 0.5 & 0.5 \\ \hline V_{OOD,MOA} & UVLO (V_{BOOT} - SW) Rising & HS_{NI} = 5 V, V_{BOOT} Ramps Down & 0.5 & 0.5 \\ \hline V_{BOOT,MVC} & UVLO (V_{BOOT} - SW) Falling Hysteresis & HS_{NI} = 5 V, V_{BOOT} Ramps Down & 0.5 & 0.5 \\ \hline V_{BOOT,MVC} & UVLO (V_{BOOT} - SW) Falling Hysteresis & V_{NI}, Rising & 2.4 & 0.5 & 0.5 \\ \hline V_{II} & Low-level Logic Threshold & HS_{NI}, LS_{NI} Falling - V_{II} Falling & 0.5 & 0.5 & 0.5 \\ \hline V_{VINST} & Logic Threshold Hysteresis & V_{HI}, Rising - V_{II}, Falling - V_{II}, Falling & 0.5 & 0.5 & 0.5 & 0.5 \\ \hline V_{MVST} & Logic Threshold Hysteresis & V_{HI}, Rising - V_{II}, Falling & 0.5 $	V <sub>DD_UVLO+</sub>	UVLO Trip Level V <sub>DD</sub> Rising	$LS_{IN} = 5 V, V_{DD} Ramps Up$		6.5		
Value   UVLO Trip Level (V <sub>800T</sub> - SW) Rling   HS <sub>IN</sub> = 5 V, V <sub>800T</sub> Ramps Dp   6.25      V <sub>900T.HYST</sub> UVLO (V <sub>800T</sub> - SW) Falling Hysteresis   HS <sub>IN</sub> = 5 V, V <sub>800T</sub> Ramps Down   0.5      LogicInue Time   V          V <sub>1</sub> Logic Threshold   HS <sub>IN</sub> , LS <sub>IN</sub> Falling    0.5      V <sub>1</sub> Logic Threshold Hysteresis   V <sub>1H</sub> Rising -V <sub>1L</sub> Falling   0.5       V <sub>1</sub> Logic Threshold Hysteresis   V <sub>1H</sub> Rising -V <sub>1L</sub> Falling   0.5       V <sub>1</sub> Logic fineshold Hysteresis   V <sub>1H</sub> Rising -V <sub>1L</sub> Falling   0.5       V <sub>1</sub> HS <sub>IN</sub> and LS <sub>IN</sub> Pull-Down Resistance   HS <sub>IN</sub> LS <sub>IN</sub> =5 V   4.5   7   1.1   KΩ     V <sub>1</sub> Lodelay <sub>1LS,on</sub> High side on propagation delay   SW = 0 V and LS FET turn-on   30       Lodelay <sub>1LS,off</sub> Ibl side off propagation delay   SW = 0 V and LS FET turn-off   30       Lodelay <sub>LS,off</sub> Ibl side off propagati	V <sub>DD_HYST</sub>	UVLO V <sub>DD</sub> Falling Hysteresis	$LS_{IN} = 5 V, V_{DD}$ Ramps Down		0.5		N N
VBLOD (VBLOD (VBLOD - SW) Falling Hysteresis   HS <sub>IN</sub> = 5 V, VBLOD VBLOD RAMPS DOWN   0.5   0     Logic Input Five   VIE   VIE <td>V<sub>BOOT_UVLO+</sub></td> <td>UVLO Trip Level (V<sub>BOOT</sub> - SW) Rising</td> <td>HS<sub>IN</sub> = 5 V, V<sub>BOOT</sub> Ramps Up</td> <td></td> <td>6.25</td> <td></td> <td>v</td>	V <sub>BOOT_UVLO+</sub>	UVLO Trip Level (V <sub>BOOT</sub> - SW) Rising	HS <sub>IN</sub> = 5 V, V <sub>BOOT</sub> Ramps Up		6.25		v
Logic Input Pins $V_{H}$ High-level Logic ThresholdHS <sub>IN</sub> , LS <sub>IN</sub> Rising2.4. $V_{L}$ Low-level Logic ThresholdHS <sub>IN</sub> , LS <sub>IN</sub> Falling.0.5 $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling0.5. $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling0.5. $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling0.5. $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling0.5. $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling0.5. $V_{HYST}$ Logic Threshold Hysteresis $V_{HI}$ Rising – $V_{L}$ Falling4.5711kQ $Dynamic Characteristics (Logic Input to output switching node) See Figure 4a and 4b for timing diagram and test circuit)L_{cdelayLS, ont}Low side on propagation delaySW = 60 V and HS FET turn-on30L_{delayLS, ont}Low side off propagation delaySW = 00 and LS FET turn-off30L_{matchoff}Delay matching LSOFF to HSONLS turn-off to HS turn-on0L_{matchoff}Delay matching HSOFF to LSONHS turn-off to HS turn-on or HS turn-off to LS turn-on5.V_{mis}SW to GND voltage slew rateLSIN = 0 V, HSIN = 0 V, SN = 48 V, IOUT = 10 A^{(213)}$ 27V/nsHigh Side International ColorSinge O V1014.5	V <sub>BOOT_HYST</sub>	UVLO (V <sub>BOOT</sub> - SW) Falling Hysteresis	HS <sub>IN</sub> = 5 V, V <sub>BOOT</sub> Ramps Down		0.5		
V <sub>H</sub> High-level Logic Threshold   HS <sub>IN</sub> , LS <sub>IN</sub> Rising   2.4   Image March     V <sub>L</sub> Low-level Logic Threshold   HS <sub>IN</sub> , LS <sub>IN</sub> Falling   0.8   0.8     V <sub>HYST</sub> Logic Threshold Hysteresis   V <sub>H</sub> Rising - V <sub>L</sub> Falling   0.5   7   11   kΩ     Dyname the second of the sec	Logic Input Pi	ins					
VILLow-level Logic ThresholdHSIN, LSIN, Falling0.8VVHYSTLogic Threshold HysteresisVH, Rising -VL, Falling0.50.5RINHSIN, and LSIN, Pull-Down ResistanceHSIN, LSIN = 5 V4.5711kQ <b>Dynamic Characteristics (Logic Input to output switching models and the fortiming diagram and test circuit)</b> L_delayLS, onHigh side on propagation delaySW = 0 V and HS FET turn-on301L_delayLS, onLow side off propagation delaySW = 0 V and LS FET turn-on301L_delayLS, onLow side off propagation delaySW = 0 V and LS FET turn-off301L_delayLS, onfHigh side off propagation delaySW = 0 V and LS FET turn-off301t_adelayLS, onfDelay matching LS <sub>0FF</sub> to HS <sub>ON</sub> LS turn-off to HS turn-on of HS turn-onf01t_matchonfDelay matching HS <sub>0FF</sub> to LS <sub>ON</sub> HS turn-off to LS turn-on or HS turn-onf to LS turn-on51VM_MminMinimum input pulse width50% to 50% width1511dV/dtS to GND voltage slaw rateLS <sub>N</sub> = 0 V, HS <sub>IN</sub> = 0 V > 5 V, V <sub>N</sub> = 48 V, Iour = 10 A <sup>(2)(3)</sup> 27VHigh side Arguadrant clampILOAD = +/10 A, HS <sub>IN</sub> & S W = 0 V10014.5mΩMKS_DS_LBARPHigh side 3''' quadrant clampILOAD = +/10 A, LS <sub>IN</sub> = 5 V, LS <sub>IN</sub> = 0 V339pFQoss, HSEFTOutput capacitance (V <sub>IN</sub> to SW)HS <sub>IN</sub> = 0 V, SW = 80 V, SW = 0 V339pFQoss, HSEFTOutput capacitance (V <sub>IN</sub> to SW) <td< td=""><td>V<sub>IH</sub></td><td>High-level Logic Threshold</td><td>HS<sub>IN</sub>, LS<sub>IN</sub> Rising</td><td>2.4</td><td></td><td></td><td></td></td<>	V <sub>IH</sub>	High-level Logic Threshold	HS <sub>IN</sub> , LS <sub>IN</sub> Rising	2.4			
V <sub>HYST</sub> Logic Threshold HysteresisV <sub>H</sub> Rising -V <sub>LL</sub> Falling0.5.R <sub>IN</sub> HS <sub>IN</sub> and LS <sub>IN</sub> Pull-Down ResistanceHS <sub>IN</sub> , LS <sub>IN</sub> = 5 V4.5711kΩ <b>Dynamic Char-teristics (Logic Input to output switching node)</b> See Figure 4a and 4b for timing diagram and test circuit) $t_{delayHS,onf}$ High side on propagation delaySW = 0 V and HS FET turn-on30. $t_{delayLS,onf}$ Low side on propagation delaySW = 60 V and LS FET turn-onf30. $t_{delayLS,off}$ High side off propagation delaySW = 0 V and LS FET turn-off30. $t_{delayLS,off}$ Low side off propagation delaySW = 0 V and LS FET turn-off30. $t_{natchoff}$ Delay matching LS <sub>OFF</sub> to HS <sub>ON</sub> LS turn-off to LS turn-on0. $t_{natchoff}$ Delay matching LS <sub>OFF</sub> to LS <sub>ON</sub> HS turn-off to LS turn-on or HS turn-on for LS turn-on5. $dV/dt$ SW to GND voltage slew rateLS $urn-off to HS turn-on or HS turn-off to LS turn-on5.dV/dtSW to GND voltage slew rateLS urn-off to HS turn-on or HS turn-off to LS turn-on20.dV/dtSW to GND voltage slew rateLS urn-off to HS turn-on or HS turn-off to LS turn-on20.dV/dtSW to GND voltage slew rateLS urn-off to HS turn-on or HS turn-off to LS turn-on1014.5mQdV/dtSW to GND voltage slew rateLS urn-off to HS turn-on20dV/dtSW to GND voltage slew rateLS urn-off to HS turn-off$	V <sub>IL</sub>	Low-level Logic Threshold	HS <sub>IN</sub> , LS <sub>IN</sub> Falling			0.8	V
$R_{IN}$ $HS_{IN}$ and $LS_{IN}$ Pull-Down Resistance $HS_{IN}$ , $LS_{IN} = 5V$ 4.5711 $K\Omega$ Dynamic Characteristics (Logic Input to output switching node) See Figure 4a and 4b for timing diagram and test circuit) $t_delay_{HS_onf}$ High side on propagation delay $SW = 0V$ and HS FET turn-on301 $t_delay_{LS_onf}$ Low side on propagation delay $SW = 60V$ and LS FET turn-onf301 $t_delay_{LS_onf}$ Low side off propagation delay $SW = 60V$ and LS FET turn-off301 $t_delay_{LS_onf}$ Low side off propagation delay $SW = 60V$ and LS FET turn-off301 $t_delay_{LS_onf}$ Low side off propagation delay $SW = 0V$ and LS FET turn-off301 $t_{natchonf}$ Delay matching LS <sub>OFF</sub> to HS <sub>ON</sub> LS turn-off to HS turn-on00 $t_{matchoff}$ Delay matching HS <sub>OFF</sub> to LS <sub>ON</sub> HS turn-off to LS turn-on51 $V_{lockout}$ Cross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on51 $VMM_{min}$ Minimum input pulse width50% to 50% width1527V/nsHigh Side Internet Power FET $Ro_{S(on),HS}$ High side FET $R_{DS(on)}$ $I_{LOAD} = +/-10A, HS_{IN} = 5V, LS_{IN} = 0V$ 1014.5mQ $V_{HS_{DS_{C},LS_{M}}$ Usite transmit of SIN $S_{IN} = 0V, SN = 48V, SN = 0V$ 339 $PF$ $Q_{OSS, HSFET}$ Output charge ( $V_{IN}$ to SN) $HS_{IN} = 0V, SN = 48V, SN = 0V$ 339 $PF$ $Q_{OSS, HSFET}$ Output charge	V <sub>IHYST</sub>	Logic Threshold Hysteresis	$V_{\rm H}$ Rising – $V_{\rm IL}$ Falling		0.5		
Dynamic Characteristics (Logic Input to output switching node) See Figure 4a and 4b for timing diagram and test circuit) $t_delay_{HS_om}$ High side on propagation delaySW = 0 V and HS FET turn-on301 $t_delay_{LS_om}$ Low side on propagation delaySW = 60 V and LS FET turn-on301 $t_delay_{LS_om}$ High side off propagation delaySW = 60 V and LS FET turn-onff301 $t_delay_{LS_off}$ Low side off propagation delaySW = 0 V and LS FET turn-off301 $t_{adelay_{LS_off}}$ Low side off propagation delaySW = 0 V and LS FET turn-off301 $t_{matchom}$ Delay matching LS <sub>OFF</sub> to HS <sub>ON</sub> LS turn-off to HS turn-on01 $t_{matchoff}$ Delay matching HS <sub>OFF</sub> to LS <sub>ON</sub> HS turn-off to LS turn-on or HS turn-on or 51 $t_{tockout}$ Cross-conduction lockout timeLS turn-off to HS turn-on or HS turn-on fot LS turn-on5 $WM_min$ Minimum input pulse width50% to 50% width151 $dV/dt$ SW to GND voltage slew rate $L_{SM} = 0.7, SW = 80.7, SW = 0.7, V_{N} = 48.7, louT = 10.4^{(2)(3)}$ 27V/nsHigh side FET R <sub>DS(on)</sub> $I_{LOAD} = +/-10.4, HS_{IN} = 5.7, LS_{IN} = 0.7, V_{IN} = 48.7, SW = 0.7, SW = 60.7, SW = 60.7, SW = 0.7, SW = 60.7, SW = 0.7$	R <sub>IN</sub>	HS <sub>IN</sub> and LS <sub>IN</sub> Pull-Down Resistance	$HS_{IN}, LS_{IN} = 5 V$	4.5	7	11	kΩ
t_delayHs_onHigh side on propagation delaySW = 0 V and HS FET turn-on30t_delayLs_onLow side on propagation delaySW = 60 V and LS FET turn-on30t_delayLs_offHigh side off propagation delaySW = 60 V and LS FET turn-off30t_delayLs_offLow side off propagation delaySW = 60 V and LS FET turn-off30t_delayLs_offLow side off propagation delaySW = 0 V and LS FET turn-off30t_delayLs_offDelay matching LSOFF to LSONLS turn-off to HS turn-on0t_matchoffDelay matching HSOFF to LSONHS turn-off to LS turn-on th Sturn-off to LS turn-on0t_lockoutCross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on5dV/dtSW to GND voltage slew rateLS_IN = 0 V, HSIN = 0 V > 5 V, VIN = 48 V, I_OUT = 10 A <sup>(2)(3)</sup> 27V/nsHigh side FET RDSIONI_LOAD = +/-10 A, HSIN = 5 V, LSIN = 0 V1014.5mΩVHS_DS_ClampHigh side STG quadrant clampI_LOAD = - 10 A, HSIN & LSIN = 0 VQoss_HSFETOutput capacitance (VIN to SW)HSIN = 0 V, VIN = 48 V, SW = 0 VQoss_HSFETOutput capacitance (VIN to SW)HSIN = 0 V, VIN = 48 V, SW = 0 VQoss_HSFETOutput capacitance (VIN to SW)HSIN = 0 V, VIN = 48 V, SW = 0 VQoss_HSFETOutput capacitance (VIN to SW)	Dynamic Char	acteristics (Logic Input to output switchin	ng node) See Figure 4a and 4b for timing diagram and test circuit	)			
t_delay_{L_{0.0}}Low side on propagation delaySW = 60 V and LS FET turn-on303010t_delay_{HS_off}High side off propagation delaySW = 60 V and LS FET turn-off303010t_delay_{LS_off}Low side off propagation delaySW = 0 V and LS FET turn-off303010t_delay_{LS_off}Low side off propagation delaySW = 0 V and LS FET turn-off301010t_atchoffDelay matching LS_{0FF} to LS_{0N}LS turn-off to HS turn-on0010t_ockoutCross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on510dV/dtSW to GND voltage slew rateLS_N = 0V, HS_IN = 0V $\rightarrow$ 5 V, V_IN = 48 V, I_{0UT} = 10 A <sup>(2)(3)</sup> 27V/nsHigh side FET R <sub>DS(on</sub> )I_LOAD = +/-10 A, HS_IN = 5 V, LS_IN = 0 V1014.5mΩVHS_DS_clampHigh side 3r <sup>d</sup> quadrant clampI_LOAD = +/-10 A, HS_IN = 5 V, LS_IN = 0 V22-2.5VLEAK_VIN-SWLeakage current (V_IN to SW)HS_IN = 0 V, SW = 80 V, SW = 0 V339pFQoss_HSFETOutput capacitance (V_IN to SW)HS_IN = 0 V, VIN = 48 V, SW = 0 V339pFQoss_HSFETOutput capacitance (V_IN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V26nCLow side Internal Power FETR_S(on)_LSLow side FET R_DS(on)I_LOAD = +/-10 A, LS_IN = 5 V, HS_IN = 0 V339pFQoss_HSFETOutput capacitance (V_IN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V339pFQoss_	t_delay <sub>HS_on</sub>	High side on propagation delay	SW = 0 V and HS FET turn-on		30		
t_delay_{HS_off}High side off propagation delaySW = 60 V and HS FET turn-off303010t_delay_{LS_off}Low side off propagation delaySW = 0 V and LS FET turn-off303010t_matchonDelay matching LS_OFF to HS_ONLS turn-off to HS turn-on0010t_matchoffDelay matching HS_OFF to LS_ONHS turn-off to LS turn-on0010ViccoutCross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on510V/dtSW to GND voltage slew rateLS in = 0V, HS_IN = 0V > 5 V, VIN = 48 V, IOUT = 10 A <sup>(2)(3)</sup> 27V/nsHigh Side Internal Power FETRosion)_HSHigh side FET RDS(on)ILOAD = +/-10 A, HS_IN = 5 V, LS_IN = 0V1014.5mQVH5_DS_ClampHigh side 3rd quadrant clampILOAD = +/-10 A, HS_IN = 5 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HS_IN = 0 V, SW = 80 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V339pFQoSS_HSFETDutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V26nCLow side FET RDS(on)ILOAD = +/-10 A, HS_IN S = 5 V, HS_IN = 0 V1014.5mQVH5_DS_ClampDutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V26nCLow Side BET RDS(on)ILOAD = +/-10 A, LS_IN = 5 V, HS_IN = 0 V1014.5 <td>t_delay<sub>LS_on</sub></td> <td>Low side on propagation delay</td> <td>SW = 60 V and LS FET turn-on</td> <td></td> <td>30</td> <td></td> <td></td>	t_delay <sub>LS_on</sub>	Low side on propagation delay	SW = 60 V and LS FET turn-on		30		
t_delayLS_offLow side off propagation delaySW = 0 V and LS FET turn-off30 $t_{matchon}$ Delay matching LS_OFF to HS_ONLS turn-off to HS turn-on0 $t_{matchoff}$ Delay matching HS_OFF to LS_ONHS turn-off to LS turn-on0 $t_{lockout}$ Cross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on5PWM_minMinimum input pulse width50% to 50% width15dV/dtSW to GND voltage slew rateLS I_IN = 0 V, HS_IN = 0 V $\Rightarrow$ 5 V, VIN = 48 V, I_OUT = 10 A <sup>(2)(3)</sup> 27V/nsHigh side FET R_DS(on)I_LOAD = +/-10 A, HS_IN = 5 V, LS_IN = 0 V1014.5mΩVHS_DS_ClampHigh side 3rd quadrant clampI_LOAD = -10 A, HS_IN = 5 V, LS_IN = 0 VQoSS_HSFETOutput capacitance (VIN to SW)HS_IN = 0 V, VIN = 48 V, SW = 0 V100210 $\mu A$ Coss_HSFETOutput capacitance (VIN to SW)HS_IN = 0 V, VIN = 48 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V339pFDelson_LSLow side FET RDS(on)I_LOAD = +/-10 A, LS_IN = 5 V, HS_IN = 0 VVHS_DS_ClampOutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 VUp advant clampI_LOAD = -10 A, HS_IN & SUN = 0 VHS_DS_Clamp	t_delay <sub>HS_off</sub>	High side off propagation delay	SW = 60 V and HS FET turn-off		30		
tmatchonDelay matching LSOFF to HSONLS turn-off to HS turn-on0tmatchoffDelay matching HSOFF to LSONHS turn-off to LS turn-on0tmatchoffDelay matching HSOFF to LSONHS turn-off to LS turn-on0tlockoutCross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on5PWM_minMinimum input pulse width50% to 50% width15dV/dtSW to GND voltage slew rateLS IN = 0 V → 5 V, VIN = 48 V, IOUT = 10 A (2)(3)27V/nsHigh Side Internal Power FETRoston, HSHigh side FET RDS(on)ILOAD = +/-10 A, HSIN = 5 V, LSIN = 0 V1014.5mΩVHS_DS_ClampHigh side 3rd quadrant clampILOAD = -10 A, HSIN & LSIN = 0 V-2-2.5VILEAK_VIN-SWLeakage current (VIN to SW)HSIN = 0 V, SW = 80 V, SW = 0 V339pFQoSS_HSFETOutput capacitance (VIN to SW)HSIN = 0 V, SW = 48 V, SW = 0 V339pFQoSS_HSFETOutput charge (VIN to SW)HSIN = 0 V, SW = 48 V, SW = 0 V26nCLow Side Internal Power FETRDS(on)_LSLow side FET RDS(on)ILOAD = +/-10 A, HSIN = 5 V, HSIN = 0 V26nCLow Side Internal Power FETULOAD = -10 A, HSIN & LSIN = 0 V1014.5mΩVHS_DS_ClampLow side FET RDS(on)ILOAD = +/-10 A, LSIN = 5 V, HSIN = 0 V26nCLow Side Internal Power FETULOAD = -10 A, HSIN & LSIN = 0 V26nCLow Side GET RDS(on)ILOAD = -10 A, HSIN & LSIN = 0 V22-2.5<	t_delay <sub>LS_off</sub>	Low side off propagation delay	SW = 0 V and LS FET turn-off		30		
$t_{matchoff}$ Delay matching HS <sub>OFF</sub> to LS <sub>ON</sub> HS turn-off to LS turn-on0 $t_{lockout}$ Cross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on5PWM_minMinimum input pulse width50% to 50% width15dV/dtSW to GND voltage slew rateLS $_{IN} = 0 V \rightarrow 5 V$ , $V_{IN} = 48 V$ , $I_{OUT} = 10 A^{(2)(3)}$ 27V/nsHigh Side Internal Power FETRpS(on)_HSHigh side FET RpS(on) $I_{LOAD} = +/-10 A$ , $HS_{IN} = 5 V$ , $LS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ High side 3rd quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} \& LS_{IN} = 0 V$ 22-2.5V $Q_{OSS_HSFET}$ Output capacitance ( $V_{IN}$ to SW)HS $_{IN} = 0 V$ , $SW = 80 V$ , $SW = 0 V$ 339pF $Q_{OSS_HSFET}$ Output charge ( $V_{IN}$ to SW)HS $_{IN} = 0 V$ , $SW = 48 V$ , $SW = 0 V$ 26nCLow Side Internal Power FET $R_{DS(on)_{LS}}$ Low side FET RpS(on) $I_{LOAD} = +/-10 A$ , $LS_{IN} = 5 V$ , $LS_{IN} = 0 V$ 339pF $Q_{OSS_HSFET}$ Output capacitance ( $V_{IN}$ to SW)HS $_{IN} = 0 V$ , $SW = 48 V$ , $SW = 0 V$ 26nCLow Side Internal Power FET $R_{DS(on)_{LS}}$ Low side FET RpS(on) $I_{LOAD} = +/-10 A$ , $LS_{IN} = 5 V$ , $HS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side FET RpS(on) $I_{LOAD} = -10 A$ , $HS_{IN} \& SV = 0 V$ 26nCLow Side Internal Power FETULAD $I_{LOAD} = -10 A$ , $HS_{IN} \& SV_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$	t <sub>matchon</sub>	Delay matching LS <sub>OFF</sub> to HS <sub>ON</sub>	LS turn-off to HS turn-on		0		ns
$t_{lockout}$ Cross-conduction lockout timeLS turn-off to HS turn-on or HS turn-off to LS turn-on5PWM_minMinimum input pulse width50% to 50% width15dV/dtSW to GND voltage slew rateLS $_{IN} = 0 V$ , HS $_{IN} = 0 V \rightarrow 5 V$ , $V_{IN} = 48 V$ , $I_{OUT} = 10 A^{(2)(3)}$ 27V/nsHigh Side Internal Power FET $R_{DS(on)_HS}$ High side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A$ , $HS_{IN} = 5 V$ , $LS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ High side 3rd quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} \otimes 10 V$ 22-2.5V $V_{HS_DS_Clamp}$ Leakage current ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $SW = 80 V$ , $SW = 0 V$ 100210 $\mu A$ $C_{OSS_HSFET}$ Output capacitance ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $SW = 48 V$ , $SW = 0 V$ 26nCLow Side Internal Power FET $R_{DS(on)_{LS}}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A$ , $LS_{IN} = 5 V$ , $HS_{IN} = 0 V$ 26nC $Q_{OSS_HSFET}$ Output capacitance ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $SW = 48 V$ , $SW = 0 V$ 26nCLow Side Internal Power FET $R_{DS(on)_{LS}}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A$ , $LS_{IN} = 5 V$ , $HS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side 3rd quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} \otimes LS_{IN} = 0 V$ 26nC $V_{HS_DS_Clamp}$ Low side 3rd quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} \otimes LS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side 3rd quadran	t <sub>matchoff</sub>	Delay matching HS <sub>OFF</sub> to LS <sub>ON</sub>	HS turn-off to LS turn-on		0		
PWM_minMinimum input pulse width50% to 50% width15dV/dtSW to GND voltage slew rateLSLS0 V + SV, VIN48 V, IOUT10 A27V/nsHigh Side Internal Power FET $R_{DS(on),HS}$ High side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A$ , $HS_{IN} = 5 V$ , $LS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ High side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} = 5 V$ , $LS_{IN} = 0 V$ -2-2.5V $I_{LEAK_VIN-SW}$ Leakage current ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $SW = 80 V$ , $SW = 0 V$ 100210 $\mu A$ $C_{OSS_HSFET}$ Output capacitance ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $V_{IN} = 48 V$ , $SW = 0 V$ 339pF $Q_{OSS_HSFET}$ Output charge ( $V_{IN}$ to SW) $HS_{IN} = 0 V$ , $SW = 48 V$ , $SW = 0 V$ 26nCLow Side Internal Power FET $R_{DS(on), LS}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A$ , $LS_{IN} = 5 V$ , $HS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = -10 A$ , $HS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} = 0 V$ 1014.5m $\Omega$ $V_{HS_DS_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} = 0 V$ 22-2.5V $V_{HS_DS_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} & LS_{IN} = 0 V$ -2-2.5V $V_{HS_DS_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 A$ , $HS_{IN} & LS_{IN} =$	t <sub>lockout</sub>	Cross-conduction lockout time	LS turn-off to HS turn-on or HS turn-off to LS turn-on		5		
dV/dtSW to GND voltage slew rateLS <sub>IN</sub> = 0 V, HS <sub>IN</sub> = 0 V → 5 V, V <sub>IN</sub> = 48 V, I <sub>OUT</sub> = 10 A $^{(2)(3)}$ 27V/nsHigh Side Internal Power FETR <sub>DS(on),HS</sub> High side FET R <sub>DS(on)</sub> I <sub>LOAD</sub> = +/-10 A, HS <sub>IN</sub> = 5 V, LS <sub>IN</sub> = 0 V1014.5mΩV <sub>HS_DS_Clamp</sub> High side 3 <sup>rd</sup> quadrant clampI <sub>LOAD</sub> = -10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V-2-2.5VI <sub>LEAK_VIN-SW</sub> Leakage current (V <sub>IN</sub> to SW)HS <sub>IN</sub> = 0 V, SW = 80 V, SW = 0 V100210µAC <sub>OSS_HSFET</sub> Output capacitance (V <sub>IN</sub> to SW)HS <sub>IN</sub> = 0 V, V <sub>IN</sub> = 48 V, SW = 0 V339pFQ <sub>OSS_HSFET</sub> Output charge (V <sub>IN</sub> to SW)HS <sub>IN</sub> = 0 V, SW = 48 V, SW = 0 V26nCLow Side Internal Power FETN1014.5mΩR <sub>DS(on)_LS</sub> Low side FET R <sub>DS(on)</sub> I <sub>LOAD</sub> = +/-10 A, LS <sub>IN</sub> = 5 V, HS <sub>IN</sub> = 0 V1014.5mΩV <sub>HS_DS_Clamp</sub> Low side 3 <sup>rd</sup> quadrant clampI <sub>LOAD</sub> = -10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V1014.5mΩV <sub>HS_DS_Clamp</sub> Low side 3 <sup>rd</sup> quadrant clampI <sub>LOAD</sub> = -10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V1014.5mΩ	PWM_min	Minimum input pulse width	50% to 50% width		15		
High Side Internal Power FET $R_{DS(on)\_HS}$ High side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 \text{ A}$ , $HS_{IN} = 5 \text{ V}$ , $LS_{IN} = 0 \text{ V}$ 1014.5 $m\Omega$ $V_{HS\_DS\_Clamp}$ High side $3^{rd}$ quadrant clamp $I_{LOAD} = -10 \text{ A}$ , $HS_{IN} \otimes LS_{IN} = 0 \text{ V}$ -2-2.5 $V$ $I_{LEAK\_VIN-SW}$ Leakage current ( $V_{IN}$ to SW) $HS_{IN} = 0 \text{ V}$ , SW = 80 V, SW = 0 V100210 $\mu A$ $C_{OSS\_HSFET}$ Output capacitance ( $V_{IN}$ to SW) $HS_{IN} = 0 \text{ V}$ , $V_{IN} = 48 \text{ V}$ , $SW = 0 \text{ V}$ 339pF $Q_{OSS\_HSFET}$ Output charge ( $V_{IN}$ to SW) $HS_{IN} = 0 \text{ V}$ , $SW = 48 \text{ V}$ , $SW = 0 \text{ V}$ 26nCLow Side Internal Power FET $R_{DS(on)\_LS}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 \text{ A}$ , $LS_{IN} = 5 \text{ V}$ , $HS_{IN} = 0 \text{ V}$ 1014.5 $m\Omega$ $V_{HS\_DS\_Clamp}$ Low side 3rd quadrant clamp $I_{LOAD} = -10 \text{ A}$ , $HS_{IN} \otimes LS_{IN} = 0 \text{ V}$ 201014.5 $m\Omega$ $V_{HS\_DS\_Clamp}$ Low side 3rd quadrant clamp $I_{LOAD} = -10 \text{ A}$ , $HS_{IN} \otimes LS_{IN} = 0 \text{ V}$ -2-2.5 $V$	dV/dt	SW to GND voltage slew rate	$LS_{IN} = 0 V, HS_{IN} = 0 V \rightarrow 5 V, V_{IN} = 48 V, I_{OUT} = 10 A^{(2)(3)}$		27		V/ns
R DS(on)_HSHigh side FET R DS(on)I LOAD = +/-10 A, HS IN $\approx$ 5 V, LS IN $\approx$ 0 V1014.5mQVHS_DS_ClampHigh side 3rd quadrant clampI LOAD = -10 A, HS IN $\approx$ LS IN $\approx$ 0 V-2-2.5VI LEAK_VIN-SWLeakage current (V IN to SW)HS IN $\approx$ 0 V, SW $\approx$ 80 V, SW $\approx$ 0 V100210 $\mu$ ACOSS_HSFETOutput capacitance (V IN to SW)HS IN $\approx$ 0 V, V IN $\approx$ 48 V, SW $\approx$ 0 V339pFQOSS_HSFETOutput charge (V IN to SW)HS IN $\approx$ 0 V, SW $\approx$ 48 V, SW $\approx$ 0 V26nCLow Side Internal Power FETTT1014.5mQVHS_DS_ClampLow side FET R DS(on)I LOAD $=$ +/-10 A, LS IN $=$ 5 V, HS IN $=$ 0 V1014.5mQVHS_DS_ClampLow side 3rd quadrant clampI LOAD $=$ -10 A, HS IN $\approx$ 20 V-2-2.5VVHS IN $=$ 0 V, SW $=$ 80 V, SW $=$ 80 V-2-2.5V	High Side Inte	ernal Power FET	· · · · · · · · · · · · · · · · · · ·				
V_{HS_DS_Clamp}High side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 \text{ A}, HS_{IN} \& LS_{IN} = 0 \text{ V}$ -2-2.5V $I_{LEAK_VIN-SW}$ Leakage current (V <sub>IN</sub> to SW) $HS_{IN} = 0 \text{ V}, SW = 80 \text{ V}, SW = 0 \text{ V}$ 100210 $\mu \text{A}$ $C_{OSS\_HSFET}$ Output capacitance (V_{IN} to SW) $HS_{IN} = 0 \text{ V}, SW = 80 \text{ V}, SW = 0 \text{ V}$ 339pF $Q_{OSS\_HSFET}$ Output charge (V_{IN} to SW) $HS_{IN} = 0 \text{ V}, V_{IN} = 48 \text{ V}, SW = 0 \text{ V}$ 26nCLow Side Internal Power FET $R_{DS(on)\_LS}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 \text{ A}, LS_{IN} = 5 \text{ V}, HS_{IN} = 0 \text{ V}$ 1014.5m $\Omega$ $V_{HS\_DS\_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 \text{ A}, HS_{IN} \& LS_{IN} = 0 \text{ V}$ -2-2.5V $V_{HS\_DS\_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 \text{ A}, HS_{IN} \& SN_{IN} = 0 \text{ V}$ -2-2.5V	R <sub>DS(on) HS</sub>	High side FET R <sub>DS(on)</sub>	I <sub>LOAD</sub> = +/-10 A, HS <sub>IN</sub> = 5 V, LS <sub>IN</sub> = 0 V		10	14.5	mΩ
Leakage current (V_IN to SW)HS_IN = 0 V, SW = 80 V, SW = 0 V100210 $\mu A$ $C_{OSS\_HSFET}$ Output capacitance (V_IN to SW)HS_IN = 0 V, V_IN = 48 V, SW = 0 V339pF $Q_{OSS\_HSFET}$ Output charge (V_IN to SW)HS_IN = 0 V, SW = 48 V, SW = 0 V26nCLow Side Internal Power FET $R_{DS(on)\_LS}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 A, LS_{IN} = 5 V, HS_{IN} = 0 V$ 1014.5 $m\Omega$ $V_{HS\_DS\_Clamp}$ Low side 3rd quadrant clamp $I_{LOAD} = -10 A, HS_{IN} & LS_{IN} = 0 V$ -2-2.5VLow Side grad quadrant clamp $I_{S} = 0V SW = 80 V$ 150330140140	V <sub>HS DS Clamp</sub>	High side 3 <sup>rd</sup> quadrant clamp	I <sub>LOAD</sub> = - 10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V		-2	-2.5	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	ILEAK VIN-SW	Leakage current (V <sub>IN</sub> to SW)	HS <sub>IN</sub> = 0 V, SW = 80 V, SW = 0 V		100	210	μA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	COSS HSEFT	Output capacitance (V <sub>IN</sub> to SW)	$HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V$		339		pF
Dow Side Internal Power FET   RDS(on)_LS Low side FET RDS(on) ILOAD = +/-10 A, LS <sub>IN</sub> = 5 V, HS <sub>IN</sub> = 0 V 10 14.5 m $\Omega$ VHS_DS_Clamp Low side 3 <sup>rd</sup> quadrant clamp I_LOAD = -10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V -2 -2.5 V   I Loakago gurgent (SW(to GND)) IS = 0V/SW = 80 V 150 310 110	Q <sub>OSS HSEET</sub>	Output charge (V <sub>IN</sub> to SW)	$HS_{IN} = 0 V, SW = 48 V, SW = 0 V$		26		nC
$R_{DS(on)\_LS}$ Low side FET $R_{DS(on)}$ $I_{LOAD} = +/-10 \text{ A}, LS_{IN} = 5 \text{ V}, HS_{IN} = 0 \text{ V}$ 1014.5 $m\Omega$ $V_{HS\_DS\_Clamp}$ Low side 3 <sup>rd</sup> quadrant clamp $I_{LOAD} = -10 \text{ A}, HS_{IN} \& LS_{IN} = 0 \text{ V}$ -2-2.5 $V$ $I_{LOAD} = -10 \text{ A}, HS_{IN} \& LS_{IN} = 0 \text{ V}$ $I_{LOAD} = -10 \text{ A}, HS_{IN} \& LS_{IN} = 0 \text{ V}$ -2-2.5 $V$	Low Side Internal Power FET						
$V_{HS_{DS_{Clamp}}} \text{ Low side 3^{rd} quadrant clamp} \qquad I_{LOAD} = -10 \text{ A}, \text{HS}_{IN} \& \text{LS}_{IN} = 0 \text{ V} \qquad -2  -2.5  \text{V}$	R <sub>DS(on)</sub> LS	Low side FET R <sub>DS(on)</sub>	$I_{LOAD} = +/-10 \text{ A}, \text{ LS}_{IN} = 5 \text{ V}, \text{ HS}_{IN} = 0 \text{ V}$		10	14.5	mΩ
$\frac{1}{1} = \frac{1}{10} =$	V <sub>HS DS Clamp</sub>	Low side 3 <sup>rd</sup> quadrant clamp	I <sub>LOAD</sub> = - 10 A, HS <sub>IN</sub> & LS <sub>IN</sub> = 0 V		-2	-2.5	V
1 I FAK SW-GND   LEaraye current (3νν to GIVD)   LS <sub>IN</sub> = 0 V, SVV = 00 V     ISU   310   UA	ILEAK SW-GND	Leakage current (SW to GND)	LS <sub>IN</sub> = 0 V, SW = 80 V		150	310	μA
$C_{WFL1}$ HV well capacitance (SW to GND) HS <sub>IN</sub> = 0 V, V <sub>IN</sub> = 48 V, SW = 48 V 57		HV well capacitance (SW to GND)	HS <sub>IN</sub> = 0 V, V <sub>IN</sub> = 48 V, SW = 48 V		57		
$C_{OSS   SFFT} \qquad Output capacitance (SW to GND) \qquad LS_{IN} = 0 V, SW = 48 V \qquad 396 \qquad PF$	COSS I SEFT	Output capacitance (SW to GND)	$LS_{IN} = 0 V, SW = 48 V$		396		pF
$Q_{OSS_{\perp}SEET}  Output charge (SW to GND) \qquad \qquad LS_{IN} = 0 V. SW = 48 V \qquad \qquad 31 \qquad nC$		Output charge (SW to GND)	$LS_{IN} = 0 V, SW = 48 V$		31		nC
) Parameters that show only typical value are guaranteed by design and may not be tested in production	(1) Parameters th	hat show only typical value are guaranteed by d	esign and may not be tested in production		1		_

(2) Measured using EPC90120 configured in a Buck converter operating at  $V_{IN} = 48$  V to  $V_{OUT} = 12$  V,  $f_{SW} = 1$  MHz, L = 2.2  $\mu$ H,  $I_{OUT} = 10$  A (3) Maximum turn-on dV/dt is defined by an internal resistor limiting the gate charging current



Figure 4b: Logic Input to Switch-node Waveforms



### **Table 1: Operational Truth Table**

Truth Table						
V <sub>DD</sub>	V <sub>boot</sub> –SW	HS <sub>IN</sub>	LS <sub>IN</sub>	HS FET	LS FET	
<uvlo< td=""><td>-</td><td>-</td><td>-</td><td>OFF</td><td>OFF</td></uvlo<>	-	-	-	OFF	OFF	
	<uvlo< td=""><td>-</td><td>0</td><td>OFF</td><td>OFF</td></uvlo<>	-	0	OFF	OFF	
>UVLU		-	1	OFF	ON	
>UVLO		0	0	OFF	OFF	
		0	1	OFF	ON	
		1	0	ON	OFF	
		1	1	O	FF	

# **Application Information**

#### **General Description**

The EPC2152 ePower<sup>TM</sup> Stage IC integrates a half-bridge gate driver with internal high side and low side FETs. Integration is implemented using EPC's proprietary GaN IC technology. The monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits for controlling the high side and low side eGaN output FETs, configured as a half-bridge power stage.

#### Synchronous bootstrap FET

The IC uses a synchronous bootstrap FET between  $V_{DD}$  and  $V_{BOOT}$  to charge the bootstrap capacitor. This bootstrap FET is activated only after the LS power FET is turned on, to avoid overcharging the bootstrap capacitor during deadtimes, when the switch-node voltage can be negative. The use of a GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage of the synchronous bootstrap FET is the lower voltage drop of approximately 100 mV compared to the 0.6 – 0.7 V of a typical Si bootstrap diode. As a result, the V<sub>BOOT</sub> voltage is maintained close to the V<sub>DD</sub> voltage, allowing the HS and LS gate drive circuits to have similar gate drive currents and dynamic performance.

### **Protection Circuits**

The EPC2152 integrates driver protection and under voltage lockout (UVLO) circuits for V<sub>DD</sub> and V<sub>BOOT</sub>. These protection circuits allow for the proper operation of the driver as shown in Table 1.

Separate and independent high side  $(HS_{IN})$  and low side  $(LS_{IN})$  logic control inputs allow external controllers to set the desired deadtimes for optimal operating efficiency. Cross conduction lockout logic commands both FETs off when both logic inputs are simultaneously high. Figure 5 shows how the logic inputs interact with each other. Here the timing diagram applies to HS FET and LS FET in half-bridge configuration and current is in the positive direction going out of the half-bridge.

When HSIN and LSIN are logic high at the same time, both HS FET and LS FET will shut off. A built-in lockout time of t\_lockout is added to guarantee a minimum deadtime.

### Figure 5: Input-to-Output Timing Diagram



(Current flowing OUT of SW node)

#### **Layout Guidelines**

Monolithic integration of the half-bridge output FETs as well as their associated gate drivers significantly reduce parasitic common source inductance (CSI) and gate drive loop inductance. What remains is the high frequency power loop inductance, controlled by the PCB layout and the components in the loop, the DC input capacitors and the power stage. Experimental data confirmed that the efficiency curves can be impacted by as much as 4% depending on the power loop inductance varying from 0.4 nH to 3 nH. Another negative effect of excessive power loop inductance is the overvoltage spike at the SW node. Decreasing the high frequency loop inductance results in lower voltage overshoot, increased input voltage capability, and reduced EMI.

A recommended layout for the EPC2152 device is shown in Figure 6a based on EPC90120 development board. This PCB layout uses the concept of creating a low-profile magnetic field cancellation loop in a multilayer PCB as shown in Figure 6b. The design utilizes the first inner layer connected to the GND plane as a power loop return path. Separated only by a thin substrate, the top layer power loop and first inner layer current return path directly underneath generate opposing magnetic fields with induced currents that have opposite direction. The result is a cancellation of magnetic fields that translates into a reduction in parasitic inductance.

#### **Figure 6a: Top View**



#### **Figure 6b: Side View**



#### **Switching Speed**

The EPC2152 device is tuned to switch at around 1.5 ns at 48 V V<sub>IN</sub> to minimize output FET switching losses while keeping the voltage overshoot at the SW pin within an acceptable level. Using the recommended layout guidelines, shown in Figure 6, the parasitic loop inductance can be reduced to less than 0.2 nH, as demonstrated in **EPC90120 development board**.

#### EPC90120 Development Board

To simplify the evaluation of EPC2152, EPC offers the EPC90120 development board. A photo with a top view of the board and its functional block diagram are shown in Figure 7. The board can be easily configured to operate the power stage in either a buck or boost converter. The layout supports optimal switching performance using the recommended layout guideline. And various probe points are included to facilitate waveforms and efficiency measurement.

#### Figure 7a: EPC90120 Development Board

(see EPC90120 Quick Start Guide for details)



#### Figure 7b: EPC90120 Functional Block Diagram



#### **Load Current Rating**

The Power Stage Load Current listed in this datasheet is defined as the load current of a Buck converter using EPC2152 that results in a device case temperature of 100°C (assuming 400 LFM of forced cooling and no heatsink). The data is based on experimental measurements of the EPC90120 development board configured as a Buck converter with  $V_{IN} = 48 \text{ V}$ ,  $V_{OUT} = 12 \text{ V}$ ,  $L = 2.2 \mu$ H, and 1 MHz of switching frequency. Without a heatsink installed, most of the energy dissipated within the EPC2152 device flows towards the PCB through the solder pads, and from there, to the ambient.

For higher current, dual sided cooling can be implemented by installing a heatsink as shown in Figure 8. With this configuration, heat can flow from the junction towards the solder bumps and the board, or in the opposite direction, to the case and heatsink. This dual heat flow path translates into lower thermal resistance and therefore lower junction temperature for the same power dissipation. To maximize heat dissipation to the heatsink, a thin thermal interface material (TIM) with high-thermal conductivity, is recommended. More details and recommended part numbers can be found in the Thermal Considerations sections of the EPC90120 Quick Start Guide.



**Heat paths** 

Thermal shim

#### **Figure 8: Thermal Concept of Dual Sided Cooling**

Decoupling capacitors

# **Packaging information**

#### **DIE OUTLINE - PAD VIEW**



# eGaN<sup>®</sup> FET DATASHEET

## EPC2152



#### eGaN<sup>®</sup> FET DATASHEET

# EPC2152

#### TAPE AND REEL CONFIGURATION



	Dimension (mm)			
EPC2152 (Note 1)	Target	MIN	MAX	
a	12.00	11.90	12.30	
b	1.75	1.65	1.85	
c (Note 2)	5.50	5.45	5.55	
d	4.00	3.90	4.10	
е	8.00	7.90	8.10	
f (Note 2)	2.00	1.95	2.05	
g	1.50	1.50	1.60	

#### Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

#### **DIE MARKINGS**



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