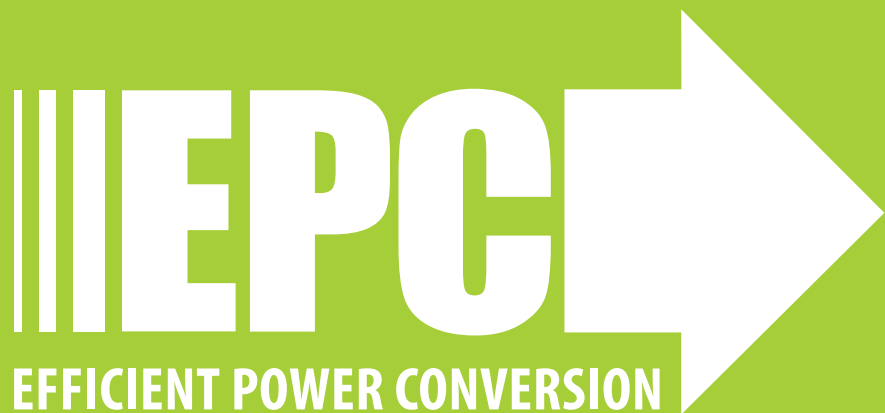


Development Board EPC9001

Quick Start Guide

40 V Half-Bridge with Gate Drive, Using EPC2015



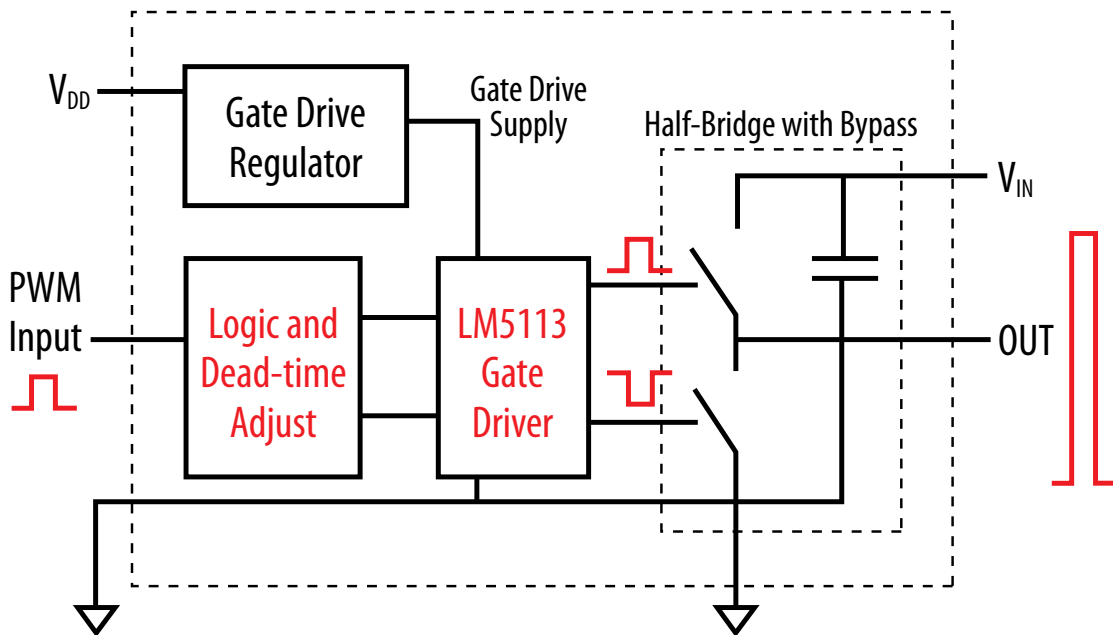


Figure 1: Block Diagram of EPC9001 Development Board

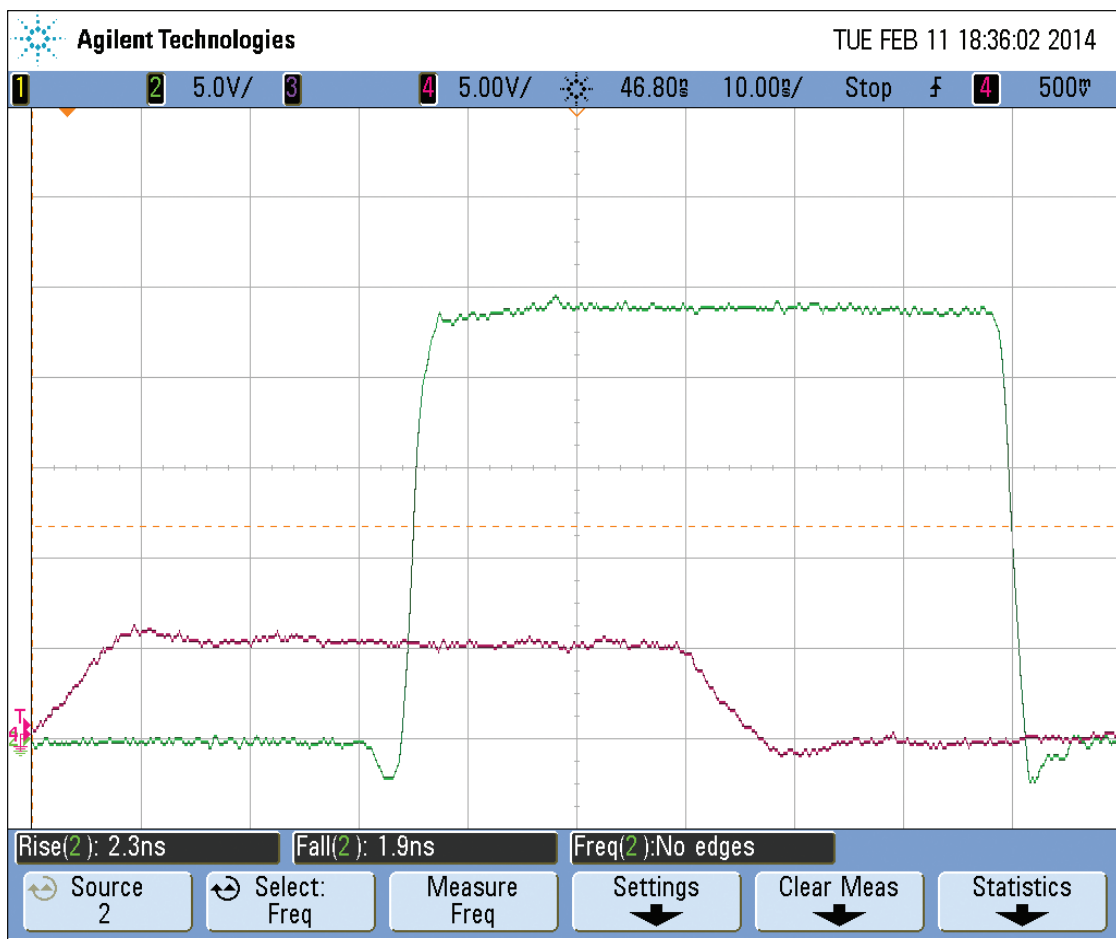


Figure 4: Typical Waveforms for $V_{IN} = 24\text{ V}$ to $1.2\text{ V}/15\text{ A}$ (500kHz) Buck converter
 CH1: V_{PWM} Input voltage – CH3: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

Quick Start Procedure

Development board EPC9001 is easy to set up to evaluate the performance and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6).
2. With power off, connect the switch node of the half bridge OUT (J3).
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and
4. With power off, connect the input PWM control signal to PWM (J2,
5. Turn on the gate drive supply – make sure the supply is between 7
6. Turn on the bus voltage to the required value (do not exceed the a
7. Turn on the controller / PWM input source and probe switching no
8. Once operational, adjust the bus voltage and load PWM control with efficiency and other parameters.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to use an oscilloscope probe tip through the large via on the switch node (designed for this purpose). See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9001 development board showcases the EPC2015 *eGaN* FET. Although these devices, their relatively smaller size does magnify the thermal management requirements due to ambient temperature and convection cooling. The addition of heat-sinking and cooling devices, but care must be taken to not exceed the absolute maximum die temperature.

NOTE. The EPC9001 development board does not have any current or thermal

performance of the EPC2015 *eGaN* FET. Refer to Figure 2 for proper connect

) and ground / return to $-V_{IN}$ (J7, J8).

3, J4) to your circuit as required.

and ground return to $-V_{DD}$ (J1, Pin-2).

Pin-1) and ground return to any of the remaining J2 pins.

7 V and 12 V range.

absolute maximum voltage of 40 V on V_{OUT}).

mode to see switching operation.

within the operating range and observe the output switching behavior,

be taken to avoid long ground leads. Measure the switch node (OUT) by placing the
(purpose) and grounding the probe directly across the GND terminals provided. See

ough the electrical performance surpasses that for traditional silicon de-
requirements. The EPC9001 is intended for bench evaluation with low am-
and forced air cooling can significantly increase the current rating of these
temperature of 125°C.

mal protection on board.

DESCRIPTION

The EPC9001 development board is a 40 V maximum device voltage, 15 A maximum output current, half bridge with onboard gate drives, featuring the EPC2015 enhancement mode (*eGaN*[®]) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2015 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9001 development board is 2" x 1.5" and contains not only two EPC2015 *eGaN* FET in a half bridge configuration using

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS
V _{DD}	Gate Drive Input Supply Range	
V _{IN}	Bus Input Voltage Range	
V _{OUT}	Switch Node Output Voltage	
I _{OUT}	Switch Node Output Current	
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High'
		Input 'Low'
	Minimum 'High' State Input Pulse Width	V _{PWM} rise and fall time
	Minimum 'Low' State Input Pulse Width	V _{PWM} rise and fall time

* Assumes inductive load, maximum current depends on die temperature – actual maximum current

Limited by time needed to 'refresh' high side bootstrap supply voltage.

the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

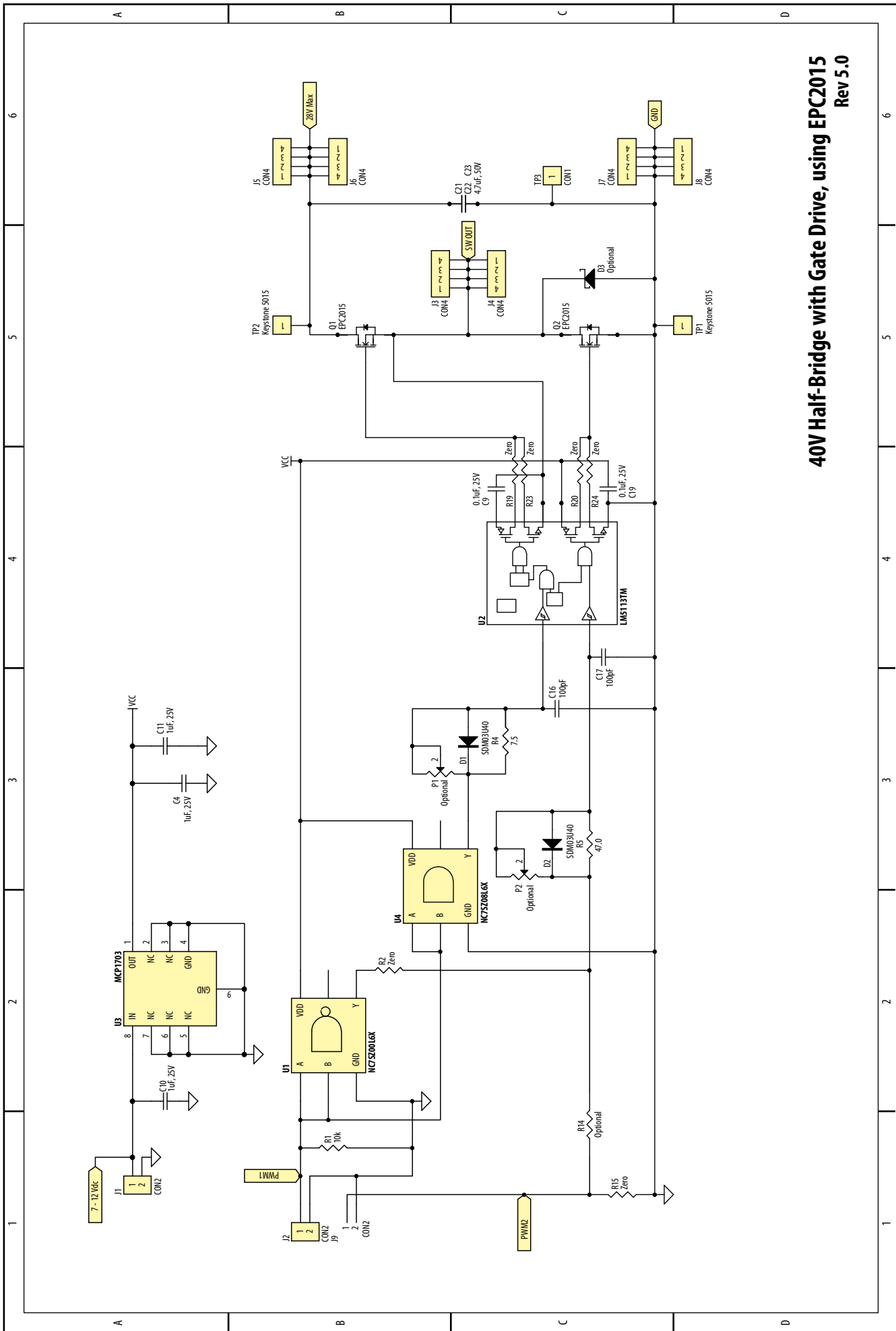
For more information on the EPC2015s *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

	MIN	MAX	UNITS
	7	12	V
		28*	V
		40	V
		15*	A
	3.5	6	V
	0	1.5	V
$t_{\text{e}} < 10\text{ns}$	60		ns
$t_{\text{e}} < 10\text{ns}$	200#		ns

Values are subject to switching frequency, bus voltage and thermals.

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	3	C4, C10, C11,	Capacitor, 1uF, 10%, 25V, X5R	Murata, GRM188R61E105KA12D
2	2	C16, C17	Capacitor, 100pF, 5%, 50V, NP0	Kemet, C0402C101K5GACTU
3	2	C9, C19	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
4	3	C21, C22, C23	Capacitor, 4.7uF, 10%, 50V, X5R	TDK, C2012X5R1H475K125AB
5	2	D1, D2	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
6	3	J1, J2, J9	Connector	2pins of Tyco, 4-103185-0
7	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
8	2	Q1, Q2	eGaN® FET	EPC, EPC2015
9	1	R1	Resistor, 10.0K, 5%, 1/8W	Stackpole, RMCF0603FT10K0
10	2	R2, R15	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603ZT0R00
11	1	R4	Resistor, 7.5 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT7R50
12	1	R5	Resistor, 47 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT47R0
13	4	R19, R20, R23, R24	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
14	2	TP1, TP2	Test Point	Keystone Elect, 5015
15	1	TP3	Connector	1/40th of Tyco, 4-103185-0
16	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
17	1	U2	I.C., Gate driver	Texas Instruments, LM5113TME
18	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
19	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
20	0	R14	Optional Resistor	
21	0	D3	Optional Diode	
22	0	P1, P2	Optional Potentiometer	



40V Half-Bridge with Gate Drive, using EPC2015
 Rev 5.0

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