Evaluation Board EPC9022/23/24/25/27/28/29/30 Quick Start Guide

Half-Bridge with Gate Drive using EPC8000 Family

February 15, 2015

Version 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The evaluation board is in a half bridge topology with onboard gate drives, featuring the EPC8000 family of high frequency enhancement mode (eGaN®) field effect transistors (FETs). The purpose of these evaluation boards is to simplify the evaluation process of the EPC8000 family of eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The evaluation board is 2" x 1.5" and contains two eGaN FETs in a half bridge configuration using the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC8000 family of eGaN FETs, please refer to the datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range	40 V devices; EPC9024, EPC9027, EPC9028		28*	V
		65 V devices; EPC9022, EPC9025, EPC9029		45*	V
		100 V devices; EPC9023, EPC9030		70*	V
V_{OUT}	Switch Node Output Voltage	40 V devices; EPC9024, EPC9027, EPC9028		40	V
		65 V device EPC9022, EPC9025, EPC9029		65	V
		100 V devices; EPC9023, EPC9030		100	V
I_{OUT}	Switch Node Output Current	40 V device EPC9024		4.4*	A
		40 V device EPC9027		3.5*	A
		40 V device EPC9028		2.2*	A
		65 V device EPC9022		1.6*	A
		65 V device EPC9025		2.2*	A
		65 V device EPC9029		3.5*	A
		100 V device EPC9023		2.2*	A
		100 V device EPC9030		3.2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
F_{MIN}	Minimum Switching Frequency	Bootstrap Capacitor Limited	500		kHz
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	20		ns
	Minimum 'Low' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50†		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
† Limited by time needed to 'refresh' high side bootstrap supply voltage.

QUICK START PROCEDURE

The evaluation board is easy to set up to evaluate the performance of the eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on V_{OUT} as indicated in the table below:
   a. EPC9022, 65 V
   b. EPC9023, 100 V
   c. EPC9024, 40 V
   d. EPC9025, 65 V
   e. EPC9027, 40 V
   f. EPC9028, 40 V
   g. EPC9029, 65 V
   h. EPC9030, 100 V
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The evaluation board showcases the EPC8000 family of eGaN FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The evaluation board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The evaluation board does not have any current or thermal protection on board.

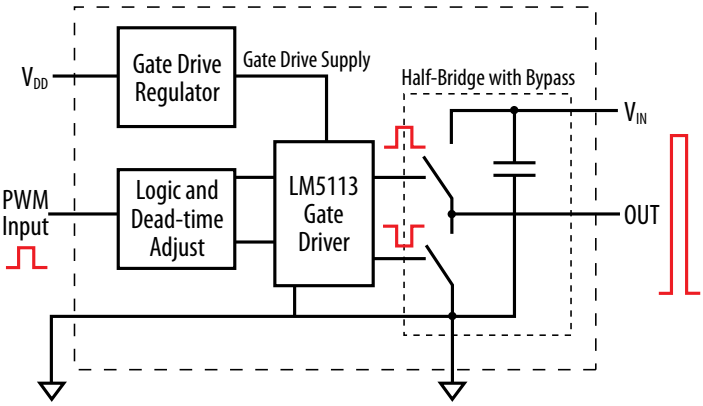

Figure 1: Block Diagram of Evaluation Board

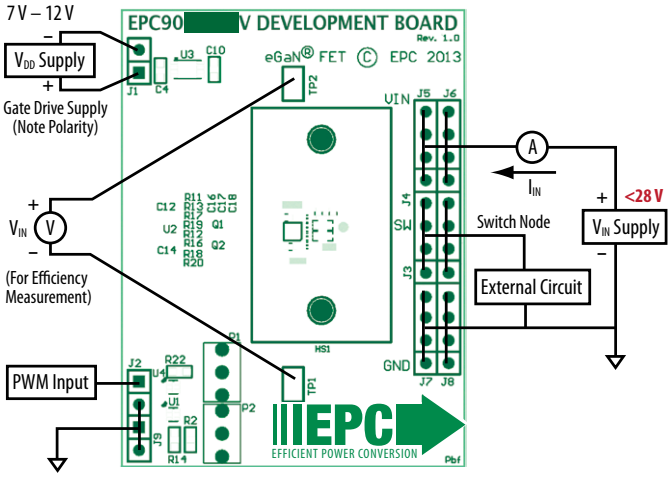

Figure 2: Proper Connection and Measurement Setup

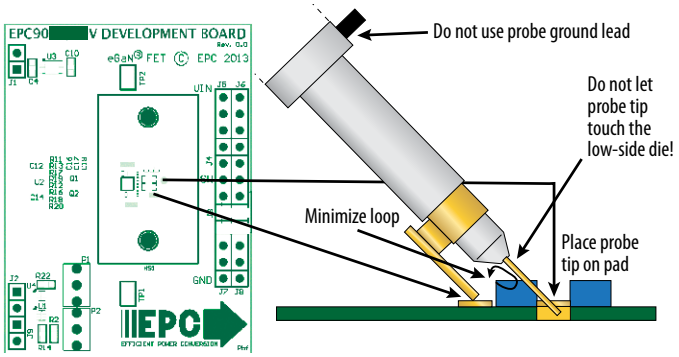

Figure 3: Proper Measurement of Switch Node – OUT

Figure 4: Typical Waveforms for V_{IN} = 28 V to 3.3 V/4 A (5 MHz) Buck converter
CH2: (V_{OUT}) Switch node voltage –– CH4: V_{PWM} Input voltage

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9022/23/24/25/27/28/29/30 landing page at:
https://epc-co.com/epc/products/demo-boards/epc9022

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