

# Development Board EPC9060/61 Quick Start Guide

*Half-bridge with Gate Drive  
for EPC2030/31*

Revision 2.0



## DESCRIPTION

These development boards are in a half-bridge topology with onboard gate drives, featuring the EPC2030/31 eGaN® field effect transistors (FETs). The purpose of these development boards is to simplify the evaluation process of these eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The development board is 2" x 2" and contains two eGaN FETs in a half-bridge configuration using the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance and has additional area to add buck output filter components on the board. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in figure 1.

For more information on the EPC2030 and EPC2031 eGaN FETs, please refer to the datasheets available from EPC at [www.epc-co.com](http://www.epc-co.com). The datasheet should be read in conjunction with this quick start guide.

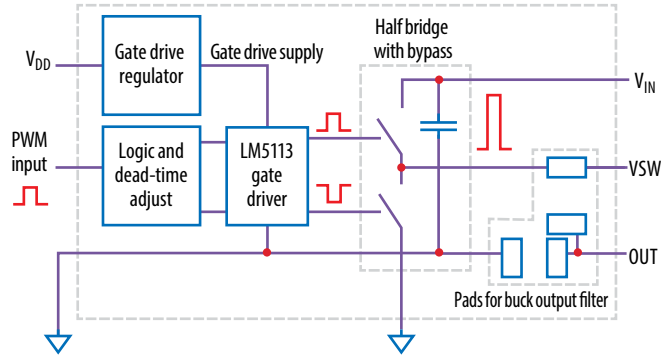


Figure 1: Block Diagram of Development Board

Table 1: Performance Summary (T<sub>A</sub> = 25 °C) EPC9060/61

Symbol	Parameter	Conditions	Min	Max	Units
V <sub>DD</sub>	Gate Drive Input Supply Range		7	12	V
V <sub>IN</sub>	Bus Input Voltage Range	When using 40 V devices, EPC9060		32 <sup>(1)</sup>	V
		When using 60 V devices, EPC9061		48 <sup>(1)</sup>	V
V <sub>OUT</sub>	Switch Node Output Voltage	When using 40 V devices, EPC9060		40	V
		When using 60 V devices, EPC9061		60	V
I <sub>OUT</sub>	Switch Node Output Current	When using 40 V devices, EPC9060		25 <sup>(1)</sup>	A
		When using 60 V devices, EPC9061		24 <sup>(1)</sup>	A
V <sub>PWM</sub>	PWM Logic Input Voltage Threshold	Input 'Low'	3.5	6	V
		Input 'High'	0	1.5	V
	Minimum "High" State Input Pulse Width	V <sub>PWM</sub> rise and fall time < 10ns	50		ns
	Minimum "Low" State Input Pulse Width	V <sub>PWM</sub> rise and fall time < 10ns	100 <sup>(2)</sup>		ns

(1) Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermal cooling.

(2) Limited by time needed to 'refresh' high side bootstrap supply voltage.

**QUICK START PROCEDURE**

The development boards are easy to set up to evaluate the performance of the eGaN FET. Refer to figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to  $+V_{IN}$  (J5, J6) and ground / return to  $-V_{IN}$  (J7, J8).
2. With power off, connect the switch node of the half-bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to  $+V_{DD}$  (J1, Pin-1) and ground return to  $-V_{DD}$  (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on  $V_{OUT}$  as indicated in the table below:
  - a. EPC9060, 40 V
  - b. EPC9061, 60 V
7. Turn on the controller / PWM input source and probe switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See figure 3 for proper scope probe technique.

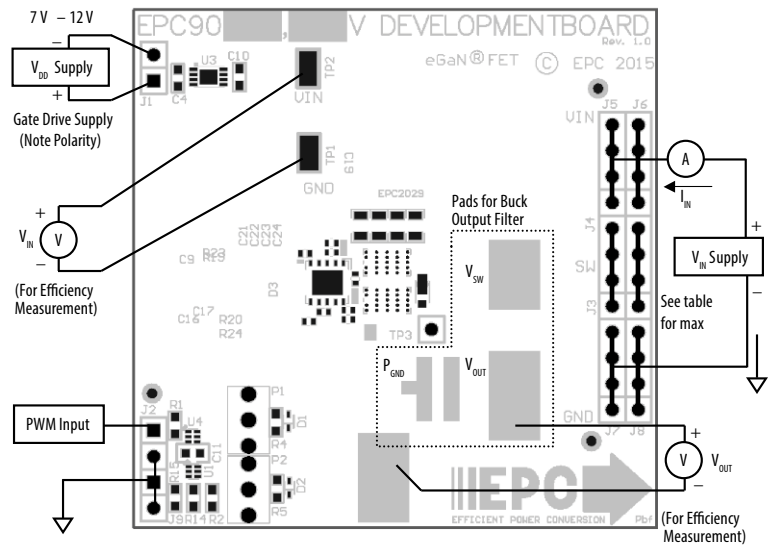


Figure 2: Proper Connection and Measurement Setup

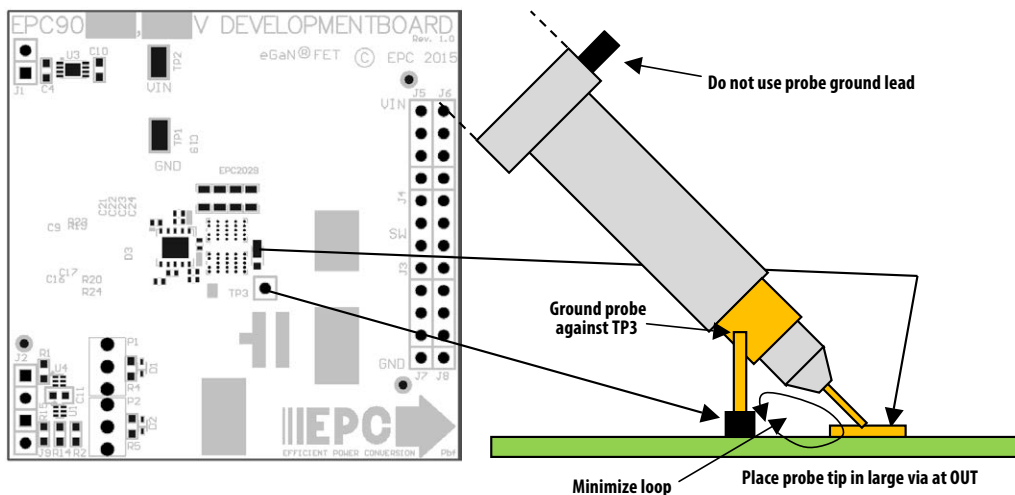


Figure 3: Proper Measurement of Switch Node – OUT

## THERMAL CONSIDERATIONS

The EPC9060/61 development boards showcase the EPC2030/31 eGaN FETs. Although the electrical performance surpasses that for traditional Silicon devices, their relatively smaller size does magnify the thermal management requirements. These development boards are intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling

can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE: The EPC9060/61 development boards do not have any current or thermal protection on board.

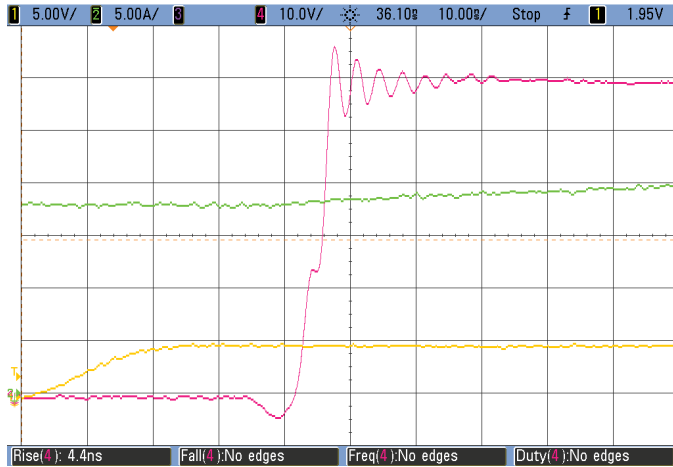


Figure 4 (a) – Rising Edge

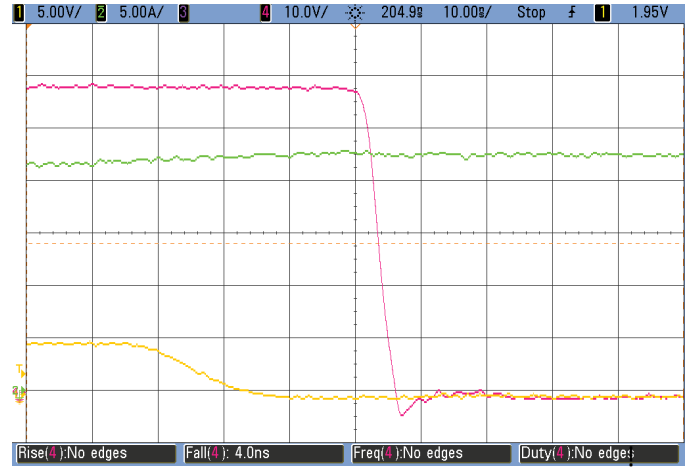


Figure 4 (b) – Falling Edge

Typical Waveforms for  $V_{in} = 60\text{ V}$  to  $5\text{ V}/20\text{ A}$  (300 kHz) Buck converter CH1: ( $V_{PWM}$ ) Input logic signal – CH2: ( $I_{OUT}$ ) Output inductor current – CH4: ( $V_{OUT}$ ) Switch node voltage

**Table 2 : Bill of Material**

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	3	C4, C10, C11	Capacitor, 1 $\mu$ F, 10%, 25 V, X5R	Murata	GRM188R61E105KA12D
2	2	C16, C17	Capacitor, 100 pF, 5%, 50 V, NP0	Kemet	C0402C101K5GACTU
3	1	C9	Capacitor, 0.1 $\mu$ F, 10%, 25 V, X5R	TDK	C1005X5R1E104K
4	1	C19	Capacitor, 1 $\mu$ F, 10%, 25 V, X5R		C1005X5R1E105K
5	4	C21, C22, C23, C24	Capacitor, - see Table 3		See Table 3
6	2	D1, D2	Schottky Diode, 30 V	Diodes Inc.	SDM03U40-7
7	3	J1, J2, J9	Connector	FCI	68001-236HLF
8	1	J3, J4, J5, J6, J7, J8	Connector	FCI	68602-224HLF
9	2	Q1, Q2	eGaN <sup>®</sup> FET - see Table 3		See Table 3
10	1	R1	Resistor, 10.0 k, 5%, 1/10 W	Panasonic	ERJ-3GEY0R00V
11	2	R2, R15	Resistor, 0 $\Omega$ , 1/8 W	Stackpole	RMCF0603ZT0R00
12	1	R4	Resistor, 47 $\Omega$ , 1%, 1/10 W	Stackpole	RMFC0603FT47R0
13	1	R5	Resistor, 75 $\Omega$ , 1%, 1.10 W	Stackpole	RMCF0603FT75R0
14	4	R19, R20, R23, R24	Resistor, 0 $\Omega$ , 1/16 W	Stackpole	RMCF0402ZT0R00
15	2	TP1, TP2	Test Point	Keystone Elect	5015
16	1	TP3	Connector	1/40th of Tyco	4-103185-0
17	1	U1	I.C., Logic	Fairchild	NC7SZ00L6X
18	1	U2	I.C., Gate Driver	National	LM5113
19	1	U3	I.C., Regulator	Microchip	MCP1703T-5002E/MC
20	1	U4	I.C., Logic	Fairchild	NC7SZ08L6X
21	0	R14	Optional Resistor		
22	0	D3	Optional Diode		
23	0	P1, P2	Optional Potentiometer		

**Table 3 : Variable BOM Components**

Board Number	Item	Qty	Reference	Part Description	Manufacturer	Part Number
EPC9060	5	4	C21, C22, C23, C24	Capacitor, 4.7 $\mu$ F, 50 V $\pm$ 10%, X5R	TDK	C2012X5R1H475K125AB
	9	2	Q1, Q2	eGaN <sup>®</sup> FET	EPC	EPC2030
EPC9061	5	4	C21, C22, C23, C24	Capacitor, 1 $\mu$ F, 100 V $\pm$ 10%, X7S	TDK	CGA4J3X7S2A105K125AE
	9	2	Q1, Q2	eGaN <sup>®</sup> FET	EPC	EPC2031

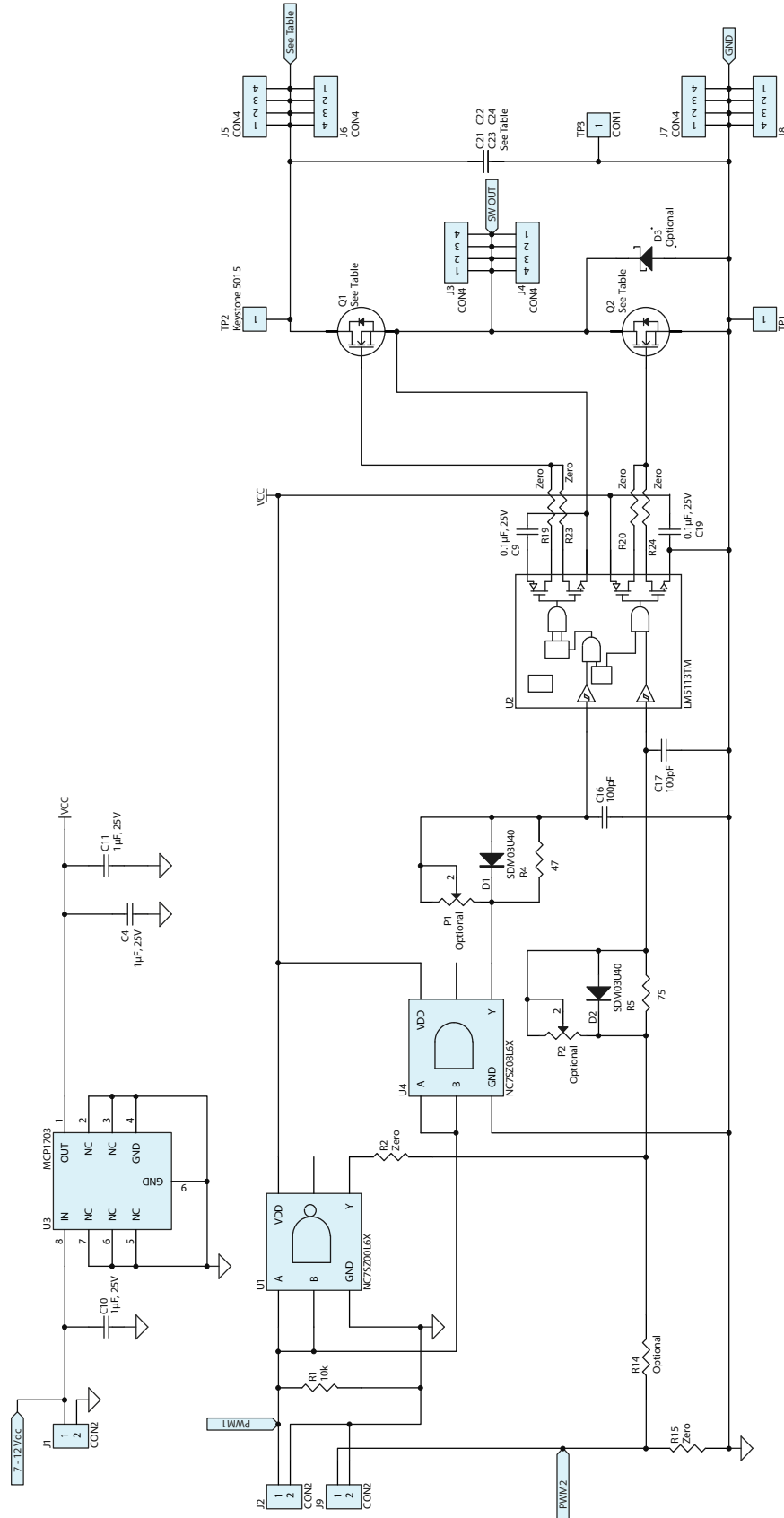


Figure 5: Development Board Schematic

## For More Information:

Please contact [info@epc-co.com](mailto:info@epc-co.com)  
or your local sales representative

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### Demonstration Board Notification

**The EPC9060/61 board is intended for product evaluation purposes only. It is not intended for commercial use nor is it FCC approved for resale.** Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions. This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

As an evaluation tool, this board is not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant.

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