Development Board EPC9098 Quick Start Guide

170 V Half-bridge with Gate Drive, Using EPC2059

Revision 2.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9098 development board is a 170 V maximum device voltage, 17 A maximum output current, half bridge with onboard gate drives, featuring the EPC2059 GaN field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2059 by including all the critical components on a single board that can be easily connected into many existing converter topologies.

The EPC9098 development board measures 2" x 2" and contains two EPC2059 GaN FETs in a half bridge configuration with the Texas Instruments LMG1210 gate driver. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on EPC2059 please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC9098

Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Input Supply Range		7.5		12	V
V_{IN}	Bus Input Voltage Range(1)				135	V
I_{OUT}	Switch Node Output Current (2)				17	A
V_{SW}	Switch Node Voltage				170	V
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'Low'	0		1.5	V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	Minimum 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10ns	200			ns

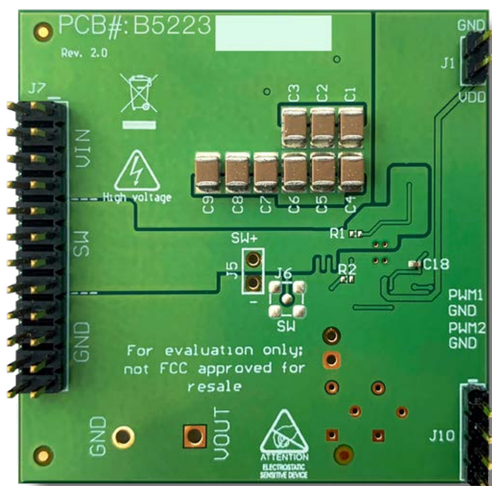
(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 170 V for EPC2059.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the LMG1210 datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.

Front view



Back view

EPC9098 development board

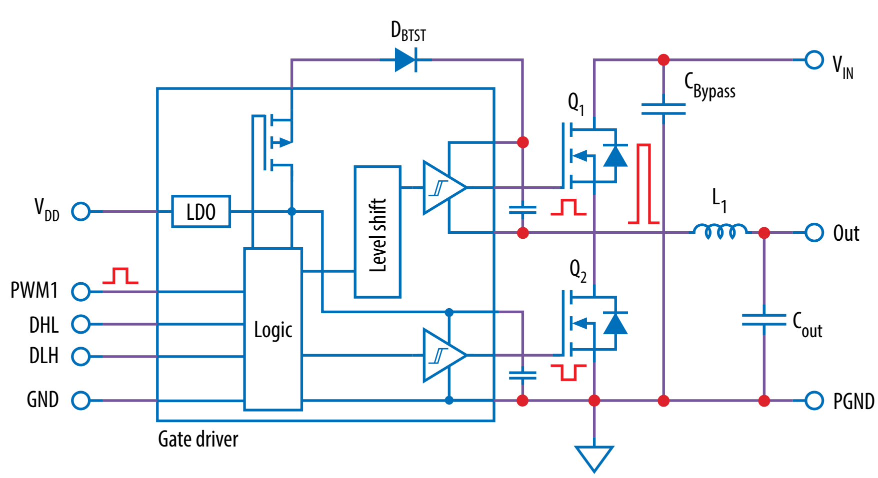


Figure 1: Block diagram of EPC9098 development board

QUICK START PROCEDURE

The EPC9098 development board is easy to set up as a buck or boost converter to evaluate the performance of two EPC2059 eGaN FETs. It can operate in single PWM mode with on board dead time, defined as the delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. The EPC9098 board can also operate in dual PWM input mode.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM with preset dead time of 10 ns for the FETs as shown in figure 3(a). This is the default configuration. Refer to the LMG1210 datasheet for details on how to adjust the dead time setting using P1 and P2 or R14 and R15.

To select dual input mode, the zero-ohm resistor in position R5 needs to be removed and a zero-ohm resistor must be installed in position R6 as shown in figure 3(b).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM input can be chosen. Figure 3(a) shows the connection setup for single PWM input mode and figure 3(b) for the dual PWM input mode.

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in dual PWM input mode and not making use of the gate driver dead time function.

Once the input source and dead-time settings have been chosen and set, then the board can be operated.

1. With power off, connect the input power supply bus to VIN and ground/return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 3.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J10 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

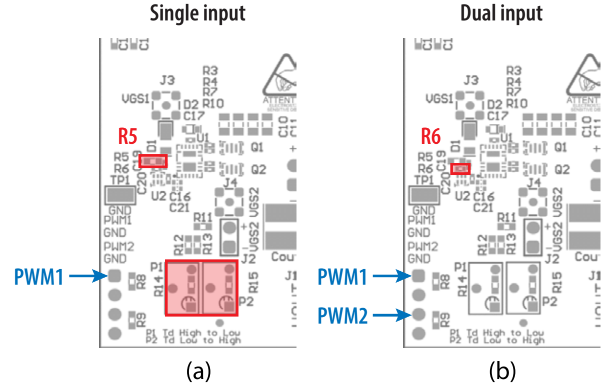


Figure 2: Input mode selection

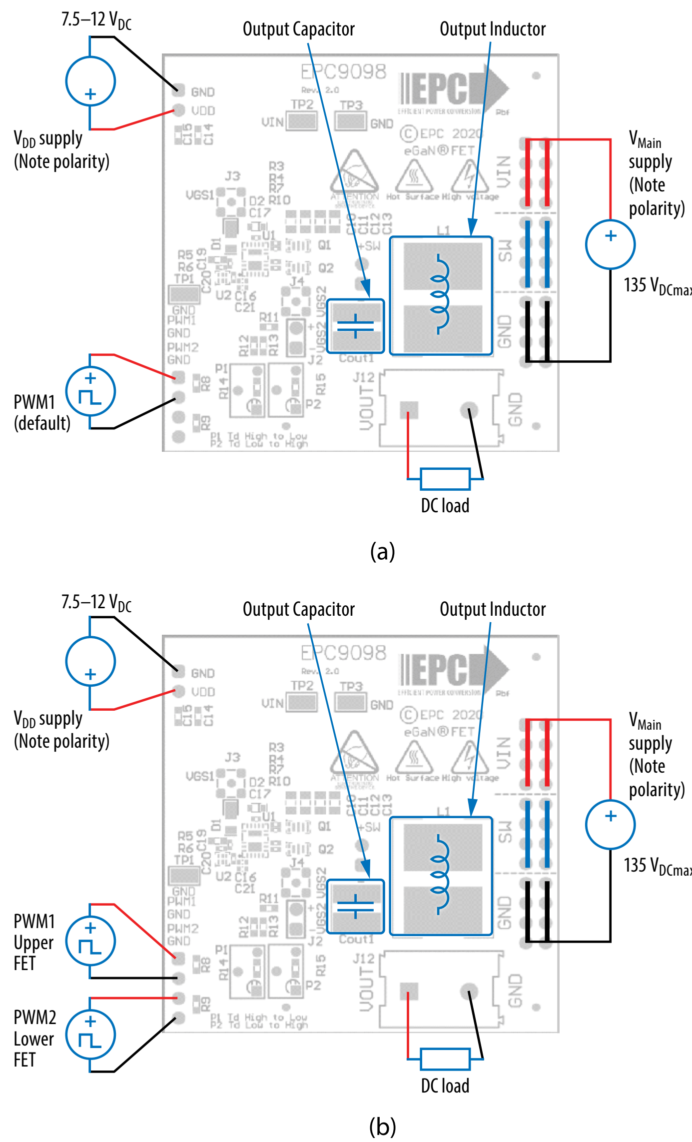


Figure 3: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, output capacitor, inductor, PWM, and load connections.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM input can be chosen. Figure 4(a) shows the connection setup for single PWM input mode and figure 4(b) for the dual PWM input mode. ***Note that in boost mode, the PWM polarity is inverted.***

Notes: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in dual PWM input mode and not making use of the gate driver dead time function.

Once the input source and dead-time settings have been chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 4, or provided off board.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (labeled as VIN) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to V_{DD} (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J10 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the output is not open circuit, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

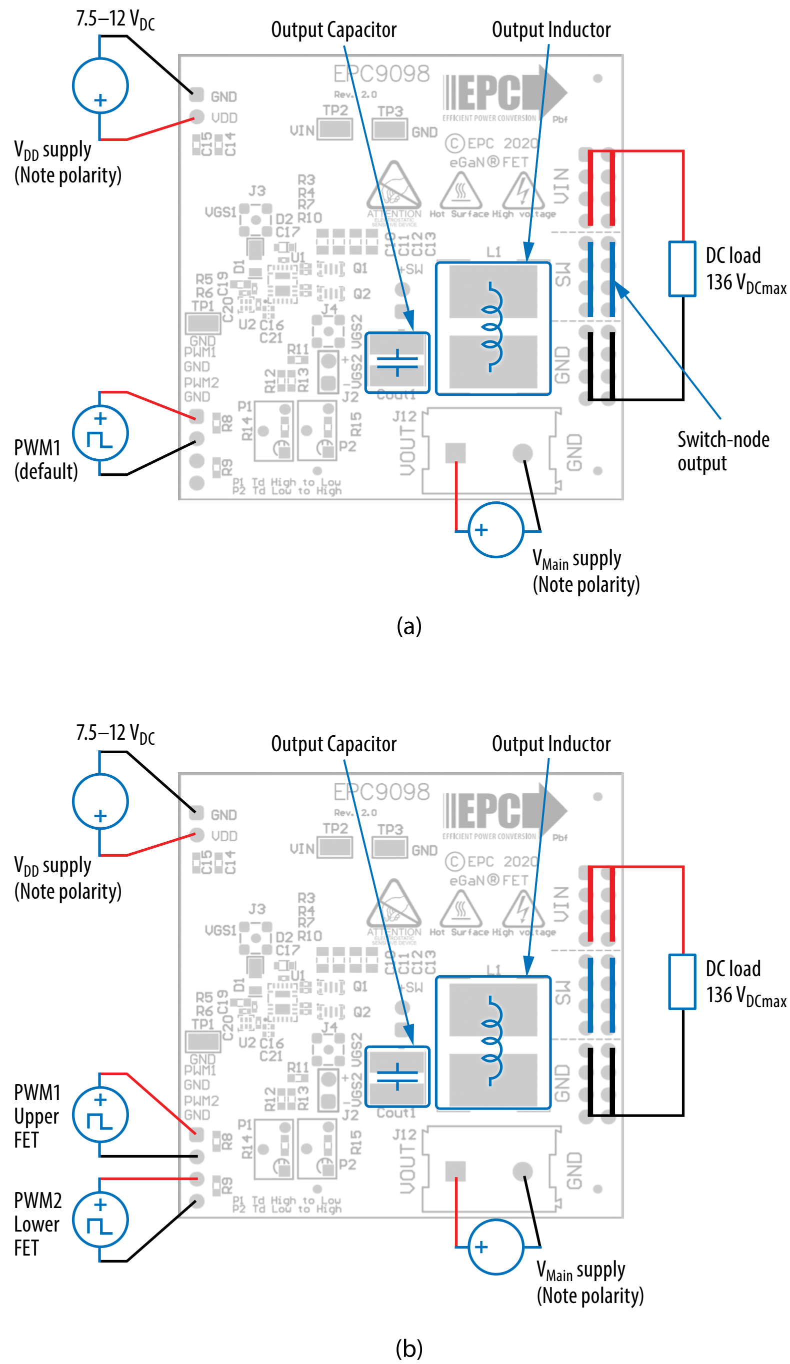


Figure 4: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, output capacitor, PWM, and load connections.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 5. Figure 6 shows an actual switch-node voltage measurement when operating the board as a buck converter.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J5) and an MMCX connector (J6) are provided for switch-node measurement.

A differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix has a mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

NOTE. For information about measurement techniques, the EPC website offers: "**AN023 Accurately Measuring High Speed GaN Transistors**" and the How to GaN educational video series, including: **HTG09- Measurement**

THERMAL CONSIDERATIONS

The EPC9098 development board showcases the EPC2059 eGaN FET. The EPC9098 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE. The EPC9098 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult: D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

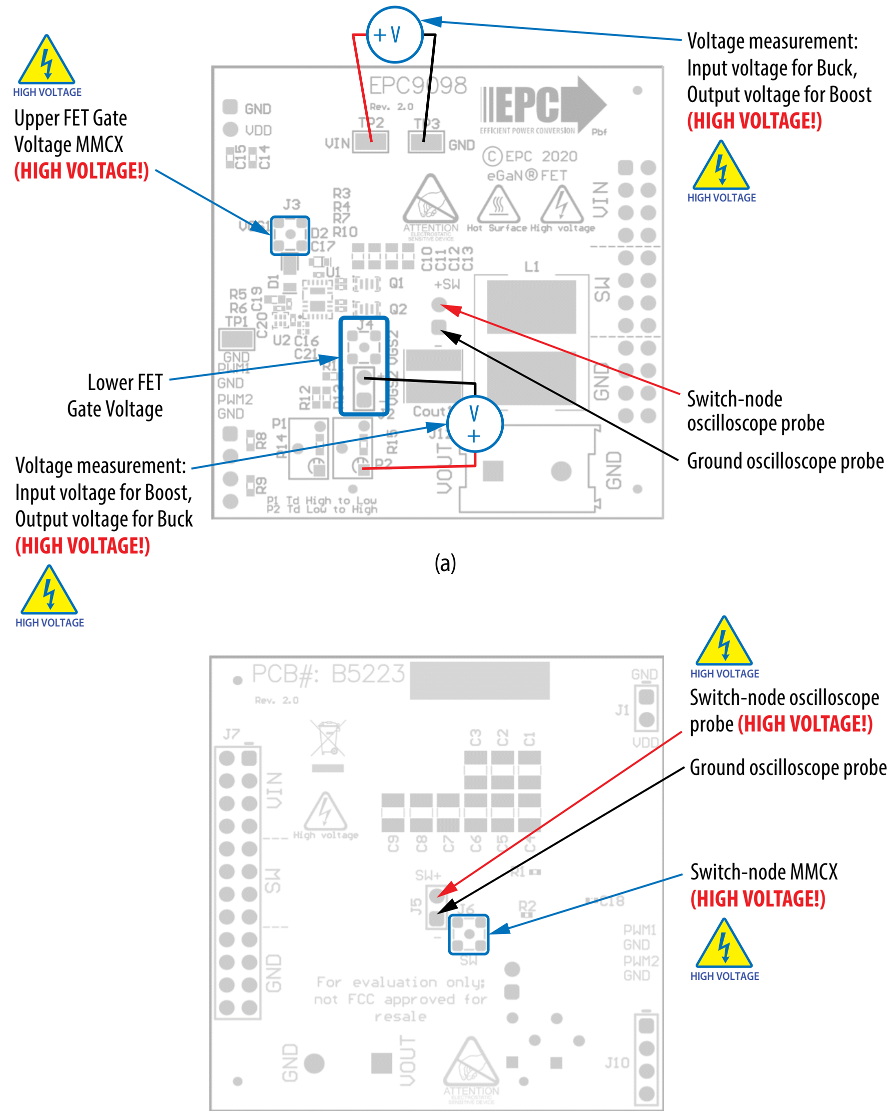
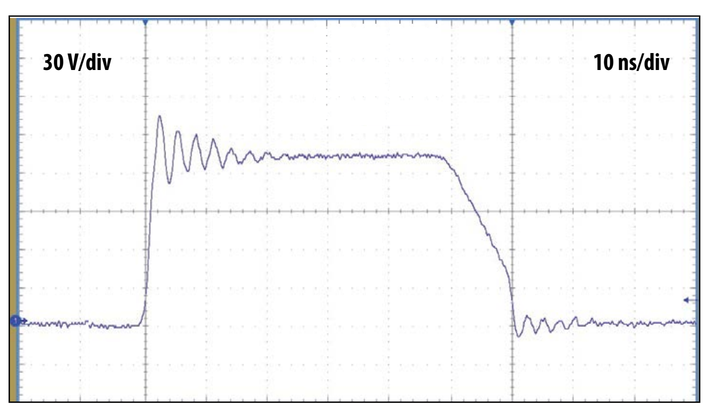


Figure 5 Measurement points (a) front side, (b) Back side



V_{IN} = 135 V, V_{OUT} = 12 V, I_{OUT} = 5 A, f_{sw} = 200 kHz, L = 30 µH

Figure 6: Typical switch-node waveform when operated as a buck converter

Table 2: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	9	C1, C2, C3, C4, C5, C6, C7, C8, C9	Capacitor, 0.33 µf, 10%, 250 V, X7T	TDK	CGA6M3X7T2E334K200AA
2	4	C10, C11, C12, C13	Capacitor, 0.1 µf, 10%, 250 V, X7T	TDK	CGA4J3X7T2E104K125AA
3	1	C14	Capacitor, 1 µf, 10%, 25 V, X7R	TDK	C1608X7R1E105K
4	1	C15	Capacitor, 4.7 µf, 10%, 25 V, X5R	TDK	C1608X5R1E475K080AC
5	2	C16, C21	Capacitor, 2.2 µf, 10%, 16 V, X5R	TDK	C1005X5R1C225K050BC
6	1	C17	Capacitor, 0.47 µf, 10%, 25 V, X5R	TDK	C1005X5R1E474K050BB
7	1	C18	Capacitor, 0.22 µf, 10%, 16 V, X7R	TDK	C1005X7R1C224K050BC
8	2	C19, C20	Capacitor, 10 pf, 10%, 25 V, C0G/NP0	Murata	GRM1555C1E100JA01D
9	1	D1	Diode Super Barrier, 200 V, 1A	Diodes	SBR1U200P1Q
10	1	D2	Zener Diode, 5.61 V, 500 mW	On Semiconductor	MM5Z5V6ST1G
11	1	J1	Connector, .1" Male Vert	Tyco	4-103185-0-02
12	1	J7	Connector, .1" Male Vert	Tyco	4-103185-0-04
13	1	J10	Connector, .1" Male Vert	Tyco	4-103185-0-04
14	2	Q1, Q2	eGaN FET, 170 V, 9 mΩ	EPC	EPC2059
15	4	R3, R4, R7, R10	Resistor, 4.7 Ω, 5%, 1/10 W, 0402	Panasonic	ERJ-2GEJ4R7X
16	1	R5	Resistor, 10 kΩ, 5%, 1/10 W, 0603	Stackpole	RMCF0603JT10K0
17	2	R8, R9	Resistor, 10 kΩ, 5%, 1/10 W, 0603	Yageo	RC0603JR-0710KL
18	1	R11	Resistor, 0 Ω jumper, 1/10 W, 0603	Stackpole	RMCF0603ZT0R00
19	2	R12, R13	Resistor, 20 kΩ, 5%, 1/10 W, 0604	Stackpole	RNCF0603BTE20K0
20	2	R14, R15	30 kΩ 1% 1/10 W	Panasonic	ERJ-3EKF3002V
21	3	TP1, TP2, TP3	Test point, miniature SMT	Keystone	5015
22	1	U1	200 V HB Gate Driver	Texas Instruments	LMG1210
23	1	U2	IC BUFF NONINVERT 5.5 V 6MICROPAK	Fairchild	NC7WZ16L6X

Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	1	Cout1	TBD	Generic	Generic
2	3	J3, J4, J6	MMCX Connector Jack	Molex	734152063
3	1	J12	7.62 mm Euro Term.	Würth	691216410002
4	1	L1	TBD	Generic	Generic
5	2	P1, P2	Potentiometer, 1 MΩ, through-hole, for dead time adjustment	Murata	PV37W105C01B00
6	3	R1, R2, R6	Resistor, 0 Ω jumper, 1/16 W, 0402	Stackpole	RMCF0402ZT0R00

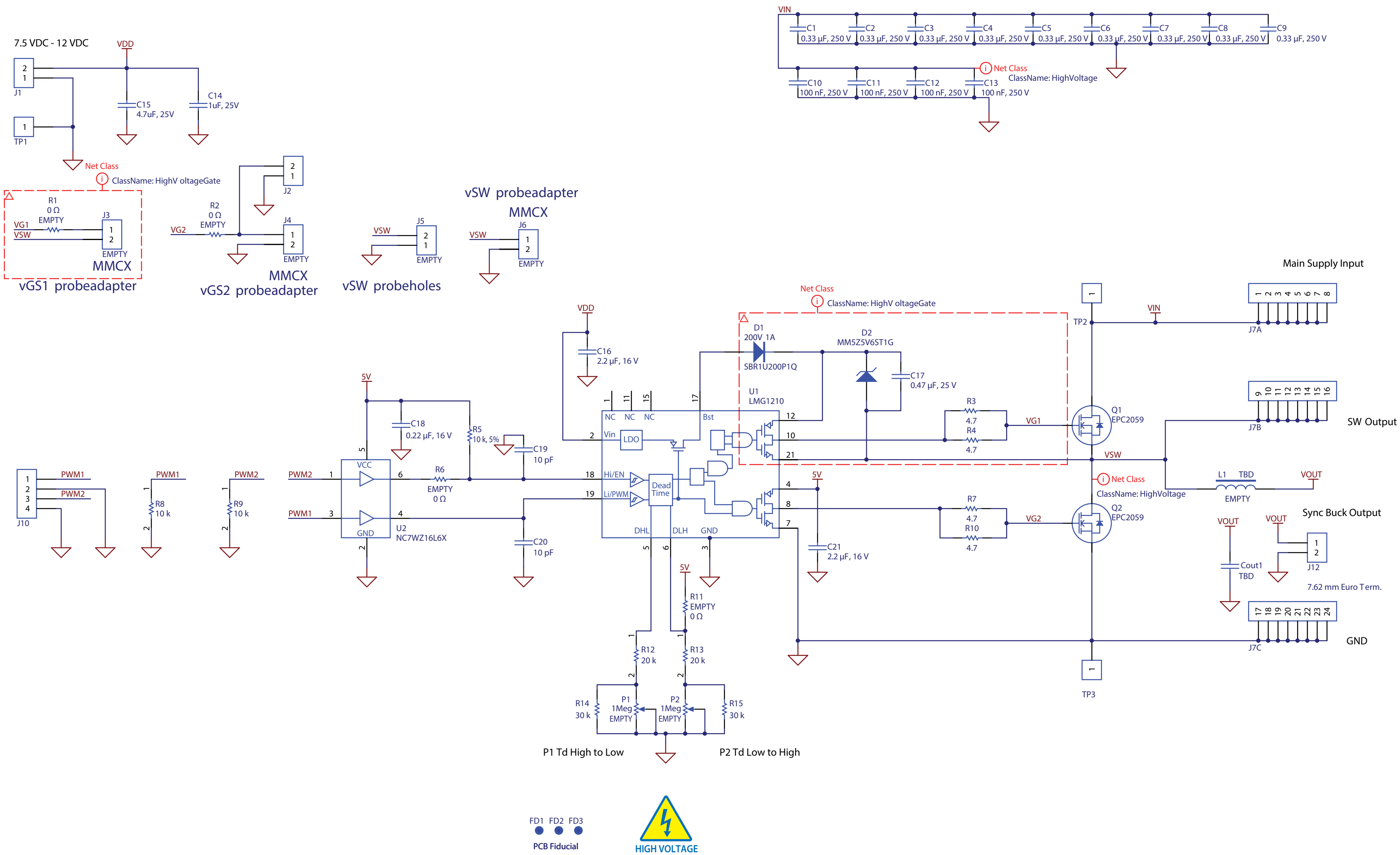


Figure 7: EPC9098 main schematic

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EFFICIENT POWER CONVERSION

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