Development Board EPC9172 Quick Start Guide

EPC21701

80 V, 15 A High Current Pulsed Laser Diode Driver

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9172 development board is primarily intended to drive laser diodes with short, high current pulses. Capabilities include minimum pulse widths of < 2.5 ns, peak currents > 15 A, and bus voltage rating of 60 V. The board is shipped with an EPC21701 eToF™ Laser Driver IC. The EPC21701 monolithically integrates an ultrafast eGaN gate driver with and a 15 A, 80 V eGaN FET in one tiny 6-terminal LGA IC. The EPC9172 ships with the EPC9989 interposer board. The EPC9989 is a collection of break-away 5 x 5 mm square interposer PCBs with footprints for different lasers, RF connectors, and a collection of other footprints designed for experimentation with different loads. The use of the interposers allows many different lasers or other loads to be mounted on the EPC9172. Laser diodes or other loads are not included, and must be supplied by the user.

The EPC9172 combines the EPC21701 eGaN IC with a printed circuit board with inputs, outputs, and test points in order to evaluate and demonstrate the capabilities of the IC and connected load. The printed circuit board is designed to minimize the power loop inductance while maintaining mounting flexibility for the laser diode or other load. It includes multiple on-board passive probes for voltages and is equipped with MMCX connections for input and sensing. The EPC21701 IC requires a 5 V_{DD} supply, but is designed to interface with 3.3 V and 5 V CMOS logic families. In many cases it can also be driven from 2.5 V logic families. Finally, the board can also be used for other applications requiring a ground-referenced eGaN IC, e.g. Class E amplifiers, boost converters, or similar. A complete block diagram of the circuit is given in Figure 1, and a detailed schematic in Figure 6.

For more information on the EPC21701 eGaN IC, please refer to the datasheet available from EPC at **www.epc-co.com**. The datasheet should be read in conjunction with this quick start guide.

SETUP AND OPERATION

Development board EPC9172 is easy to set up to evaluate the performance of the EPC21701 eGaN IC. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. Review laser safety considerations. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Refer to qualified safety personnel as necessary.
2. With power off, install laser diode U2 or other load. The use of one of the interposers from the included EPC9989 may be used to mount the laser or other load, and this is discussed in the section **LASER DIODE AND LOAD CONSIDERATIONS** for further information.
3. With power off, connect the input power supply bus to +V_{BUS} (J1) and ground / return to –V_{BUS} (J9) or GND.
4. With power off, connect the logic supply (5.1 V_{DC}) to +V_{Logic} (J9) and ground return to –V_{Logic} (J9) or GND.
5. With power off, connect the signal pulse generator to the input J3. J3 is terminated with 50 Ω at the input of the EPC21701 IC (U1), and can accommodate 3.3 V and 5 V CMOS logic inputs. This range may be extended in some cases, as discussed in this guide.
6. Connect the remaining measurement MMCX outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section **MEASUREMENT CONSIDERATIONS** for more information, including the attenuation values for each output. ***Note that the current sensing output is not functional for this board revision.***
7. Turn on the logic supply voltage to a value within the specification.
8. Turn on the bus voltage to a value within the specification.

Table 1: Performance Summary (T_A = 25°C) EPC9172

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{Logic}	Gate drive and logic supply		5.5		12	V
V_{BUS}	Bus input voltage range		0		60*	
I_{LOAD}	Output load current				15**	A
Z_{IN}	Input impedance	J3 input		50		Ω
V_{INPUT}	Input pulse range		0		5	V
F_{INPUT}	Input pulse frequency		0	50	100***	MHz
T_{Pin}	Input pulse width		2		1000	ns

* The voltage rating of the EPC21701 eGaN IC is 80 V. The extremely fast switching transitions may result in ringing. It is the responsibility of the user to ensure that the peak voltage does not exceed the rating.

** This is the EPC21701 rating, and does not account for heat generated by the load. It is the responsibility of the user to ensure that operating temperatures are within component specifications.

*** The EPC21701 is specified to have a 100 MHz maximum operating frequency, but in many cases can operate at a higher frequency.

SAFETY WARNING: This board is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

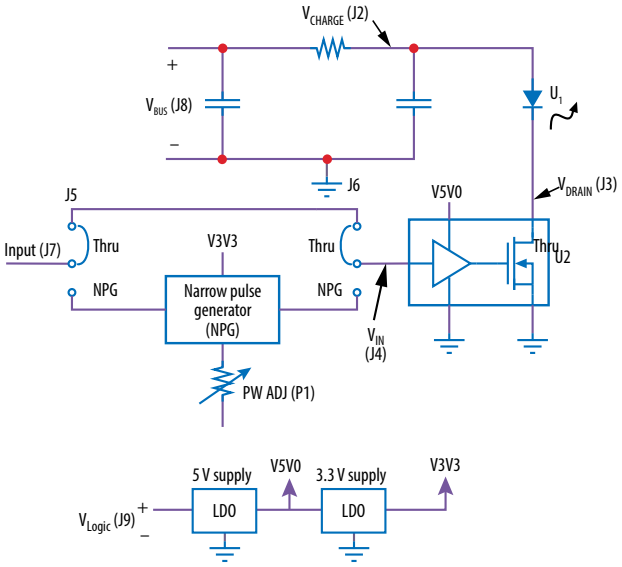

Figure 1: Block diagram of EPC9172 development board

9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate electro-optical receiver.
10. Once operational, adjust the bus voltage, input pulse width, and pulse repetition frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

NOTE: This circuit contains nodes with very fast edges and with voltages one or two orders of magnitude higher that standard logic signals. Standard methods and probes for power circuits will normally not provide accurate results and may disrupt circuit operation. Please consider probe choice and use carefully. See EPC measurement applications note.

OPERATING PRINCIPLE

The EPC9172 is intended as both a demonstration board and a flexible development platform. It is functional out of the box, but is designed to be modified to accommodate a broad range of applications. ***It is highly recommended that the user read the entire guide in order to get maximum value from the EPC9172. Note that there are significant feature differences between Rev. 1 and Rev. 2 PCB. Be sure to consult the correct guide for the board version of interest.***

The EPC9172 is shipped as a rectangular pulse laser diode driver. Please refer to the block diagram (Fig. 1) and the schematic (Fig. 6). The EPC9172 basic operating principle is to act as a switch to allow current from the voltage bus to flow through the laser diode or other load when the IC U2 is commanded on, and stop the load current when the IC is commanded off. The speed of the transitions are affected by the load, but are extremely fast. For example, turn-on and turn-off can be faster than 500 ps and 250 ps,

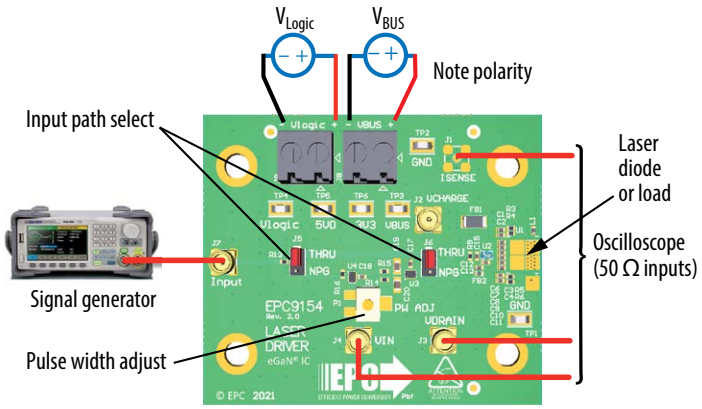

Figure 2: Connection and measurement setup

respectively, for a load current of 10 A.

The IC U2 is controlled via an input pulse that is delivered to MMCX connector J3, which is terminated on the demo board with 50 Ω at the input pin of U2. The EPC21701 is nominally designed for 3.3 V and 5 V CMOS logic levels, but will operate with many 2.5 V CMOS logic devices. When the input goes high, the gate driver stage of U2 turns on the output stage, allowing current flow through the laser diode or load.

The IC U2 is controlled via an input pulse that is delivered to MMCX connector J7. The input can either be directed straight to U2, or through a Narrow Pulse Generator (NPG). In either case, the input impedance at J7 is approximately 50 Ω. When using the THRU path, one has access to the input pin of the EPC21701 in order to evaluate the performance directly. The EPC21701 is nominally designed for 3.3 V and 5 V CMOS logic levels, but will operate with many 2.5 V CMOS logic devices and with some 1.8 V logic. The NPG is provided for the convenience of the user, and allows one to generate extremely short pulses of adjustable width. The details are given in the section OPERATING PRINCIPLES. In either case, when the input goes high, the gate driver stage of U2 turns on the output stage, allowing current flow through the laser diode or load. If the NPG is used, the output stage of U2 is turned off after an adjustable delay time provided that the input pulse is at least 5 ns longer than the pulse width set in the NPG. If the THRU mode is used, the output of U2 is turned off when the input goes low.

The voltage bus for the laser diode or other load is bypassed via the capacitor bank {C6, C7, C8, C9, C10, C11}. This capacitor bank is part of the main power loop inductance, and the layout is designed to minimize the effect of resulting parasitic inductance. The capacitor bank is fed through a relatively small resistance formed by {R3, R4, R5, R6}. The resistance serves to limit the laser or load current continuous value in the case of long pulses, and also serves to damp parasitic resonance of the power loop. The bus is further filtered via capacitors and a ferrite bead to minimize any transients appearing at the V_{BUS} (J8) input.

Measurements of key waveforms can be made through the MMCX test points provided. These test points can provide waveform measurements with equivalent bandwidths > 3 GHz. However, they have requirements and properties that differ from most conventional oscilloscope probes. More details on the usage of these test points is provided in section **MEASUREMENT CONSIDERATIONS**.

OPERATING CONSIDERATIONS

The EPC21701 is specifically designed for high speed, short pulse operation while minimizing the number of external parts required. As a result, there are some additional items and limitations that should be observed. These are discussed below.

Low V_{BUS} operation

The first consideration is that when the IC is operated with V_{BUS} < 10 V, the output may miss the one or more of first few pulses of a burst, or the first few pulses may be distorted. In many applications, this may be acceptable, and in such cases, the IC will function with V_{BUS} all the way to 0 V.

Long pulse widths

The second consideration is that the IC is designed for short pulses. It is recommended that the maximum on-time not exceed 1000 ns. Longer pulses are possible, but the output specifications are not guaranteed under such conditions.

Pulse sources

The EPC9172 has the option of driving the EPC21701 directly (THRU) or through a pulse shortening circuit called the Narrow Pulse Generator (NPG). The mode is selected via jumpers J5 and J6 as discussed earlier.

The direct (THRU) mode is provided so that the end user can evaluate how their circuit will operate with the EPC21701. The EPC21701 supports 3.3 V and 5 V CMOS logic levels, and with many CMOS devices, it will operate with 2.5 V logic levels. However, some logic gates may struggle to drive the 50 Ω input of the EPC9172 demo board. If one wishes to drive the board directly from lower voltage logic, one may need to increase the value of the 50 Ω resistor R9 and possibly use a series termination at the driving gate to prevent ringing on the line. These techniques are covered in many sources. For more information, a highly recommended reference is *High-Speed Digital Design – A Handbook of Black Magic by Johnson and Graham* [1].

The EPC21701 is intended for high speed operation, hence when using the THRU mode, it is recommended that the input signal has fast transitions. While the command input has hysteresis, it is recommended that the signal input waveform has edge transition times < 5 ns . The EPC21701 will operate with longer input transitions, but becomes more sensitive to noise at the input.

[1] Howard Johnson and Martin Graham, High Speed Digital Design: A Handbook of Black Magic, 1st Edition. Prentice Hall, Inc., 1993.

Narrow Pulse Generator (NPG)

The narrow pulse generator is provided as a convenience to the user. It allows the user to provide a short input pulse to the EPC21701 that is triggered by a longer input pulse at J7. When using the NPG, one needs to provide an input pulse suitable for 3.3 V CMOS logic, of pulse length at least 5 ns longer than the desired input to the EPC21701. The pulse length is adjustable using P1 (see Fig. 2), where CW rotation increases pulse width.

The NPG provides a range of pulse widths of approximately 1.5 to 65 ns as shipped, provided the input pulse is at least 5 ns longer than the desired NPG output pulse. The additional propagation delay of the NPG is approximately 5 to 6 ns. If precise adjustments are required, it is recommended to use a non-conductive adjustment tool, since even a small amount of extra capacitance can affect the pulse width. In addition, P1 limits the resolution of the pulse width adjustment, and this is noticeable for very short pulses. If finer adjustment is required for short pulses, it is recommended that P1 be replaced with a lower valued potentiometer from the same component series.

The NPG is provided as a convenience to the end user and as an example of a low-cost means of generating very short pulses. It is not fully characterized over standard operating ranges.

Clamping diodes

The EPC9172 is a dual edge control driver. When the IC U2 is turned off, energy stored in the stray power loop inductance can cause a U2 output voltage spike that may exceed the device ratings. In order to reduce the voltage spike, a diode-connected EPC2036 eGaN FET (Q1) can be added to help clamp the drain node. There are also provisions for up to two other clamping diodes D1 and D2. While diodes Q1, D1 and D2 can provide some protection to IC U2 and laser U1, they have parasitic inductance and capacitance that can reduce performance and add additional ringing at the very fastest speeds. Hence, they are not populated, and it is left to the user to determine whether they are beneficial for any particular application. D1, D2, and Q2 locations are on the bottom side of the EPC9172 PCB. D3 and D4 are high-speed silicon transient voltage suppressors that only act to clamp spikes above 36 V.

LASER DIODE OR LOAD CONSIDERATIONS

The EPC9172 can be used as is to mount a laser diode or other load. Figure 3 highlights the output pad locations. However, many laser suppliers have different mounting footprints, making it difficult to optimize the performance of the driver and still maintain the desired flexibility. The use of an interposer PCB provides a solution to this problem with a small added performance penalty in the form of an additional 50 pH to 100 pH power loop inductance. The EPC9172 ships with the EPC9989 interposer PCB, shown in Figure. 4. The EPC9989 has an assortment of 5 mm square interposer PCBs that can be snapped off the board. These interposers have various footprints on the top side that can accommodate several surface mount laser diodes, an MMCX connector, and several patterns designed to accommodate a wide variety of possible loads. These interposers mount between the EPC9172 and the laser diode or other load. The EPC9989 is updated as new lasers or loads become available, so Figure 4 may not show the latest board. Figure 5 shows an example of an Excelitas SMD laser diode mounted with one of the interposers.

Finally, a ground pad is made available for those who wish to use the board for alternative applications.

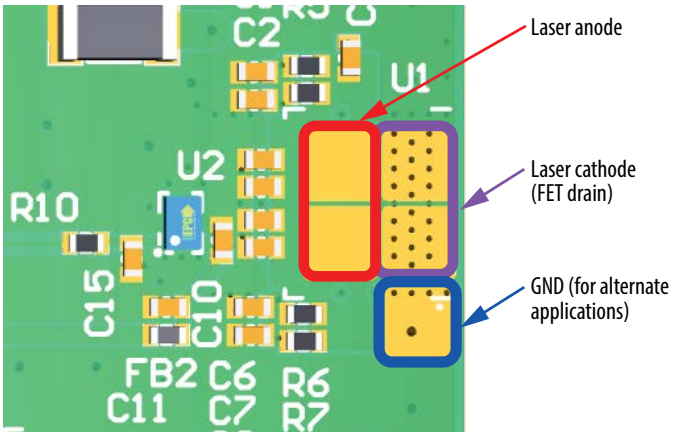

Figure 3: Output terminals of the EPC9172

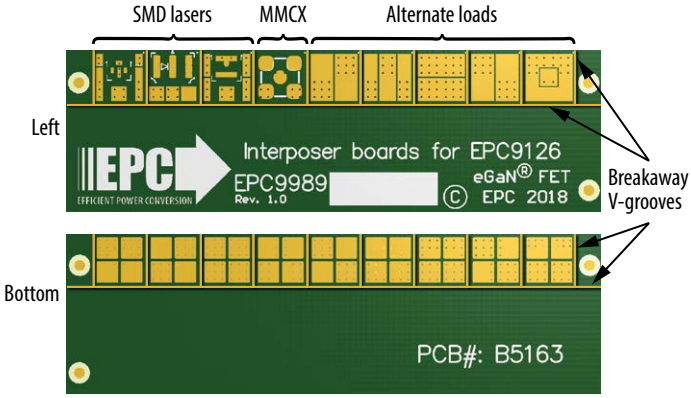

Figure 4: EPC9989 interposer. Note that this board is revised as needed to accommodate new lasers and other loads as needed, so the picture may not show the latest revision.

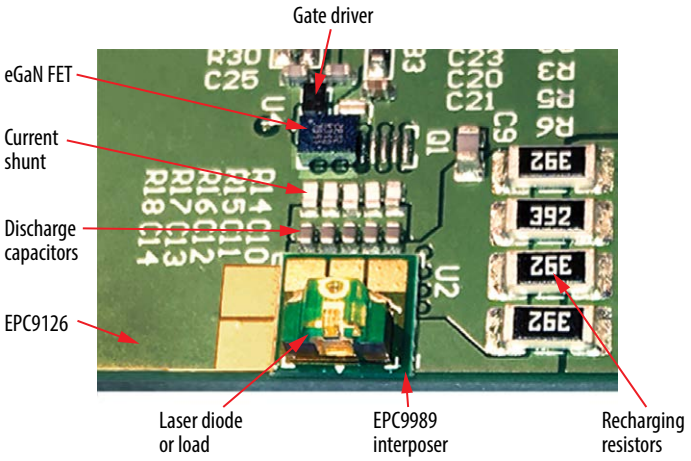

Figure 5:Laser diode mounting on output terminals with interposer. Please note that the photograph is of the EPC9126 demo board, but the same interposers and footprints apply to the EPC9172.

The recommended use of the interposer is the following:

1. Apply solder paste to the U1 pads on the EPC9172 PCB.
2. Apply solder paste to the appropriate pads on the top side of the interposer.
3. Place the desired interposer with the bottom side facing the top side of the EPC9172 on the U2 footprint, making sure the pads on the bottom of the interposer align with the footprint on top of the EPC9172 PCB.
4. Place the laser diode or desired load on the interposer, making sure the pads on the bottom of the laser or load align with the footprint on top of the interposer PCB.
5. Reflow the entire assembly with the recommended temperature profile for the solder used. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. The discharge caps, laser diode or other load, and the eGaN FET must all be mounted in close proximity to each other in order to minimize inductance. As a result, the user must take care not to damage any components when mounting the laser or changing other components in the power loop.

The EPC9172 is capable of driving laser diodes with current pulses can result in peak powers of several tens of watts of optical power. Laser diodes for lidar applications are designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

MEASUREMENT CONSIDERATIONS

MMCX jacks are provided to measure several voltages in the circuit, including EPC21701 IC input (J6) and output (J5) voltages, and the charge voltage of the energy storage cap (J2). All measurement points are designed to be terminated in 50 Ω, hence when viewing waveforms, the oscilloscope inputs should be set to a 50 Ω input. Ideally, unused inputs should be also terminated with a 50 Ω load to prevent the probes from creating additional resonances. The output voltage and the discharge cap sense voltage have on-board terminations to greatly reduce this effect, and in practice, the remaining resonances are small enough to ignore in most applications. It is recommended that the user verify this for their own requirements.

All sense measurement MMCXs, except for the shunt measurement (J1), use the transmission line probe principle to obtain waveform fidelity at sub-ns time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. The impedance of the probes at the measurement node is relatively small (~ 1 kΩ). In order to minimize the effects of the low probe impedance on the operation of the demo board, the output voltage (J5) and capacitor voltage (J2) probes have DC blocking capacitors. As a result, measured pulse waveforms will exhibit droop as pulse widths are increased. The user should keep these factors in mind if accustomed to more conventional oscilloscope probes.

Rev. 2 of the EPC9172 does not include a current shunt, therefor the current shunt output J1 is not used at this time. A future revision may include this functionality.

Table 2 summarizes the properties of the MMCX test points for ease of reference.

Table 2: Key properties of the MMCX test points for ease of reference

Designator	PCB label	Description	Attenuation factor	Internal 50 Ω termination	DC blocking cap
J2	CAP	Bus capacitor voltage (VCHARGE on schematic)	41 V/V	YES	YES
J1	SHUNT	Not used	Not used	Not used	Not used
J5	V_{OUT}	U2 output voltage	41 V/V	YES	YES
J6	V_{IN1}	U2 input voltage	20 V/V	NO	NO

NOTE. The EPC9172 demonstration board does not have any thermal protection on board.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9172 landing page at: https://epc-co.com/epc/Products/Demo-Boards/EPC9172

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