

Evaluation Boards EPC9179, EPC9180, and EPC9181 Quick Start Guide

Using EPC2252, EPC2218A, and EPC2204A

Revision 2.0



DESCRIPTION

The EPC9179, EPC9180, and EPC9181 are a set of evaluation boards primarily intended to drive laser diodes with high current pulses with pulse widths in the single digit nanosecond range, from tens to hundreds of amps. The high performance is enabled by EPC’s gallium nitride enhancement mode (eGaN[®]) FET technology. The boards use the fully automotive qualified [EPC2252](#) (80 V 75 A), [EPC2218A](#) (80 V, 231 A), or [EPC2204A](#) (80 V, 125 A). The boards are accompanied by the EPC9989 interposer board to provide the user with a simple means of mounting a small set of commercially available lasers. The EPC9989 has a collection of breakaway 5 mm square interposer PCBs with footprints for different lasers and various alternative loads. The use of the interposers allows many different lasers or other loads to be mounted on the evaluation boards. **The boards do not include a laser diode or load, which must be supplied by the user.**

All three boards have the same function and operation, differing only in peak current and pulse width. Hence, this Quick Start Guide (QSG) will refer to them collectively by EPC9179/80/81 unless otherwise specified. The key part of the EPC9179/80/81 is the resonant discharge power stage, comprising a ground-referenced eGaN FET driven by a Texas Instruments LMG1020 gate driver. The FET is used to discharge a charged capacitor through the stray inductance of the load. The eGaN FET enables the use of a high charging voltage and can turn on in ~1 ns or less, which allows peak discharge currents to be reached in a few nanoseconds or less. The printed circuit board is designed to minimize the power loop inductance and common source inductance while maintaining mounting flexibility for a laser diode or other load. It includes multiple PCB-integrated high bandwidth passive probes for the simplified measurement of key circuit voltage and current values, and is equipped with SMA connectors to provide a high speed connection to instrumentation. In addition, the user can enable an easily adjustable narrow pulse generator (NPG) capable of sub-nanosecond precision. As shipped, the board is designed to be triggered from 3.3 V logic, but is equipped with both a logic level translator and a differential receiver (LVDS, CML, LVPECL, etc.) which can be modified to accommodate different use cases. Finally, the board can also be used for other applications requiring a ground-referenced eGaN FET with ultrafast switching capability, e.g. Class E amplifiers or similar. In addition, footprints are included on the PCB to simplify the use of some common alternative laser driving techniques. A simplified block diagram of the circuit is given in Figure 1.

Additional information on the EPC9179/80/81 is available from EPC at www.epc-co.com. The full schematics, bill of materials (BOM), and PCB layout files, along with links to information and datasheets on the EPC2252, EPC2218A, and EPC2204A AEC-Q101 automotive qualified eGaN FETs can be found at the following links to the evaluation board product pages: [EPC9179](#), [EPC9180](#), [EPC9181](#). The datasheets and schematics should be read in conjunction with this quick start guide (QSG). In addition, EPC provides an application note: [AN027 eGaN FETs for Lidar – Getting the Most Out of the EPC9126 Laser Driver](#). While the note discusses the EPC9126 laser driver, the methods and analysis are directly applicable to the EPC9179/80/81.

Table 1: Performance Summary ($T_A = 25^\circ\text{C}$) EPC9179/80/81

Symbol	Parameter	Min	Nom	Max	Units
V_{Logic}	Gate drive and logic supply	5.5		12	V
V_{BUS}	Pulse charging supply	0		70	
V_{IN}	Input voltage range	0		5	
t_{PIN}	Input pulse width	2			ns
F_{PIN}	Pulse input frequency (does not account for thermal limitations)	0	Please see Table 2 for maximum recommended pulse frequency.		kHz

Table 1 provides the recommended operating conditions for the EPC9179/80/81. These conditions consider the electrical characteristics of the unmodified board, and do not take into account thermal limitations, since the latter depend on the load and use case.

LASER SAFETY WARNING: This board is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

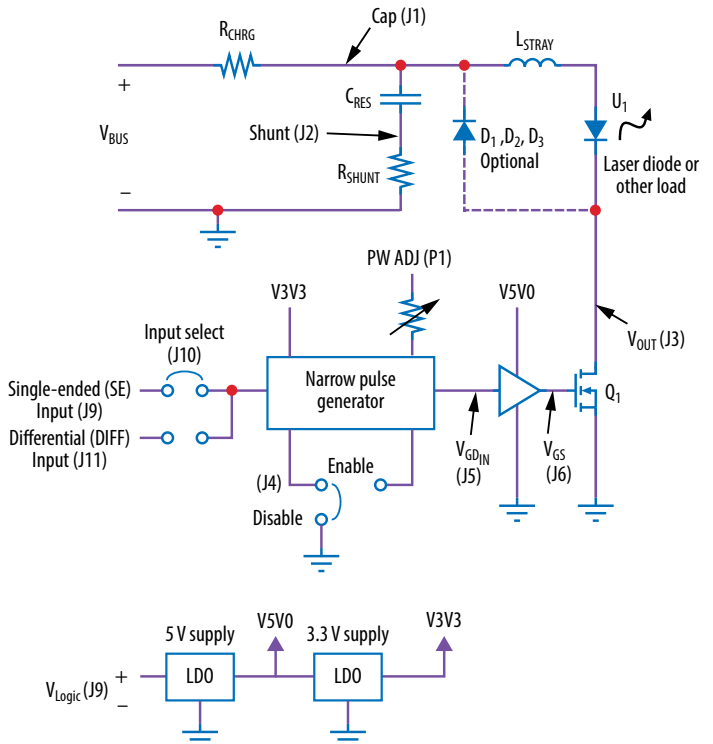


Figure 1. Block diagram of EPC9179/80/81 development board

MAIN FEATURES

- High current pulse generation with nanosecond pulse width
- Integrated high bandwidth measurements for key waveforms
- Optional narrow pulse generator to simplify operation with typical pulse and function generators
- Single-ended or differential logic inputs

OPERATING PRINCIPLE

The EPC9179/80/81 is intended as both a evaluation board and a flexible development platform. It is functional out of the box, but is designed to be modified to accommodate a broad range of applications. It is highly recommended that the user read the entire guide, especially the section **ADDITIONAL FEATURES**, in order to get maximum value from the EPC9179/80/81.

The EPC9179/80/81 is shipped as a resonant capacitive discharge laser diode driver. Please refer to the block diagram (Figure 1) and the schematic corresponding to the board of interest. It has several possible modifications (section **ADDITIONAL FEATURES**), but only the basic operation will be covered in this section. The EPC9179/80/81 operating principle is to charge the energy storage capacitance C_{RES} comprised of {C2, C3, C4, C5, C6 } through the resistor R_{CHRG} comprised of {R4, R5, R6, R7}, and when triggered, discharge C_{RES} through inductance L_{STRAY} and the laser diode or load U1. The stray inductance L_{STRAY} is a simplified representation of the total parasitic inductance of the power loop, and it is not a component mounted to the PCB. The capacitance C_{RES} and the inductance L_{STRAY} form the resonant network. Please see [AN027 eGaN FETs for Lidar – Getting the Most Out of the EPC9126 Laser Driver](#) for a complete description of resonant discharge laser driver operation.

The trigger pulse can be controlled from two different inputs. As shipped, it is controlled via an input pulse that is delivered to SMA connector J9, which is terminated on the demo board with 50 Ω. Input J9 feeds a level translator U7, and the output of the level translator is passed to an input select jumper J10. This pulse PLS_IN is passed to the input of the narrow pulse generator (NPG). When the input goes high, the output of the NPG follows, feeding the gate driver U3 which turns on Q1, allowing C_{RES} to discharge through the laser diode U2. If the NPG is disabled, then when the input goes low, Q1 turns off. If the NPG is enabled, the user can get a short gate drive output pulse to the lower limit of the gate drive IC U3’s capability. This allows the use of lower cost signal generators while working with the EPC9179/80/81. Details are given in Section **ADDITIONAL FEATURES**.

Once C_{RES} is discharged, Q1 should be turned off. Now, C_{RES} will recharge through R_{CHRG} . Once it is fully charged, the circuit can be fired again.

DIFFERENCES BETWEEN THE EPC9179, EPC9180, and EPC9181

The EPC9179, EPC9180, and EPC9181 evaluation boards are nearly identical in function, design, and layout. The key difference between the boards is the eGaN FET used for Q1. The FETs are selected to cover a wide range of peak pulse currents, with the larger FETs enabling higher peak currents. The primary tradeoff for the ability to reach higher peak currents is increased minimum pulse width. The combination of higher peak current and increased pulse width results in the need for increased resonant capacitor values and a reduced current measurement shunt value, along with a change to the latter’s ESL compensation capacitor. Table 2 gives a comparison of the three evaluation boards in order to highlight the differences.

It is recommended that the user choose the smallest FET that will meet the peak current needs. This will give the shortest possible pulse while still meeting the peak current requirements. The pulse width can be increased by increasing the value of the resonant capacitor.

Table 2. Comparison of the EPC9179, EPC9180, and EPC9181 evaluation boards

Parameter	Description	EPC9179	EPC9180	EPC9181	Units
Q ₁	FET part number	EPC2252	EPC2218A	EPC2204A	n/a
C _{RES} (C2-C6)	Effective total resonant capacitance	1.1	10.8	3.4	nF
R _{SHUNT} (R12-R16)	Effective total resonant current shunt resistance	102	30	60	mΩ
C7	Shunt compensation capacitance	12	36	18	pF
I _{Peak}	Nominal peak current for ideal diode load	75	230	125	A
T _{PW}	Nominal pulse width for high performance SMT laser diode	2-3	5-6	3-4	ns
T _{CHRG}	C _{RES} charge time to 0.98 V _{BUS} with ideal diode load	1.7	17	5.3	μs
F _{MAX}	Max pulse rate based on 1/T _{CHRG} (does not account for any thermal limitations)	590	59	190	kHz

LASER DIODE OR LOAD CONSIDERATIONS

The EPC9179/80/81 has a set of pads which can be used as is to mount a laser diode or alternative load. Figure 2 highlights the output pad locations. However, many laser suppliers have different mounting footprints, making it difficult to optimize the performance of the driver and still maintain the desired flexibility. The use of an interposer PCB provides a solution to this problem with only a small impact to performance.

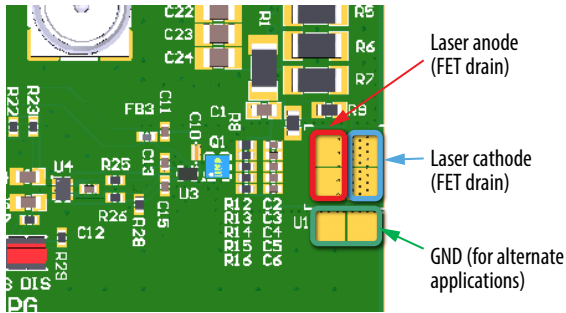


Figure 2. Output terminals of the EPC9179/80/81

The EPC9179/80/81 ships with the EPC9989 interposer PCB, shown in Figure 3. The EPC9989 has an assortment of 5 x 5 mm square interposer PCBs that can be snapped off the board. These interposers have various footprints on the top side that can accommodate several surface mount laser diodes, RF connectors, and several patterns designed to accommodate a wide variety of possible loads. These interposers mount between the EPC9179/80/81 and the laser diode or other load. Figure 4 shows an example of a laser in an SMD package mounted with one of the interposers.

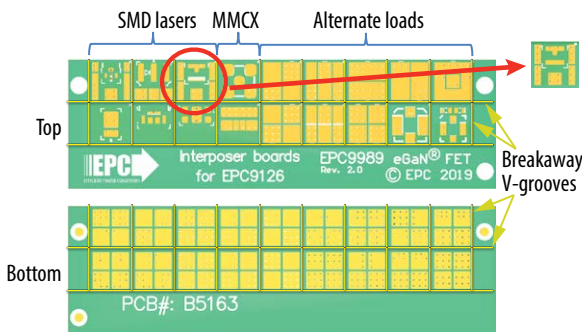


Figure 3. EPC9989 interposer PCB for mounting different lasers and loads

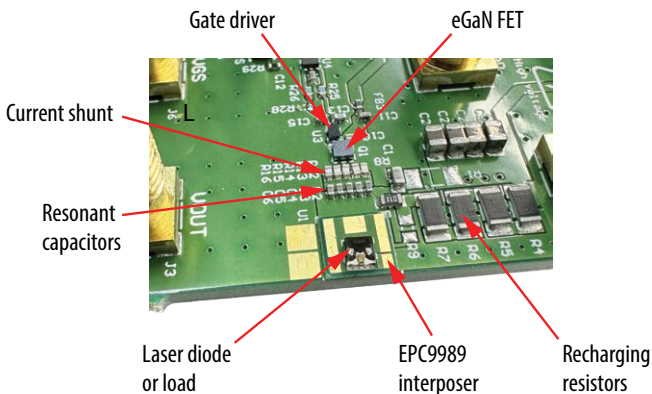


Figure 4. Laser diode mounted with EPC9989 interposer

The following procedure can be used to hand mount a laser diode or other load using the interposer. It is recommended that the person doing this work be experienced in hand rework of SMT components.

1. Prepare the EPC9179/80/81 by removing the jumpers on J4 and J10 so that they do not deform during reflow soldering. Use best practice to avoid electrostatic discharge (ESD) damage to the laser diode or other load, or to the EPC9179/80/81, during the following steps. Laser diodes are often extremely sensitive to ESD damage.
2. Select the interposer with the top side that fits the desired load.
3. Apply solder paste to the appropriate pads on the top side of the interposer.
4. Place the laser diode or desired load on the interposer such that the pads of the load line up with the matching pads on the interposer. Set this assembly gently aside, taking care not to bump it or displace the load since the solder paste is still soft.
5. Apply solder paste to the U1 pads on the EPC9179/80/81 PCB.
6. Using tweezers or other means, pick up the assembly of the interposer and laser or alternative load that was set aside in Step 4. Carefully position the assembly with the bottom side of the interposer facing the top side of the EPC9179/80/81 on the U1 footprints and set in place.
7. Reflow the EPC9179/80/81 together with the interposer-load assembly using the laser or load manufacturer's recommended temperature profile for the selected solder. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user, but it should be noted that many lasers have a polymer optical assembly that is sensitive to overheating.
8. Replace jumpers on J4 and J10.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. Maxwell's Laws dictate that the discharge capacitors, current sense resistors, and the eGaN FET must all be mounted in close proximity to minimize inductance. The resulting proximity of all these components to the laser or other load means that the user must take extra care not to damage any components when mounting the laser or changing other components in the power loop.

The schematic and layout files for the EPC9989 interposer can be found on the main information pages for the EPC9179/80/81. In addition, a PCB footprint is available so that the user may design their own custom interposer.

Laser diode current pulses can result in peak powers of several hundred watts to over 1 kW. Laser diodes for lidar applications are designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

MEASUREMENT CONSIDERATIONS

SMA jacks are provided to measure key signals in the circuit, including gate drive IC input, Q1 gate voltage, Q1 drain voltage, resonant capacitor C_{RES} voltage, and the sense voltage of the current measurement shunt (see Figure 5). All measurement points are designed to be terminated in $50\ \Omega$, hence when viewing waveforms, the oscilloscope inputs should be set to a $50\ \Omega$ input. Ideally, unused outputs should be also terminated with a $50\ \Omega$ load to prevent the probes from creating additional resonances. However, the Q1 drain voltage V_{OUT} , the discharge capacitor sense voltage CAP, and the current shunt output SHUNT also have impedance values relatively close to $50\ \Omega$ s as seen from the SMA connector. Thus, the reflection coefficient is small and in practice, the subsequent resonances are small if these are left unterminated. It is recommended that the user verify that this is suitable for their own requirements.

All sense measurement SMA connectors except for the shunt measurement use the transmission line voltage probe principle to obtain waveform fidelity at sub-ns time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. These factors are given in Table 3. The impedance of the probes at the measurement node is relatively small ($\sim 1\ \text{k}\Omega$). In order to minimize the effects of the low probe impedance on the operation of the demo board and prevent overheating of the probe input resistors, the output voltage (J3) and capacitor voltage (J1) probes have DC blocking capacitors on the PCB. As a result, measured pulse waveforms will not have any DC component and will exhibit droop as pulse widths

and other waveform features approach the RC time constant of the probe. The user should keep these factors in mind if accustomed to more conventional oscilloscope probes. If long pulse widths are used, the droop will become substantial, and an external probe may be used to measure these slower waveforms more accurately.

The current shunt is designed to estimate the discharge capacitor current. Substantial effort has been made to reduce the inductive effects of the current shunt, both through the use of carefully selected resistors and a compensation network to help compensate for the shunt equivalent series inductance. However, the shunt is a compromise between current measurement accuracy and minimizing the impact on the laser driver performance. If a more accurate shunt waveform measurement is desired, the shunt resistors may be replaced with ones that provide higher accuracy at the bandwidth required. This will require higher resistor values which will contribute to errors in the capacitor voltage measurement, increase power dissipation, and reduce the available peak current for a given bus voltage V_{BUS} . Additionally, note that the measured capacitor current also includes the current due to D1, D2, and D3 (if included), and PCB capacitance, in addition to the load current.

Finally, when one wishes to understand detailed switching behavior, it is important to consider the timing mismatch of the probe point. The approximate delay times have been calculated based on the assumption that a $50\ \Omega$ transmission line connects the SMA to the test point of interest, neglecting the effects of passive component pads. They are listed in Table 3.

Table 3: Key properties of SMA measurement outputs assuming $50\ \Omega$ terminations on measurement instruments

Designator	PC label	Description	Attenuation factor	PCB propagation delay (calculated)	DC blocking cap	DC blocking LF time constant	On-PCB termination
J1	CAP	Resonant capacitor voltage	41 V/V	119 ps	10 nF	10 ms	YES
J2	SHUNT	Resonant capacitor current measurement	19.6 A/V (EPC9179) 66.7 A/V (EPC9180) 33.3 A/V (EPC9181)	116 ps	none	n/a	YES
J3	V_{OUT}	Q1 drain voltage	41 V/V	118 ps	10 nF	10 μ s	YES
J5	V_{GDIN}	Gate drive IC (U3) input voltage	20 V/V	163 ps	none	n/a	NO
J6	V_{GS}	Q1 gate voltage	20 V/V	171 ps	none	n/a	NO

QUICK START PROCEDURE

The EPC9179/80/81 evaluation board is simple to set up for evaluation of the performance of the EPC2252, EPC2218A, and EPC2204A eGaN FETs.

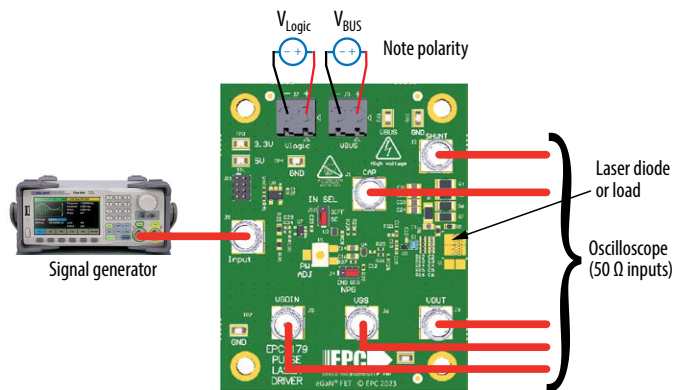


Figure 5. Connection and measurement setup

The procedure in this section provides basic instructions to operate the boards in the default (as shipped) configuration. Refer to Figure 2 for proper connection and measurement setup and follow the procedure below:

1. **Review laser safety considerations when using a laser load. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Review high voltage safety considerations since the evaluation boards may operate with voltage levels that may present a safety hazard. Refer to qualified safety personnel as necessary.**
2. With power off, install laser diode U1 or alternative suitable load. The use of one of the interposers from the included EPC9989 can be used to mount the laser or alternative load. This is discussed in the section **LASER DIODE OR LOAD CONSIDERATIONS**.
3. With power off, connect the main power supply to V_{BUS} (J8), taking care to observe the correct polarity.
4. With power off, connect the logic supply (5.5-12 V_{DC}) V_{Logic} (J7), taking care to observe the correct polarity.
5. With power off, connect the signal pulse generator to the input J9. J9 is terminated with 50 Ω , and is designed for a 3.3 V logic input as shipped. Ensure that the pulse repetition frequency is within the recommended range.
6. Connect the remaining measurement SMA outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section **MEASUREMENT CONSIDERATIONS** for more information, including the attenuation values for each output.
7. Verify that the logic supply voltage is set to a value within the specifications and turn on the logic supply voltage.
8. Verify that the bus supply voltage is set to a value within the specifications and turn on the bus supply voltage.
9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate opto-electronic receiver.

10. Once operational, adjust the bus voltage, input pulse width, and pulse repetition frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

ADDITIONAL FEATURES

The EPC9179/80/81 is designed to accommodate a range of use scenarios. Some of these are available with no modifications to the PCB. The locations of key adjustments are indicated in Figure 6. Advanced features require the ability to remove and replace SMT chip components. It is recommended that these are done by qualified personnel with experience in SMT rework.

When reading this section, please have the full schematic available for reference.

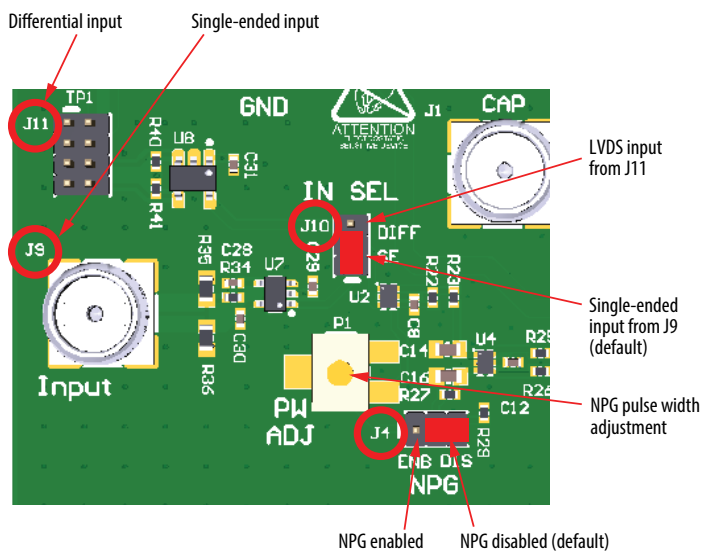


Figure 6. Location of key features and adjustments

NARROW PULSE GENERATOR

Many signal generators cannot produce an accurate, short pulse with sub-ns edges. The EPC9179/80/81 includes a narrow pulse generator (NPG) function to obtain narrow output pulses of adjustable width, following a method given in Section 8.2.2.2 of the Texas Instruments LMG1020 data sheet. The pulse width is controlled through Potentiometer P1. When adjusting P1, the use of a non-conductive tool is recommended due to the sensitivity of the adjustment to stray capacitance.

The NPG is enabled by moving the jumper on J4 to the leftmost position (see Figure 6). With the NPG enabled, the input pulse signal is split into separate turn-on and turn-off paths. The turn-on path goes through buffer U2, a fixed RC delay {R23, C14} and buffer U4 on to the IN+ (non-inverting) input of gate driver U3, which turns output Q1 on. The turn-off path is similar, but has an adjustable RC delay {P1, R27, C16}. This delayed pulse is sent to the IN- (inverting) input of U3. The longer delay of the second path means that after some interval, the IN-input of U3 goes high, and Q1 is turned off, ending the output pulse.

Potentiometer P1 is used to adjust this turn-off delay and the resulting output pulse width, with clockwise rotation increasing the pulse width applied to the gate of Q1. Note that the minimum delay setting causes both turn-on and turn-off paths to have an approximately equal delay, which would result in a zero-width pulse. Since the gate driver U3 has a minimum pulse width specification of > 1 ns, it is U3 that determines the minimum attainable output pulse width. Small errors in the delay path do not significantly impact the output. The maximum pulse width that can be obtained with the NPG is approximately 60 ns, so if longer pulses are needed, the NPG should be disabled.

When using the NPG, it is recommended that the input pulse should be at least 10 ns longer than the desired output pulse to guarantee reliable operation under all ambient conditions.

ADVANCED FEATURES

The EPC9179/80/81 has the option to be controlled from a differential input. As shipped, this input is configured for standard LVDS signals. It input is available to the user through the 8-pin header J11. Table 4 shows the pinout for J11, which also provides alternate access to some of the power supply voltages on the board. In order to enable the LVDS or other differential input, move the jumper on J10 to the upper position (Figure 6).

Table 4. J11 Pin Description

J11	Pin Description	Schematic Net Name
1	Not connected	N/A
2	Internal 5 V supply	V5V0
3	Logic supply	Vlogic
4	Internal 3.3 V supply	V3V3
5	Ground	GND
6	Non-inverting differential input	IN_D+
7	Ground	GND
8	Inverting differential input	IN_D-

LVDS AND ALTERNATE INPUTS

The following features require modifications to the board.

Load Clamping diodes

Empty component footprints are present on the EPC9179/80/81 to allow the user to mount up to 3 clamp diodes (D1, D2, D3). While such diodes can provide some protection to FET Q1 and laser or load U1, they have parasitic inductance and capacitance that can reduce performance. In addition, they clamp the laser or load reverse voltage and this can reduce turn-off speed. Hence, they are not populated, and it is left to the user to determine whether they are useful for a particular application.

Eye safe operation

In some applications, it is required that the driver remain eye-safe in the event of a failure causing Q1 to be on in an uncontrolled manner, e.g. an erroneous gate drive signal or FET short. While the charging resistance provides some current limiting, it may not be enough. In such a case, R8 can be removed, and at least one of the clamp diodes D1, D2, or D3 populated. Once this is done, the capacitor bank will be charged through the charging resistance and the clamp diode(s). However, if Q1 is on, the charging current will now flow through Q1 and not the laser diode, preventing any light output.

Fast Refresh

The value of the energy storage cap {C2, C3, C4, C5, C6} can be modified as desired, as well as the recharge resistor {R4, R5, R6, R7}. In the extreme case, the resistor may be reduced to 0 Ω for cases where a capacitive discharge pulse is not desired. The latter can also be accomplished by populating R1. If this approach is taken, it is recommended that R1 have some small value of resistance (5 Ω to 20 Ω) to damp possible resonances in the power bus.

Logic input level and type

The input specification of the demo board may also be modified. For single-ended inputs, the input logic level can be reduced from 3.3 V logic to 2.5 V or 1.8 V by changing R37. Please see the U7 datasheet for further details. If a differential input different than LVDS is desired, the differential receiver U8 can accommodate sub-LVDS, CML or LVPECL signals by changing the values of U8's input termination network. Please see the U8 datasheet for further details.

Improving laser cooling

Some pulse laser applications are thermally limited by laser power dissipation. Usually, the laser die substrate forms the cathode, which is attached to the drain of Q1. Since this terminal is the most electrically active terminal in the whole circuit, it must be kept small and electrically isolated from anything else in the circuit. This makes it difficult for heat to flow out of the laser. This terminal is connected to a small copper land on the bottom of the PCB with a thermally conductive via array. Hence, the thermal resistance from the laser cathode to the bottom thermally conductive ground plane of the PCB can be reduced by populating R17, R18, R19, and R20. The high electrical resistance of these parts means they have negligible electrical effect, but the thermal resistance of the chip resistors is much lower than the PCB substrate. Note that thermal performance can be further improved with the use of thermal bridges, which are essentially a blank resistor chip made with an aluminum nitride body for enhanced thermal performance.

PERFORMANCE EXAMPLES

Figures 7, 8, and 9 show typical waveforms for the EPC9179, EPC9180, and EPC9181 demo boards, respectively. In all cases, the waveforms were obtained with $V_{BUS} = 70\text{ V}$ at room temperature.

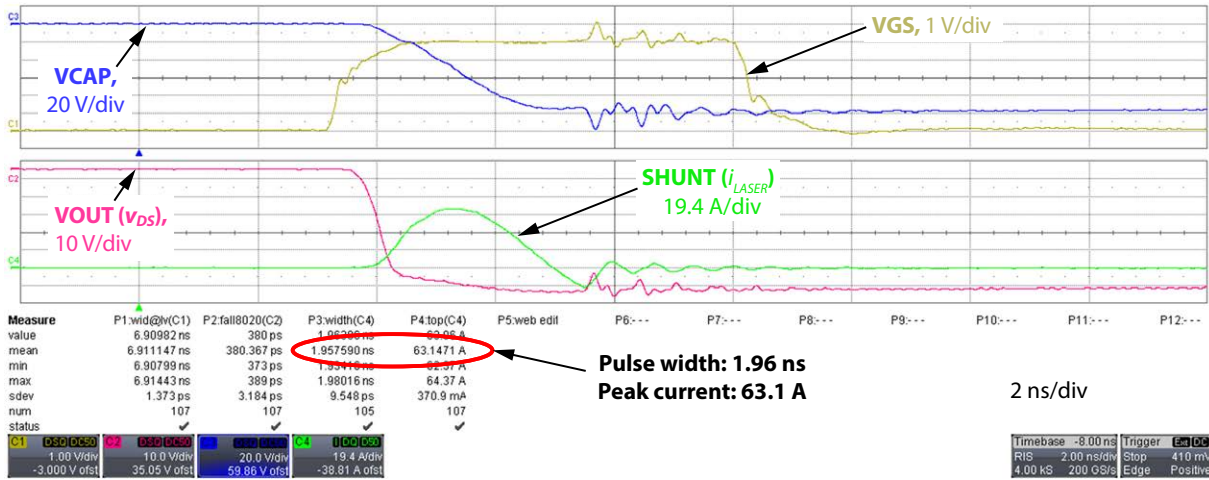


Figure 7. Waveforms for the EPC9179 demo board using an ams OSRAM SPL S1L90A_3 A01 single channel triple junction laser diode mounted with the EPC9989 interposer.

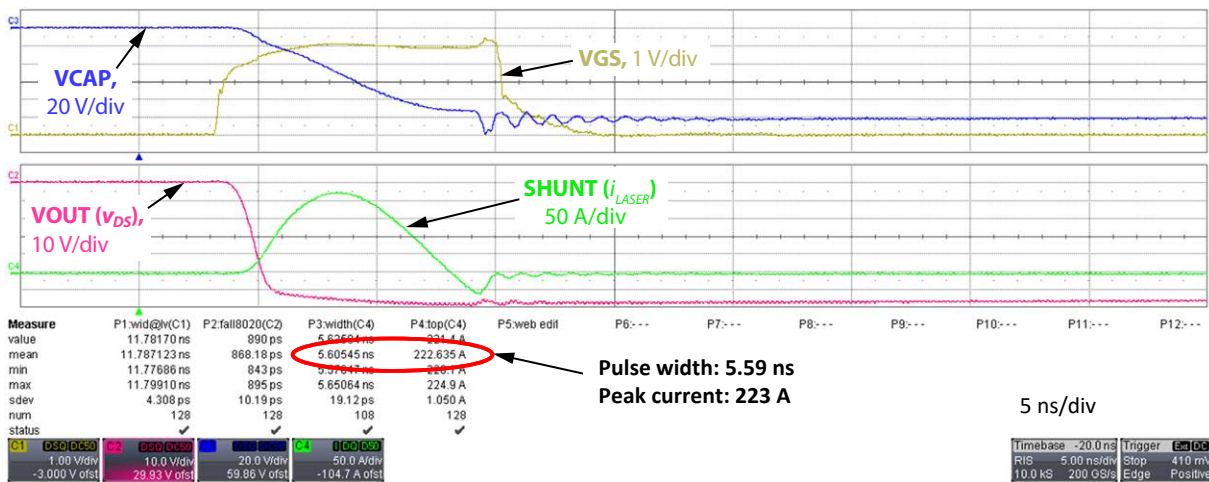


Figure 8. Waveforms for the EPC9180 demo board using an ams OSRAM SPL S4L90A_3 A01 four channel triple laser diode mounted with the EPC9989 interposer. All channels are connected in parallel.

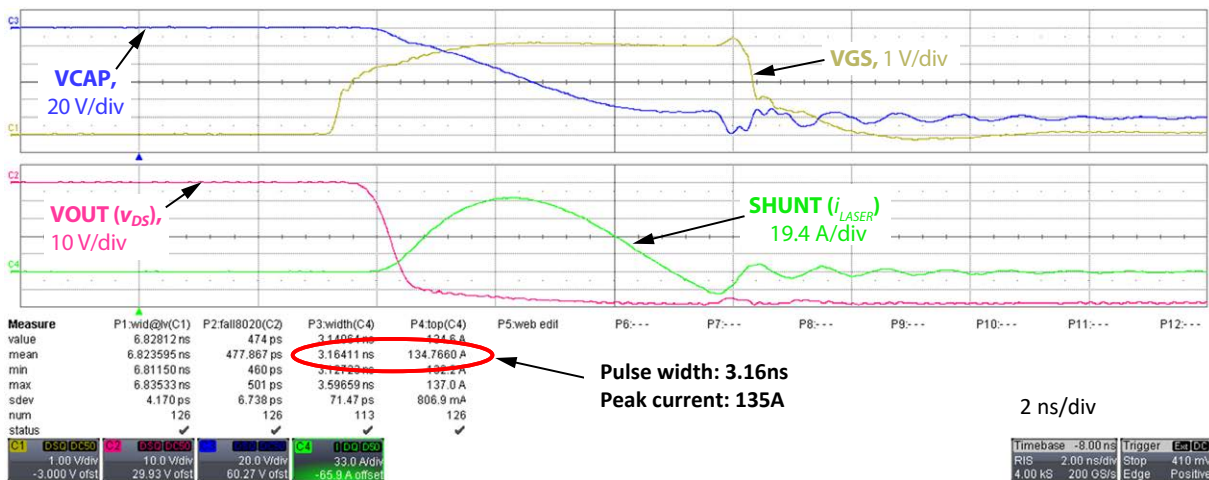


Figure 9. Waveforms for the EPC9181 demo board using an ams OSRAM SPL S4L90A_3 A01 four channel triple laser diode mounted with the EPC9989 interposer. All channels are connected in parallel.

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Evaluation Board Notification

The EPC9179/80/81 boards are intended for product evaluation purposes only. They are not intended for commercial use nor is it FCC approved for resale. Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions. This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

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