Evaluation Board EPC9182 Quick Start Guide

Low Voltage, AC Load, Solid-State Relay

January 16, 2023

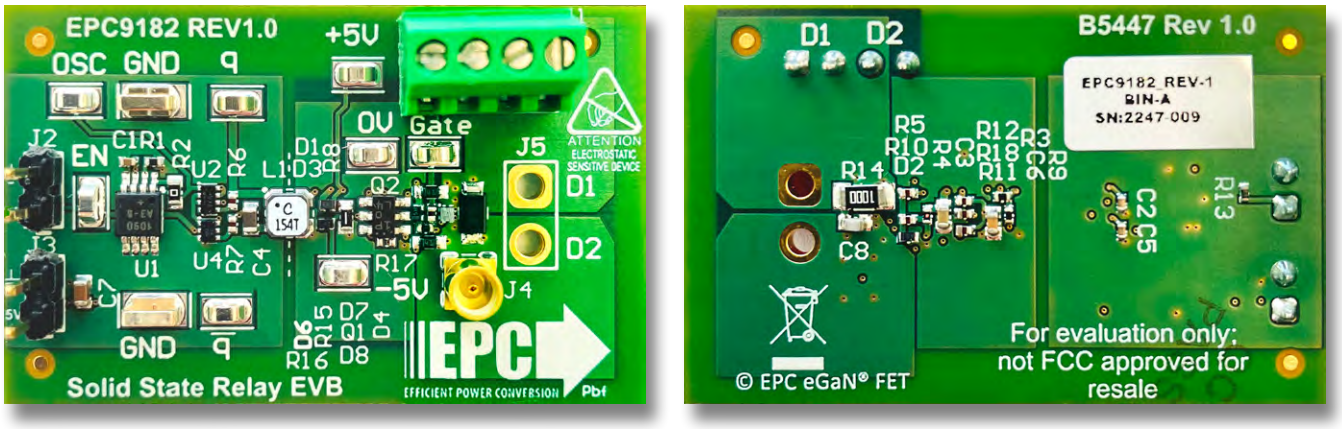
Version 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9182 evaluation board is an AC voltage solid-state relay (SSR) evaluation board, featuring the bi-directional, 100 V rated, 60 mΩ (D1-to-D2), EPC2121 eGaN® FET and can conduct up to 2 A_{RMS} continuous AC load current. This board supports 3.3 V/5 V logic enable and is designed to protect against over voltage of the FET. A block diagram overview of the function blocks of the EPC9182 is shown in figure 1.

The circuit featured on the EPC9182 is suitable for use in thermostats and can replace traditional relays.



EPC9182 board

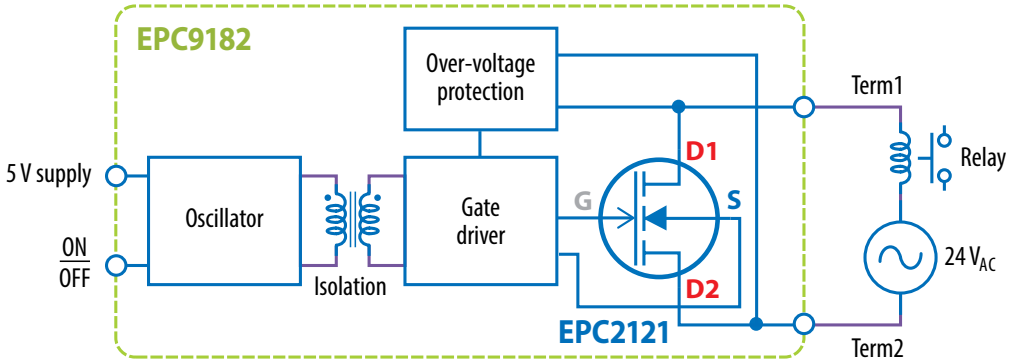


Figure 1: Block diagram overview of the EPC9182 evaluation board

MAIN FEATURES

- Bi-directional voltage blocking capability
- Low static power consumption
- FET gate is held OFF even when no power is present
- Isolation between logic and power circuits
- Small size

FEATURED eGaN FET

The EPC9182 evaluation board features the bi-directional blocking, 100 V rated, 60 mΩ $R_{DS(on)}$ (D1-to-D2), EPC2121 eGaN FET. The FET symbol and photo with pin assignment is shown in figure 2.

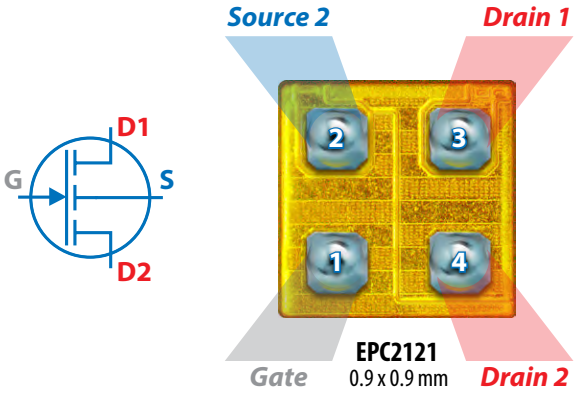


Figure 2: Featured eGaN FET of the EPC9182 evaluation board. Symbol (left), photo with pin assignment (right)

Figure 3 shows an image of both sides of the EPC9182 evaluation board, with the EPC2121 FET highlighted and showing the location of the various functional circuits.

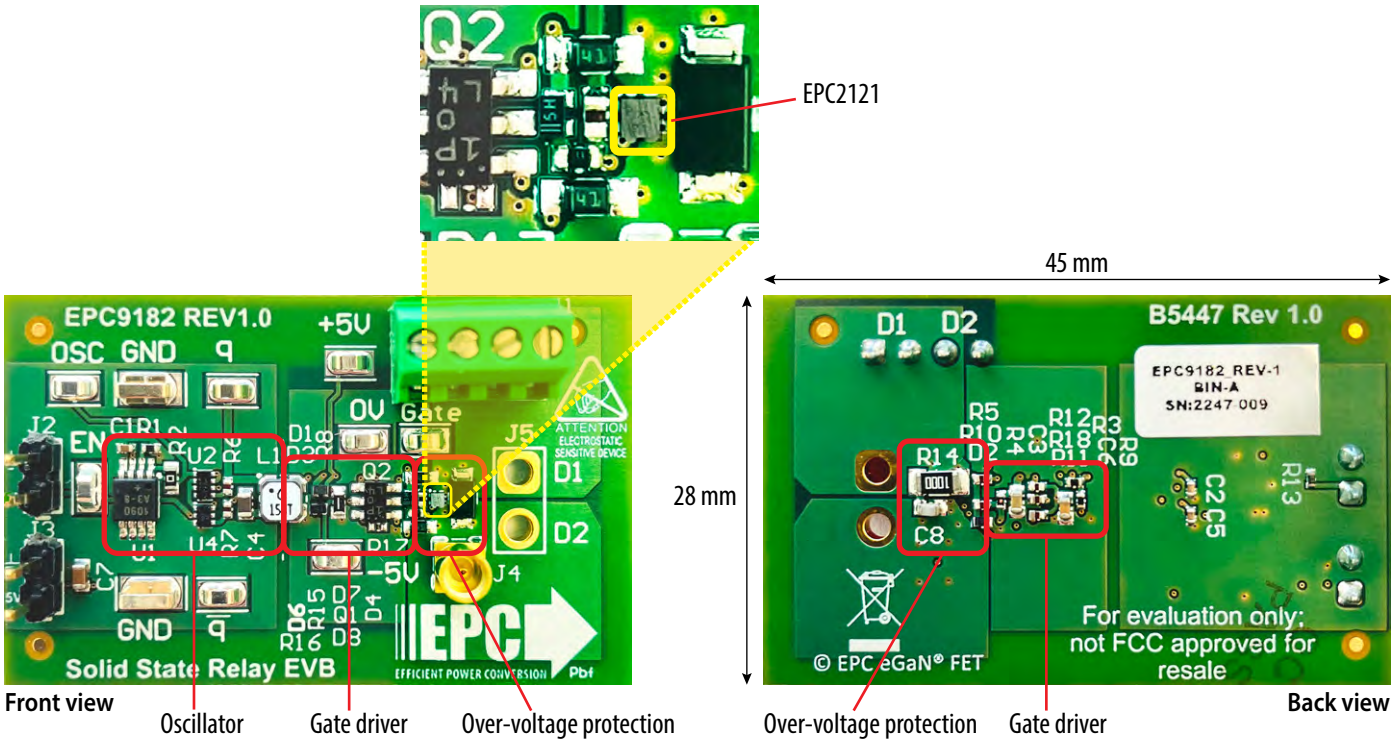


Figure 3: Functional block diagram overview of the EPC9182 evaluation board with the FET highlighted

RECOMMENDED OPERATING CONDITIONS

Table 1: Electrical Characteristics (T_a = 25 °C unless specified otherwise) EPC9182

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{D1-D2}	Drain-to-Drain voltage(1)	TVS clamp		±65		V
		FET clamp		±75		
I_{D1-D2}	Drain-to-Drain current	50 / 60 Hz		2		A_{RMS}
V_{5V}	Logic supply voltage		4.5	5	5.5	V
V_{iH}	Enable signal logic high		0.7 · V_{CC}		5.5	
V_{iL}	Enable signal logic low		-0.3		0.3 · V_{CC}	
E_{clamp}	Over-voltage clamp energy	T_J limit of 150°C		tbd		mJ
V_{iso}	GND to 0 V isolation			100[2]		V_{AC}

(1) The EPC2121 is 100 V rated. Refer to the EPC212 datasheet for device specifications. The EPC9182 includes 2 methods of over-voltage clamping.

(2) One minute winding-to-winding isolation

DETAILED DESCRIPTION OF THE EPC9182 CIRCUIT

Refer to figure 1 for the main blocks that comprise the EPC9182 evaluation board.

Gate driver

Figure 4 shows the circuit schematic of the EPC9182 gate driver circuit.

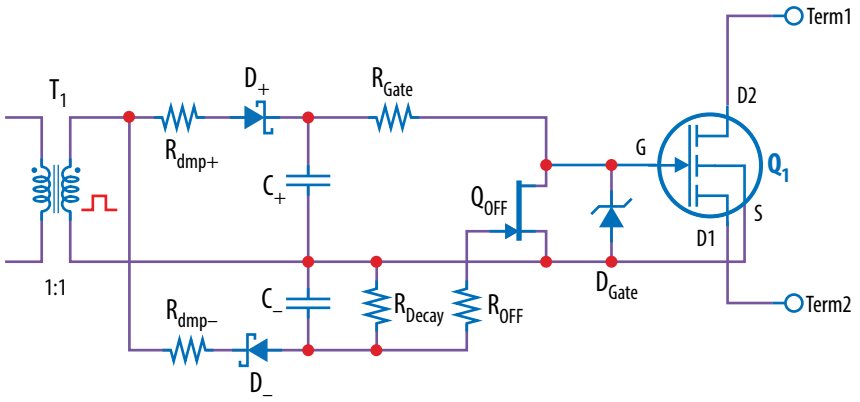


Figure 4: Schematic of the gate driver circuit of the EPC9182 evaluation board

The gate driver circuit is driven from an isolation transformer (T_1) at approximately 300 kHz. The secondary of the transformer is bi-polar rectified (D+, R_{DMP+}, C_+, D–, $R_{DMP–}$, C_) to produce both a +5 V and -5 V. The +5 V is used to turn on the EPC2121 GaN FET (Q_1). A JFET (Q_{OFF}) with R_{OFF} is used to ensure the Gate-to-Source of the EPC2121 is kept off when power to the transformer is removed and ensures the gate is held off even without power to the board.

When the transformer is powered, then the -5 V is used to turn off the JFET because C_ is smaller than C_+ and thus it charges first turning off the JFET thus allowing the +5 V to turn on the EPC2121. R_{Decay} is used to discharge C_ thus ensuring the JFET (Q_{OFF}) turns on. R_{Gate} is used to limit loading on the +5 V when the JFET is in the process of turning off. Zener diode D_{Gate} is used to protect the gate of the EPC2121 from over-voltage.

The transformer is used to provide functional isolation between the control signal and the EPC2121 device.

Over-voltage protection

The EPC9182 is intended to power AC relay's which have an inductive electrical characteristic that can lead to over-voltage damage to the EPC2121 device if not managed. To protect against voltage spikes during inductive switching events, the EPC9182 is equipped with three forms of over-voltage protection circuits on the EPC9182:

- TVS over-voltage clamp
- Drain feedback over-voltage clamp
- Snubber

Figure 5 shows the circuit schematic of the EPC9182 over-voltage protection circuits.

TVS over-voltage clamp

The primary over-voltage protection for the EPC2121 device is a bi-directional TVS diode (D_{TVS}) that clamps the voltage to the rated voltage of the TVS diode during an over-voltage event driven by load current at turn-off.

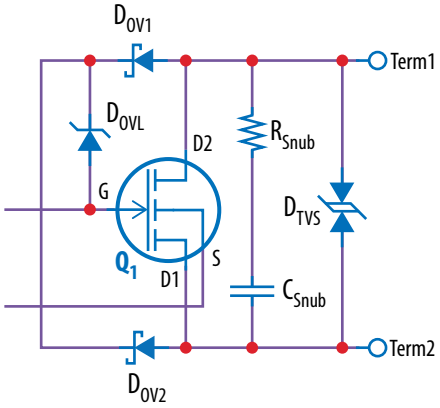


Figure 5: Schematic of the over-voltage protection circuit of the EPC9182 evaluation board.

Drain feedback over-voltage clamp

The secondary over-voltage protection circuit for the EPC2121 device uses the device itself to clamp and dissipate the over-voltage event energy. This is done by feedback of the Drain voltages (D1 or D2) back into the Gate of the device using D_{OV1}, D_{OV2}, and D_{OVL}. The clamping voltage is determined by the voltage rating of the Zener diode (D_{OVL}) and the forward voltage of the blocking diode D_{OVx}. In the default configuration of EPC9182, this over-voltage protection circuit will not activate because it it set well above the voltage level of the TVS clamp diode. To test this function, remove the TVS diode (D4).

Snubber

The snubber circuit comprises a series R_{Snub} and C_{Snub} circuit used to damp residual energy and damp high frequency ringing across the EPC2121 device during turn-off.

Oscillator and transformer driver

The oscillator circuit powers the transformer (T1) and comprises three main circuits:

- An oscillator
- D-flop-flop
- Turn-on edge starter

Figure 6 shows the circuit schematic of the EPC9182 oscillator and transformer driver circuits.

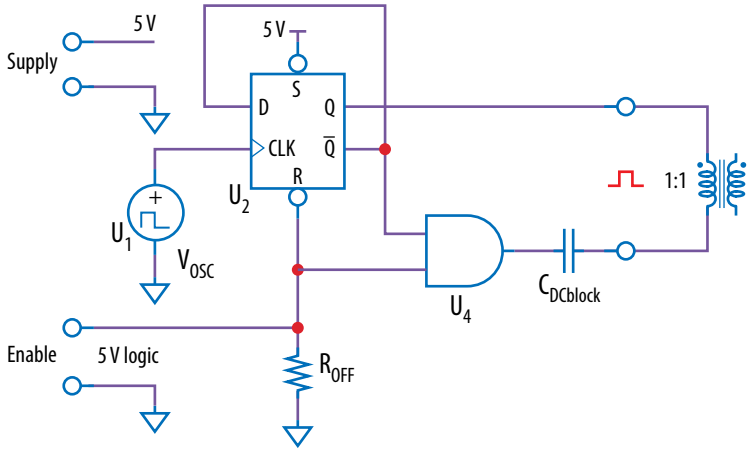


Figure 6: Schematic of the oscillator and transformer driver circuit of the EPC9182 evaluation board

A fixed frequency, 600 kHz, square-wave oscillator is fed into a D-flop-flop that halves the frequency and ensures a near perfect 50% duty cycle output required to prevent saturation of the transformer due to timing offset. An AND logic gate is used to add an ***Enable*** function to the circuit. To always ensure that the transformer starts with a specific polarity, the ***Enable*** if also fed to the $\overline{\text{Reset}}$ of the D-flip-flop. This forced polarity start ensures that the -5 V charges slightly earlier than the +5 V and ensures that the JFET is turned off as soon as possible at the onset of turn-on of the EPC2121. The non-inverting and inverting outputs are fed directly into the transformer as a differential signal that then powers the gate driver. A DC blocking capacitor ($C_{DCblock}$) is added as an extra measure to prevent transformer saturation. R_{OFF} is used to ensure that the circuit is default in the Off state when no signal is present at the ***Enable*** input.

CONNECTIONS

Figure 7 shows the power and logic connections to the EPC9182 evaluation board. There are two options for the ***Enable*** signal:

1. A 5 V supply in series with a switch shown as option 1
2. A direct voltage applied to the ***Enable*** input shown as option 2

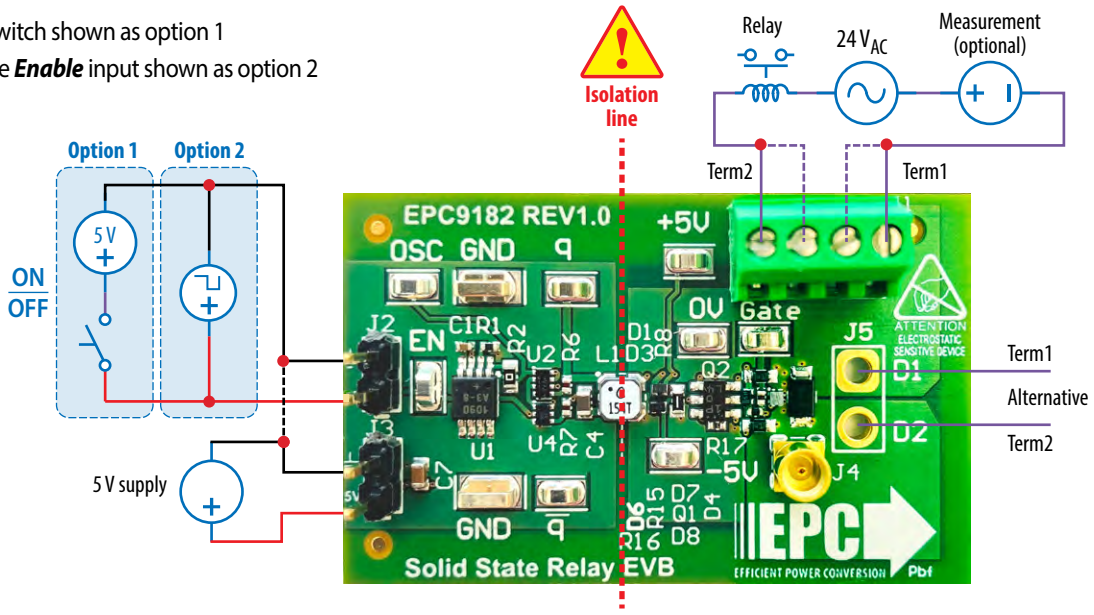


Figure 7: Power and signal connections to the EPC9182 evaluation board

Test points and measurement setup

Figure 8 shows the various measurement connections of the EPC9182 evaluation board.

It is important to note that certain connections should not be made as highlighted in figure 8. Notably DO NOT connect GND to 0 V.

The available measurement nodes with their respective reference are:

- **OSC-GND**: The 600 kHz oscillator output
- **EN-GND**: The ***Enable*** (ON/OFF) signal
- **q, /q-GND**: The nodes powering the transformer
- **+5 V –0 V**: The +5 V rail of the gate driver – Powers the EPC2121 gate
- **–5 V –0 V**: The -5 V rail of the gate driver – Powers the JFET gate
- **Gate –0 V**: Gate of the EPC2121 GaN FET
- **D1–D2**: Drain 1 to Drain 2 voltage either using the power connector (J1) or MMCX connector (J4). **This must be a floating / isolated measurement.**

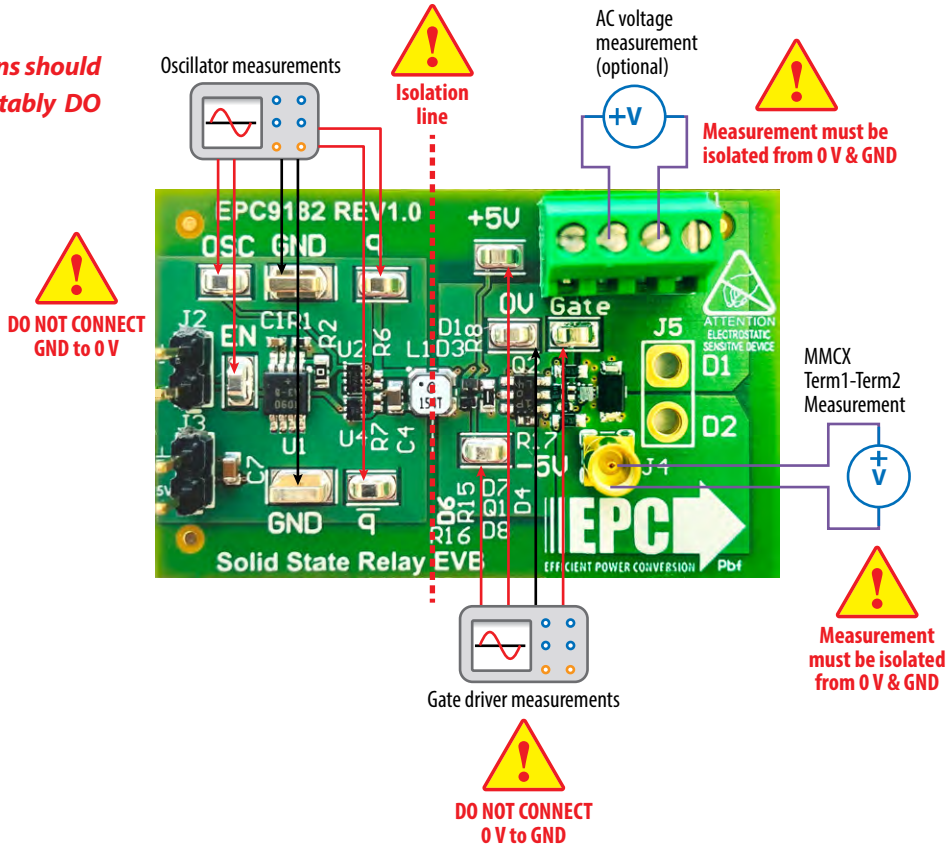


Figure 8: EPC9182 test point pad and hookup locations and designations

QUICK START PROCEDURE

Follow the procedure below to operate the EPC9182 evaluation board:

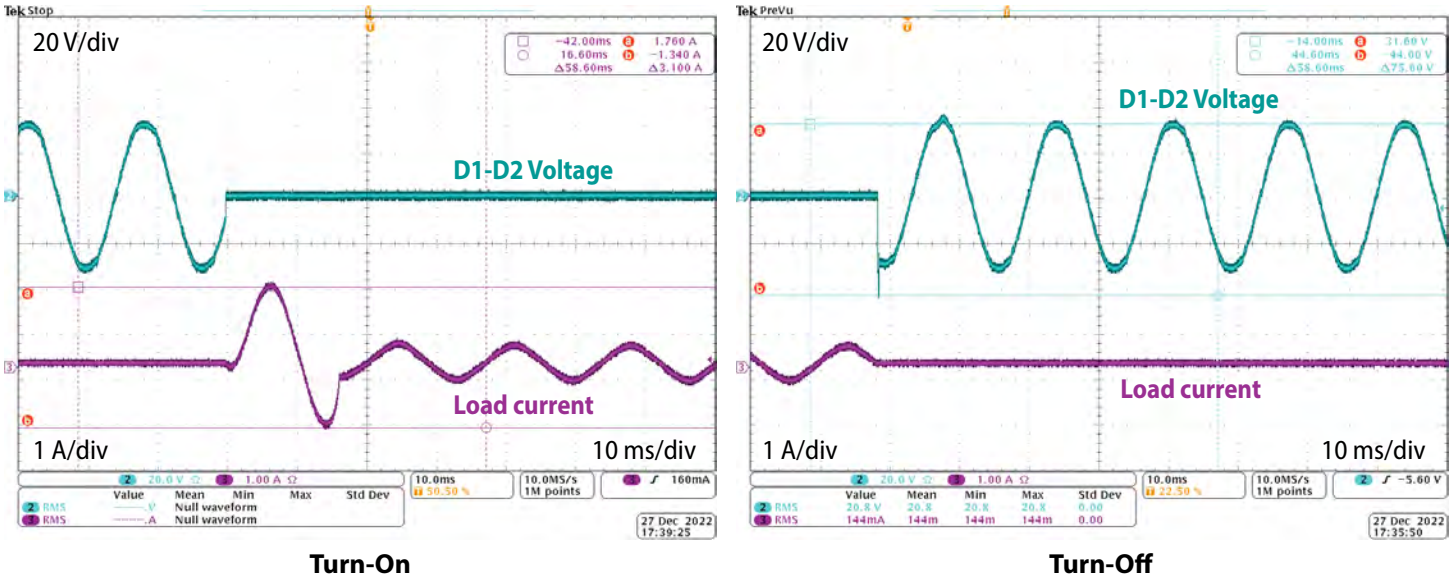
1. With power off, connect an AC source (24 V_{AC}) and the mechanical relay (load) in series with the power terminals (D1 and D2), as shown in Figure 7.
2. With power off, connect either a 5 V source in series with a switch (Option 1 of figure 7) ***or*** a 5 V source with On/Off switch (Option 2 of figure 7) to the ***Enable*** connector (J2) (note polarity).
3. With power off, connect a 5 V power supply to J3 (note polarity).
4. Turn on the 5 V supply. The circuit is by default OFF.
5. Turn on the AC source, no current should be drawn.
6. Enable the circuit by either activating the switch (Option 1) or by turning on the enable power supply (Option 2). The mechanical relay should close (clicking sound should be heard and the plunger will move inwards). If a load is attached to the high-power terminal of the mechanical relay, then the circuit should be closed.
7. Take various measurements on the board as needed paying careful attention not to connect GND to 0 V as shown in figure 8.
8. Disable the EPC9182 by either deactivating the switch (Option 1) or by turning off the enable power supply (Option 2). The mechanical relay should open (clicking sound should be heard and the plunger will move outwards).
9. Turn off the AC source.
10. Turn off the 5 V source.

EXPERIMENTAL VALIDATION

The EPC9182 operates as a relay and either a DC or AC supply may be used for the main power terminals (D1-D2) of the EPC9182. The following experimental results were taken using a **Siemens 45EG20AJ** or **Dayton 6GNY4B** mechanical relay as load and the type of source and reason is listed specified in the experimental description. Refer to figure 1 for system diagram applicable to the experimental setup used in this section.

Basic operation

For basic operation a 24 V_{AC} source is used to evaluate basic functionality. The measured turn-on and turn-off waveforms are shown in figure 9.

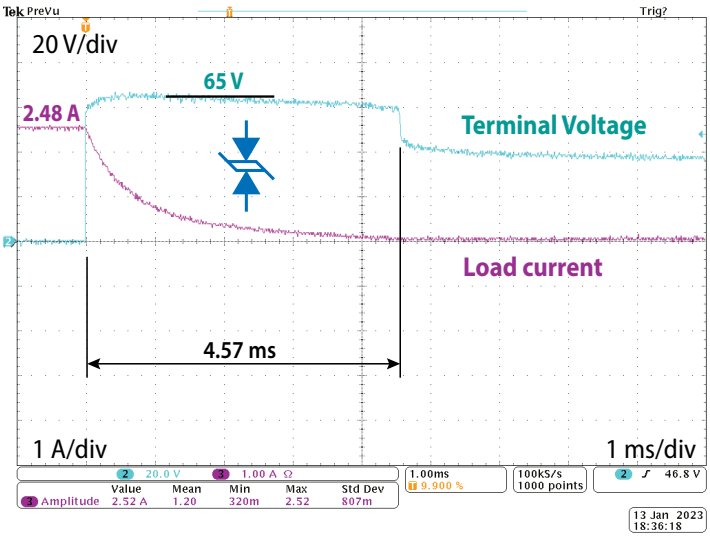


Turn-On **Turn-Off**

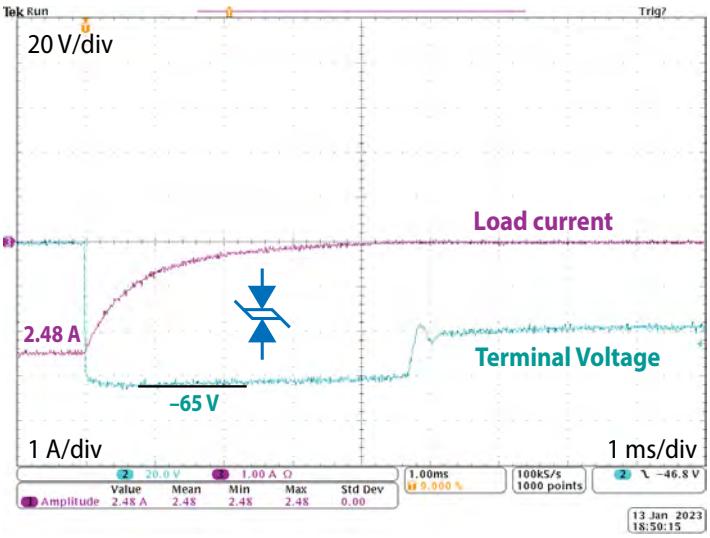
Figure 9: Measured waveforms for basic operation of the EPC9182 operating with 24 V_{AC} and powering a Siemens 45EG20AJ Relay

TVS voltage clamping results

At turn-off, the inductance of the mechanical relay will induce a voltage spike. When installed, the TVS diode (D4) will clamp this energy spike to the rated voltage of the diode and protect the EPC2121 from over-voltage damage. The zoomed-in measured waveforms at turn off when using a 37 V_{DC} supply for the power terminals is shown in figure 10 for both polarities. DC was selected for this test as it represents the worst-case scenario and the on-duration for the relay was set to a maximum of 0.5 seconds to minimize power dissipation in the relay coil. The clamping energy that the TVS diode dissipates can be determined from the measured waveforms. The current at turn-off is 2.48 A, the clamping voltage is 65 V and total clamping time is around 4.6 ms, resulting in approximately 171 mJ of total clamping energy with peak power of 161 W.



Positive Direction

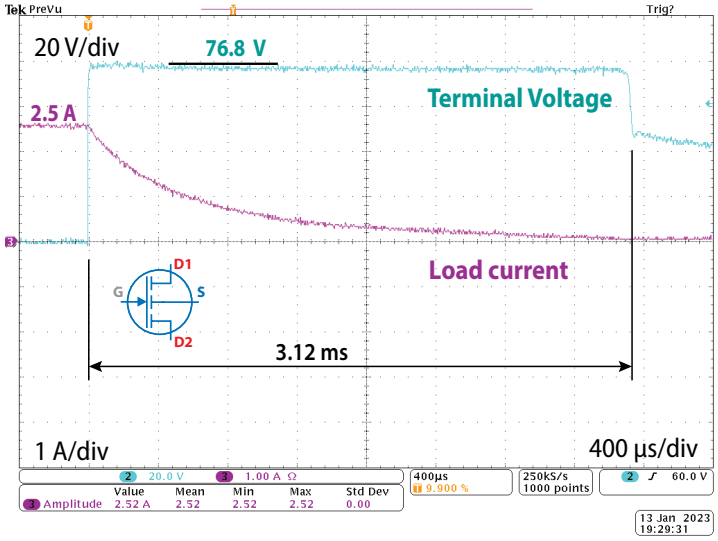


Negative Direction

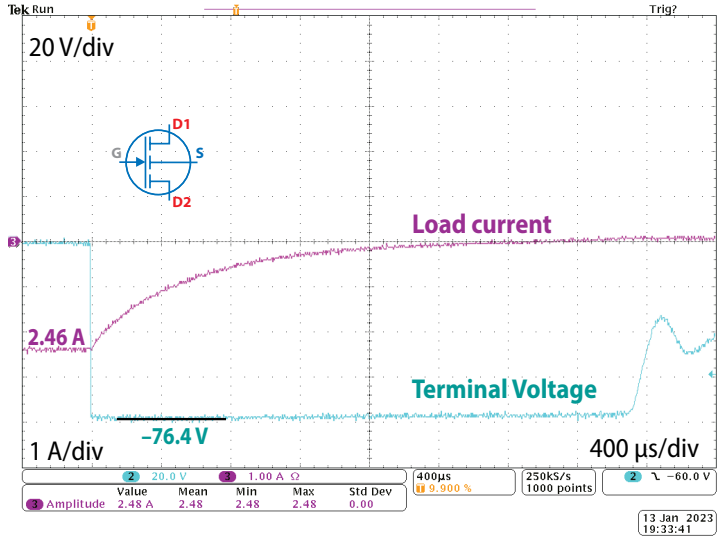
Figure 10: DC inductive switching waveforms at turn off with 37 V_{DC}, TVS diode installed and mechanical relay (Dayton 6GNY4B)

Drain feedback over-voltage clamping results

For these tests, the TVS clamping diode (D4) was removed and the sole protection was that of the drain feedback circuit. The zoomed-in measured waveforms at turn off when using a 37 V_{DC} supply for the power terminals is shown in figure 11 for both polarities. DC was selected for this test as it represents the worst-case scenario and the on-duration for the relay was set to a maximum of 0.5 seconds to minimize power dissipation in the relay coil.



Positive Direction



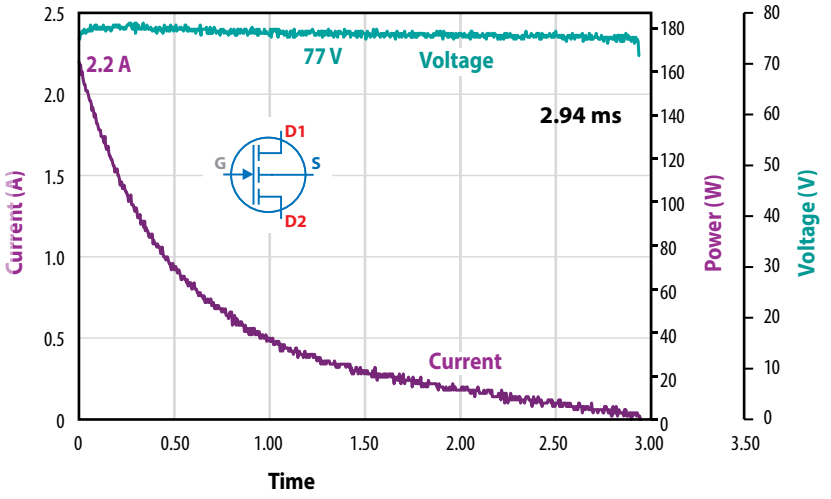
Negative Direction

Figure 11: DC inductive switching waveforms with 37 V_{DC}, no TVS diode installed and mechanical relay (Dayton 6GNY4B)

The clamping energy that the GaN FET dissipates can be determined from the measured waveforms. The current at turn-off is 2.2 A, the clamping voltage is 77 V and total clamping time is around 3 ms, resulting in approximately 112 mJ of total clamping energy with peak power of 165 W. This example is shown in figure 12.

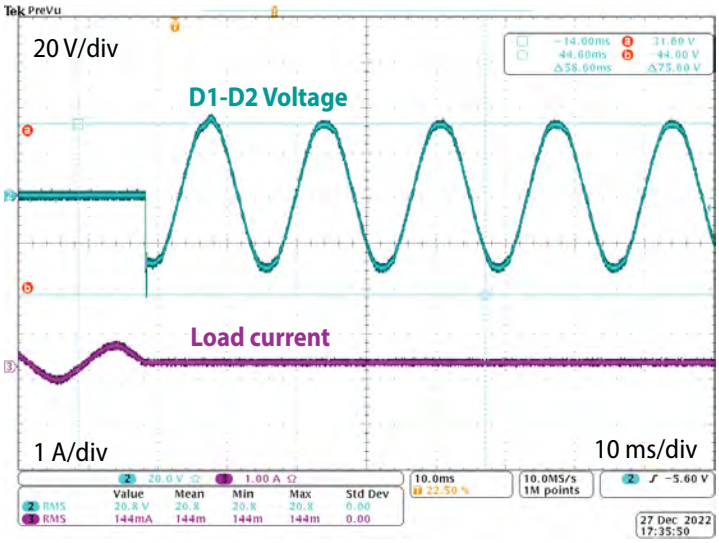
It should be noted that the junction temperature of GaN FET under these conditions can be exceeded as the power dissipated exceeds that recommended in the Safe Operating Area of the device. It is therefore important to design the circuit to turn off the mechanical relay with minimal current to reduce the turn off energy.

A similar test was repeated using an AC source with the measured results shown in figure 13. Due to the location of the turn-off, lower current was flowing in the relay at the time of turn-off resulting in lower turn-off current and hence the shorter time to dissipate the inductive energy.

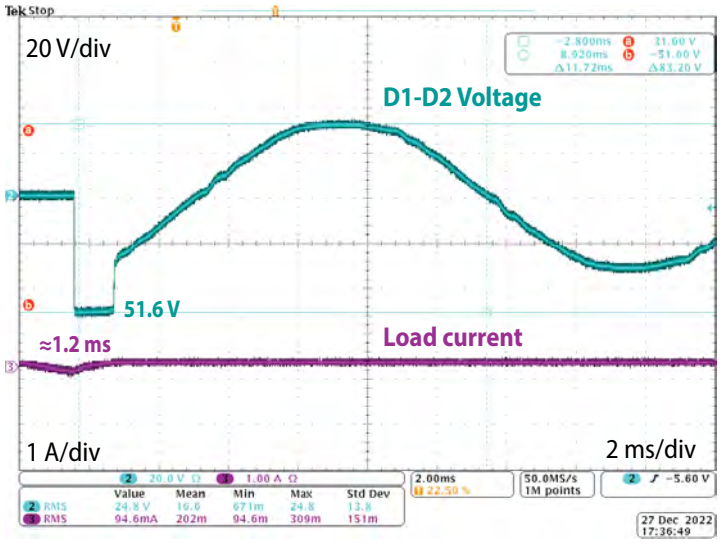


V_{Supply} = 37 V, P_{Avg} = 38.2 W, E_{OFF} = 112.3 mJ

Figure 12: Measured voltage, current and calculated power in the GaN FET with 37 V supply and turning off a Siemens 45EG20AJ Relay



Zoomed out



Zoomed in

Figure 13: AC inductive switching waveforms with 22 V_{AC}, no TVS diode installed and mechanical relay (Siemens 45EG20AJ), zoomed out (left) and zoomed in (right).

The AC test shows that selecting the correct time to turn off the relay can reduce the current at turn off and thus the energy and clamping time. In addition, a lower supply voltage can significantly reduce the energy dissipated by the eGaN FET as the source is a significant contributor to the total energy clamped by the eGaN FET. This can be achieved in AC systems by selecting to turn off the eGaN FET to occur around the zero voltage crossing point.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9182 landing page at: https://epc-co.com/epc/Products/Demo-Boards/EPC9182

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