Evaluation Board EPC9192KIT User Guide

2 x 700 W/4 Ω Class-D Amplifier

Revised April 4, 2024

Version 2.0

See page 14 for Quick Start

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9192KIT evaluation board is a reference design for an analog input, two channels, 700 W / 4 Ω, 1% THD+N per channel Class D audio amplifier. It showcases a compact Class D power stage with high power density, fitting within a volume of 60 cm^3 or 4 cubic inches. The evaluation board uses a ground referenced, split dual supply Single-Ended (SE) design, exploiting EPC's 200 V eGaN® FETs in a half bridge topology. The two channels can also be configured in Bridge-Tied-Load (BTL) mode , for up to 1400 W / 8 Ω.

EPC9192KIT is a modular design which allows scalability and expandability. The motherboard hosts two PWM modulators and two half bridge power stage daughterboards, implementing a two channels amplifier, including housekeeping supplies and protections. By customizing the PWM modulator, different modulation techniques can be implemented, as well as switching frequency can be changed. The power stage can also be customized, allowing the evaluation and comparison of different devices.

The EPC9192KIT comes with two EPC9558L PWM modulator boards, implementing an asynchronous switching, self-oscillating PWM modulator, with feedback taken after the L-C low pass filter (Post-Filter FeedBack, PFFB). Switching frequency is set to about 600 kHz. THD+N below 0.005% and SNR above 120 dB are achieved, and they can be further optimized. Also included is the EPC9558P power stage, built around two EPC2307, 200 V, 10 mΩ QFN eGaN® FET and the Onsemi NCP51820 gate driver. The board is shown in Figure 1.

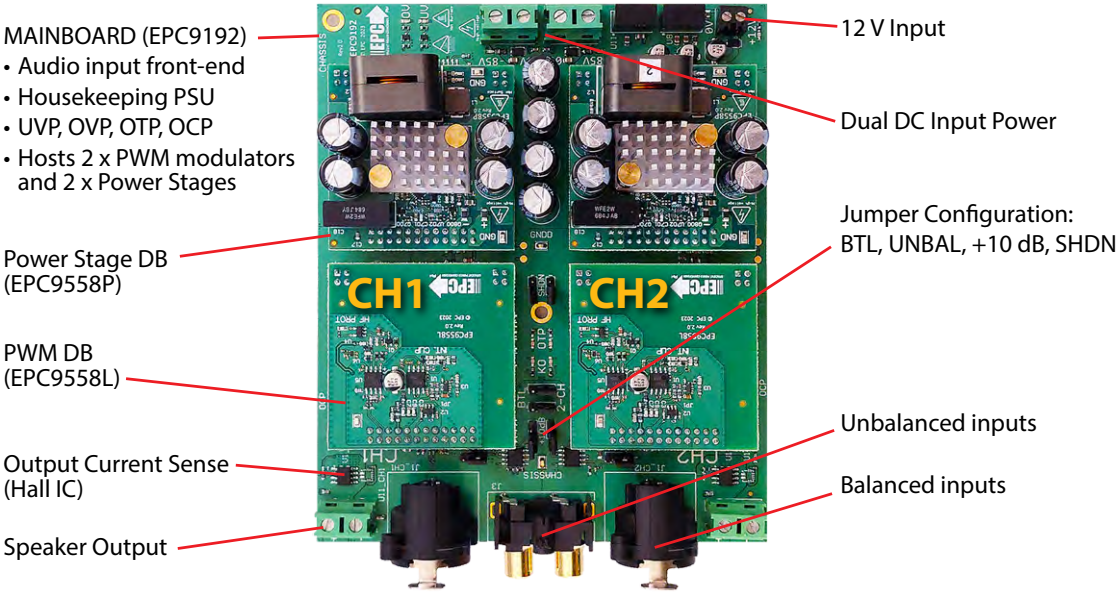


Figure 1: EPC9192KIT description

The EPC9192KIT demo board has about 96% efficiency at 350 W/8 Ω.

A functional block diagram of the EPC9192KIT evaluation board is shown in Figure 2.

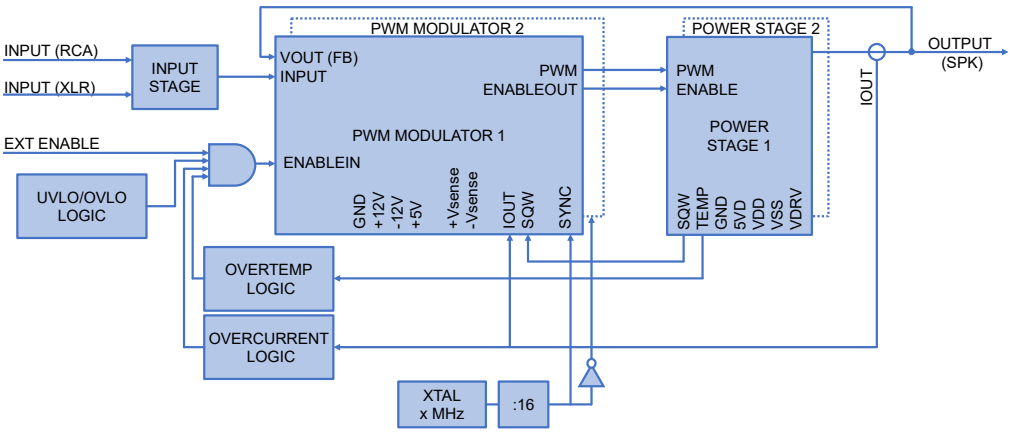


Figure 2. Block diagram of demo board EPC9192KIT

MAIN FEATURES

EPC9192KIT MOTHERBOARD

- Single regulated 12V power supply input for housekeeping (op-amps, gate drivers, etc.).
- Dual split supply input, unregulated, ±42 V to ±85 V for power stage
- Analog inputs balanced (XLR) or unbalanced (RCA)
- Input stage gain selectable -1.0 dB or +8.5 dB
- Two independent SE channels mode, or single channel BTL mode
- Undervoltage and Overvoltage protections
- Output current sense by Hall IC, with Overcurrent protection (immediate shutdown)
- Overtemperature protection
- Supports self-oscillating modulation schemes with feedback from the switching node and/or the output (post filter)
- Provision for clock generator to implement synchronous designs (not populated)

EPC9558L PWM MODULATOR DAUGHTERBOARD

- Self-oscillating design with post filter feedback, switching at about 600 kHz in idle
- > 40 dB loop gain at 20 kHz, resulting in low distortion and low output impedance
- Stable up to 0.2 µF purely capacitive loads
- Balanced input
- Fixed 20.8 dB gain
- Clipping indication
- Detection of instability and protection (shutdown)

EPC9558P POWER STAGE DAUGHTERBOARD

- Half bridge based on EPC2307, 200 V, 10 mΩ QFN eGaN® FET
- Onsemi NCP51820 gate driver, providing dead time control down to 30 ns
- PNP BJT based level shifter from ground to negative rail (low side FET source)
- 4 layers, 2 oz copper, components on top side only
- Low inductance layout, with vias in pad for PCB cooling
- Provision for push-pin mount heatsink for top cooling (included)
- 10 µH, > 40 A Isat off the shelf compact inductor (23x23x15 mm)
- EMI mitigation

RECOMMENDED OPERATING CONDITIONS

Table 1: Electrical Specifications (T_A = 25°C) EPC9192KIT

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{AUX}	Housekeeping power supply		10.8	12	13.2	V
V_{DD}	Positive input power supply		42		85	V
V_{SS}	Negative input power supply		-85		-42	V
I_{AUX}	Housekeeping supply input current	V_{OUT} = 0 V, V_{AUX} = 12 V, both channels operating		170		mA
$I_{DD, idle}$	Input power supply quiescent current	V_{OUT} = 0, V_{SS} = -70 V, V_{DD} = 70 V, both channels operating		50		mA
$I_{DD, shdn}$	Input power supply shutdown current	VSS = -70 V, V_{DD} = 70 V, both channels in shutdown		7		mA
P_{idle}	Power stage idle losses	V_{OUT} = 0, V_{SS} = -70 V, V_{DD} = 70 V, each channel		3.0		W
$f_{sw, idle}$	Idle switching frequency	V_{OUT} = 0, V_{SS} = -70 V, V_{DD} = 70 V	550	600	650	kHz
$f_{sw, min}$	Minimum switching frequency, clipping onset	V_{OUT} = ~70 V, V_{SS} = -70 V, V_{DD} = 70 V		70		kHz
V_{UVLO}	Input power supply undervoltage threshold			37		V
V_{OVLO}	Input power supply overvoltage threshold			95		V
I_{OCP}	Overcurrent trip point			45(1)		A
T_{OTP}	Overtemperature trip point			94		°C
t_{DT}	Dead time			50		ns
L_{LPF}	Low pass filter inductance			10		uH
C_{LPF}	Low pass filter capacitance			0.68		µF
P_{OUT}	Rated output power	V_{SS} = -85 V, V_{DD} = 85 V, 4 Ω load, 1% THD		700(2)		W
I_{OUT}	Output current	Peak current output for < 50 ms, limited by T_{J_MAX}			30	A
R_{LOAD}	Allowed resistive load		2	4	open	Ω
C_{LOAD}	Allowed capacitive load				0.2	µF

(1) Applies when Allegro ACS71240LLCBTR-045B5-S Hall sensor IC is installed (default). Alternate part is Monolithic Power Systems MCS1823GQTE-540BRN, whit trip point at nominal 40 A.

(2) Rated output power with heatsink assembled, 200 LFM airflow, and crest factor ≥ 6 dB (average power < 1/2 of rated). Maximum burst duration 2 s.

RECOMMENDED OPERATING CONDITIONS *(continued)*

Table 1: ***(continued)***

Symbol	Parameter	Conditions	Min	Nom	Max	Units
A_V	Input to output gain	Input stage gain setting = -1 dB, 1 kHz, 0 dBV output	19.6	19.8	20.0	dB
AV, BTL	Input to output gain, BTL mode	Input stage gain setting = -1 dB, 1 kHz, 0 dBV output	25.6	25.8	26.0	dB
$\|Z_{IN}\|$	Input impedance	XLR pin 2 and 3 to GND, or RCA tip to GND		9.2		kΩ
V_{IN}	Input voltage acceptance	XLR pin 2 and 3 to GND, or RCA tip to GND			10	Vpk
BW_{3dB}	Bandwidth at -3 dB	Any load	2		80 k	Hz
$BW_{0.5dB}$	Bandwidth at -0.5 dB	Any load	5		20 k	Hz
$\|Z_{OUT}\|$	Output impedance	20 to 20 kHz		8	30	mΩ
V_n	Output noise	20 Hz to 20 kHz, A-weighted, 4 Ω load, input stage gain setting -1 dB		40		µV
V_n	Output noise	20 Hz to 20 kHz, A-weighted, 4 Ω load, input stage gain setting +8.5 dB		60		µV
SNR	Signal to Noise Ratio	20 Hz to 20 kHz, A-weighted, 4 Ω load, input stage gain setting -1 dB		121		dB
THD	Total Harmonic Distortion	1 kHz, 10 W rated power, 4 Ω		0.005		%

DESIGN DESCRIPTION

Power Stage

The EPC9558P power stage is based on EPC2307, 200 V, 10 mΩ QFN eGaN® FET. For more information on the EPC2307 please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

The EPC9558P is a ground referenced PWM input to analog output half bridge, with dual split power supply. See block diagram in Figure 3.

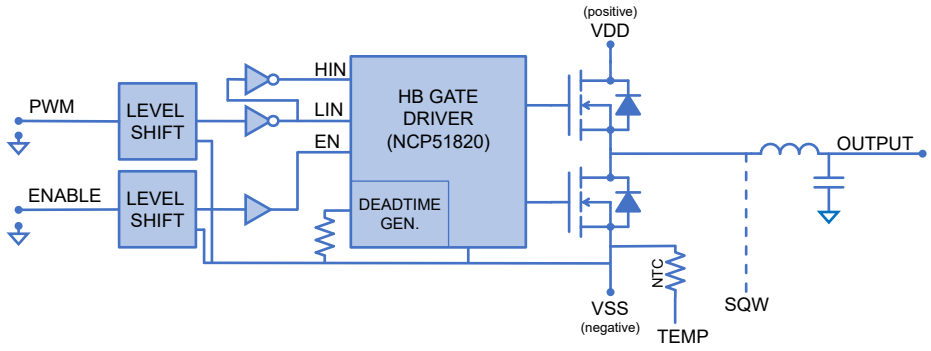


Figure 3. Block diagram of Power Stage EPC9558P

The gate driver is Onsemi NCP51820. It is configured in Mode B, internal dead time control. R86 sets the deadtime, 1 ns per kΩ, with a minimum of 30 ns. Included resistor is 49.9kΩ, for about 50 ns deadtime, which is chosen to achieve full ZVS at idle, and minimize the idle losses.

This gate driver was selected for the integrated LDOs for the gate drivers, which accepts from 9 V to 17 V input, while providing a precise 5.2 V supply to the gate drivers. This allows to use a bootstrap supply for the high side driver, with a wide range of duty cycle, and longer duration for 100% duty cycle. This duration is extended to > 50 ms by the R61/C62 network, allowing safe output clipping for extended period of time. Pre-bias is provided in order to minimize start-up glitch. The gate driver is referenced to the negative rail, so a level shifter is implemented to translate the PWM signal and Enable. It is based on a common base PNP BJT for the DC path, with a parallel speed-up capacitor.

Additional 1A 200V Schottky diode have been placed in parallel with the GaN FETs. They are meant to reduce the voltage drop when freewheeling during dead time, reducing both THD and losses in the GaN FETs.

The power stage includes the output L-C filter. It is based on off the shelf inductors for class-D audio. The recommended parts are 10uH, Codaca CFD2315FA-100M, or Providence Electronic Components THI-230230MZ-100. The capacitor is film, MKP, 0.68 µF 250V. Closest to the switching node, a small, high SRF molded inductor, in conjunction with an RC snubber, is used to mitigate radiated EMI .

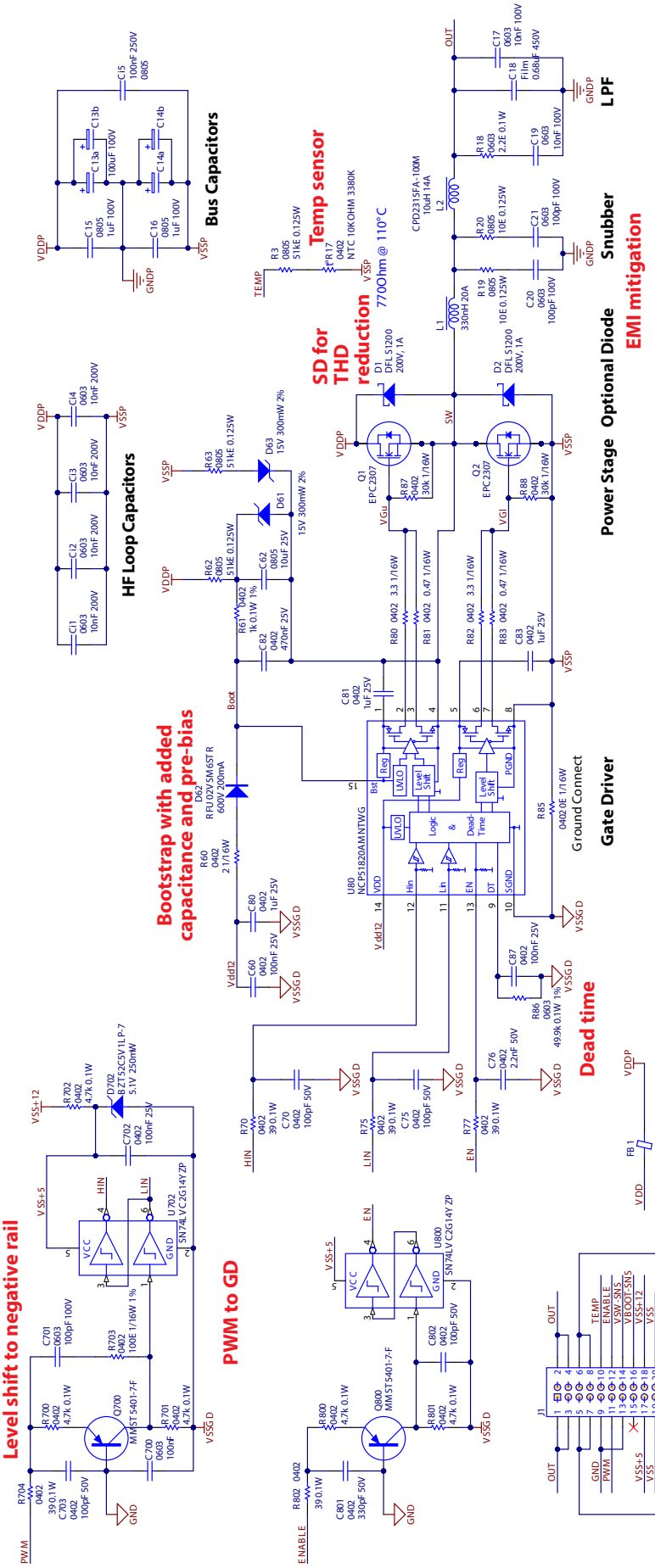


Figure 4. Simplified Power Stage Schematic

PWM Modulator

EPC9558L daughterboard implements the PWM modulator. It is based on a self-oscillating design, with an inner loop based on AC inductor current, and an outer loop based on output voltage. The design is inspired by previous work from Williamson (Carver) [1] and Veltman [2][3].

The AC inductor current is estimated by differentiating the voltage across the output capacitor (C7/C8 & R10/R13), and compared with a reference. The hysteresis provided by C3/C4 defines the allowed ripple in the inductor current, and together with propagation delay and some additional phase shift, defines the switching frequency. The inner loop reduces the gain dependency on the output filter and load, allowing a much higher loop gain in the outer loop, which defines the gain of the amplifier.

The outer loop is implemented as a second order integrator, with anti-windup by clamp D1/D2. Feedback loop gain is about 50 dB at DC (limited by R1) and 40 dB at 20 kHz, achieving low noise, low distortion and low output impedance across the audio band.

An inherent behavior of hysteretic based modulators is the switching frequency drop at high modulation index. Thanks to the 600 kHz idle frequency and high corner frequency of the L-C filter (60 kHz), the switching frequency does not fall below 70 kHz, at clipping onset.

Onboard Power Supply

There are the following power supply rails:

- AUX (+12 V): it is provided externally. It is used to power the audio opamps, and to power the other auxiliary supplies (-12 V, +5 V, V_{SS} + 12 V)
- -12 V: it is obtained from V_{AUX} by an isolated DC/DC module (Mornsun B1212S-1WR3),and it is used to power the audio opamps
- +5 V: it is obtained from V_{AUX} by an LDO. It is used to power the logic, the comparators and current sense ICs.
- V_{DD}: it is the high voltage positive power supply rail to the power stage. It is provided externally.
- V_{SS}: it is the high voltage negative power supply rail to the power stage. It is provided externally.
- V_{SS} + 12 V: it is obtained from V_{AUX} by an isolated DC/DC module (Mornsun B1212S-1WR3). It is 12 V referenced to the negative rail. It is used to power the gate driver of the power stage.

Regarding V_{DD} and V_{SS}, the external power supply is subjected to a very dynamic loading, with power peaks up to twice the rated amplifier power. The current ripple in the audio frequency band might cause regulation issues or even instability with some regulated power supplies. The onboard bulk capacitance mitigates this problem, but it is limited to 600 µF. It might be required to add and external capacitor, i.e. 3300 µF per rail.

Protections

The EPC9192KIT mainboard implements UnderVoltage, OverVoltage, OverTemperature and OverCurrent protections. When engaged, the action is pulling low the Enable input of the gate driver, placing the power stage half bridge in high impedance within a few µs. A timing circuit with auto retry will reset the protection after about 2 seconds, and is also responsible for the start-up delay.

An independent protection is implemented on the modulator DB, by comparing the high frequency components of the input with the scaled output. If they don't match, an instability issue is detected, and the output stage is disabled.

Current Sense & OCP

Current is sensed on the speaker output terminal, by using an Hall sensor IC. Allegro ACS71240LLCBTR-045B5-S Hall sensor IC is installed by default. Provision is made for Monolithic Power Systems MCS1823GQTE-540BRN. Both ICs implement also an overcurrent detection comparator.

The current measurement is AC coupled and fed to the modulator DB (pin 10 of J5). It can be used to monitor the output current or to implement custom overload protections.

Table 2

Manufacturer	Part number	Package	Current scale factor	Overcurrent limit
Allegro Microsystems	ACS71240LLCBTR-045B5-S	QFN	44.4 mV/A	45 A
Monolithic Power Systems	MCS1823GQTE-540BRN	SO-8	50 mV/A	40 A

Temperature sense & OTP

The temperature is sensed by a 0402, 10 kΩ, 3380K NTC thermistor (TDK NTCG103JF103FT1). One terminal is soldered very close to the source of the low side FET (negative rail V_{SS}), to minimize the time delay and the temperature difference between FET and NTC. Simplified schematic is shown in Figure 5. Similar to a difference amplifier, the voltage at the fixed reference divider (R5, R19a, R19b, R16) is compared with the voltage at the measurement divider, dependent of the NTC sensor (R17, R3, R18, R15). Neglecting the hysteresis provided by R13 (about ±4 °C), the overtemperature trip point is when NTC resistance equals R19b, or about 92 °C, being all the other resistors matched (R15 = R16, R18 = R19a, R3 = R5).

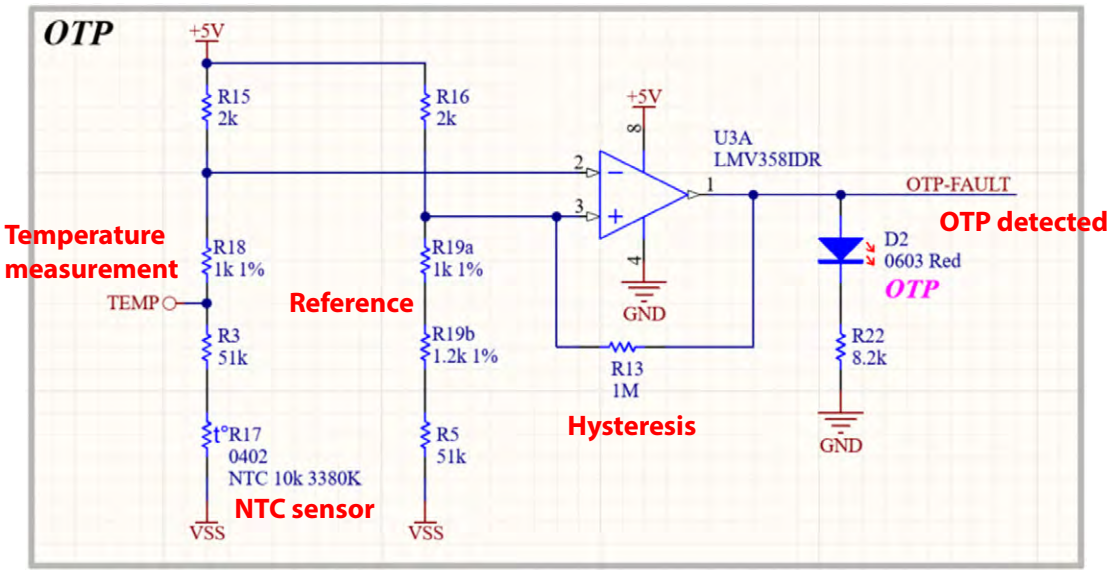


Figure 5 – Overtemperature protection simplified schematic

Temperature Sense & OTP

The temperature could in principle be monitored by measuring voltage between 5V (pin 20 of J5) and TEMP (pin 9 of J7), but due to the strong dependency on V_{SS} and the high dividing factor due to R3, it isn't very accurate. A better measurement can be extracted by measuring between TEMP (pin 9 of J7) and the node marked "Reference." Figure 6 shows the two voltages at three different VSS values of -48 V, -70 V and -85 V. The blue plot represents the logic status of the OTP protection. The trip point is slightly dependent on V_{SS}, and it is lower at higher V_{SS}.

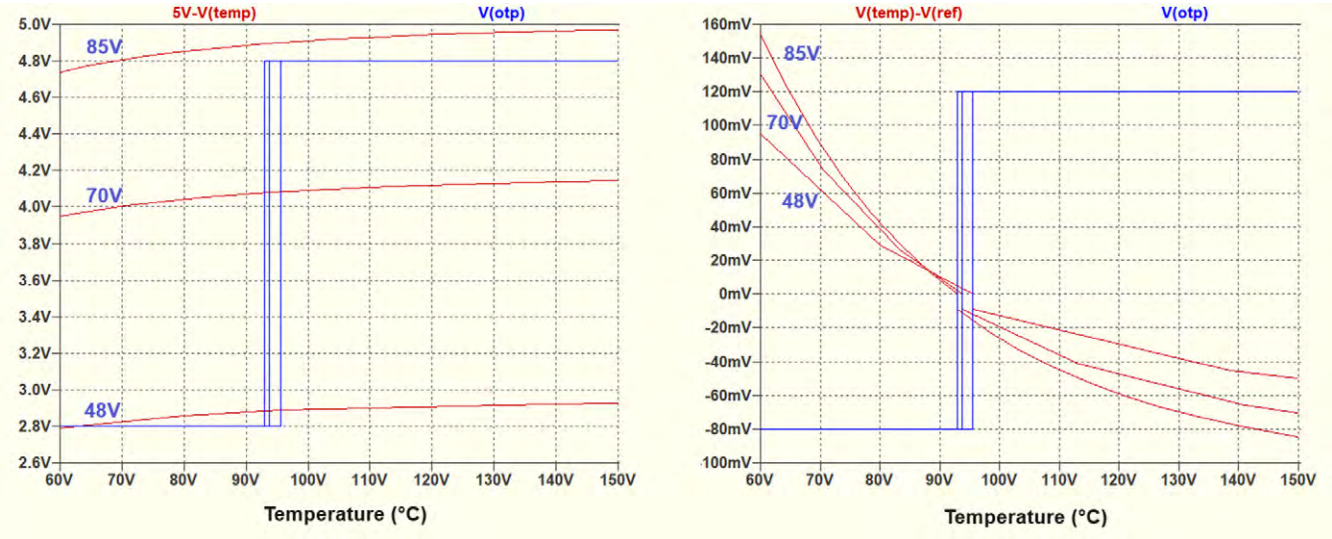


Figure 6 – Temperature sensing monitoring

Audio Inputs

There are two XLR connectors, that work as balanced inputs. For each of them, the input stage is a DC-coupled unity gain buffer, that can be also set as a 3x voltage gain amplifier by shorting jumper J2. In front of it, a simple passive R-C lowpass filter, with cutoff frequency at 500 kHz, prevents RF signals to reach the op amps. The output of this buffer is fed to a single op-amp difference amplifier, with 1st order cutoff at 100kHz, located on the PWM modulator board. The combination of those two stages implements a 3 op-amp differential amplifier.

The two RCA/Phono connectors are used as unbalanced inputs. The central pin is tied to the non-inverting input of the balanced input, right at the XLR connector pin 2. The outer contact is connected to the inverting input of the balanced input, XLR connector pin 3, and it can be also shorted with a jumper to EPC9192KIT ground by means of a 10 Ω / 100 nF network .

TEST POINTS

The most relevant signals can be found in the daughterboards headers.

In the PWM Modulator daughterboard header there are the signals shown in Figure 7.

Table 3

Pin #	Pin name		Pin #
2	AGND	AGND	1
4	IN-	IN+	3
6	AGND	AGND	5
8	ENABLEIN	VOUT	7
10	IOUT	GND	9
12	ENABLEOUT	PWM	11
14	VSS-SNS	VDD-SNS	13
16	SYNC	SQW	15
18	GND	12VN	17
20	12VP	5V	19
22	SPARE	SPARE	21
24	SPARE	SPARE	23

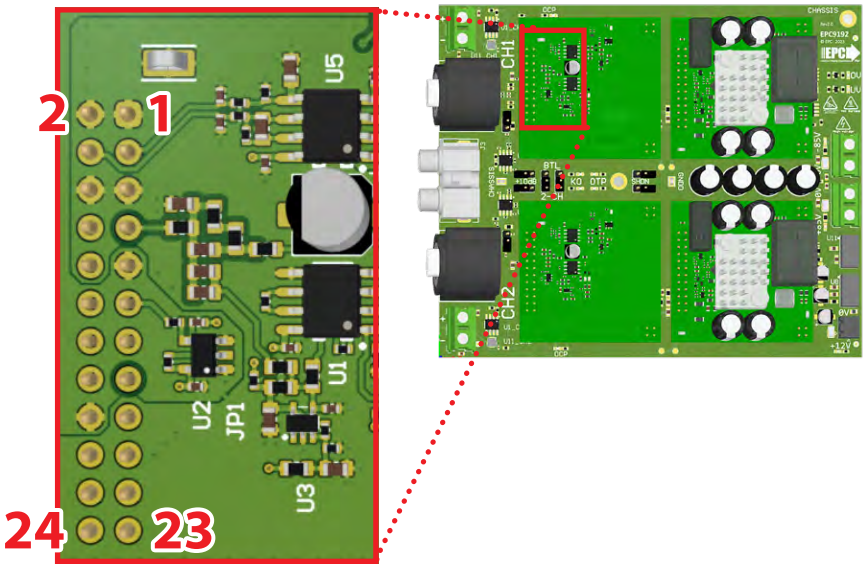


Figure 7 – PWM Modulator daughterboard signals

Signal description:

- **AGND**: audio ground
- **IN–, IN+**: inverting and not–inverting audio inputs to PWM modulator
- **ENABLEIN**: enable from motherboard
- **VOUT**: feedback from output connector
- **IOUT**: measured output current from Hall sensor
- **GND**: ground
- **ENABLEOUT**: enable to power stage
- **PWM**: digital PWM signal to power stage
- **VSS–SNS**: sense of negative supply rail, 13.2 V/V scale
- **VDD–SNS**: sense of positive supply rail, 13.2 V/V scale
- **SYNC**: square wave sync from motherboard oscillator (not mounted on motherboard)
- **SQW**: feedback from half bridge switching node (not connected on power stage DB)
- **12 VN, 12 VP**: –12 VDC and +12 VDC supply to opamps
- **5V**: +5 VDC supply to logic

In the Power Stage daughterboard header there are the signals shown in Figure 8.

Table 4

Pin #	Pin name		Pin #
2	OUT	OUT	1
4	OUT	OUT	3
6	AGND	AGND	5
8	AGND	AGND	7
10	TEMP	GND	9
12	ENABLE	PWM	11
14	SQW	GND	13
16	VBOOT	SPARE	15
18	VSS+12	VSS+5	17
20	VSS	VSS	19
22	PGND	PGND	21
24	VDD	VDD	23

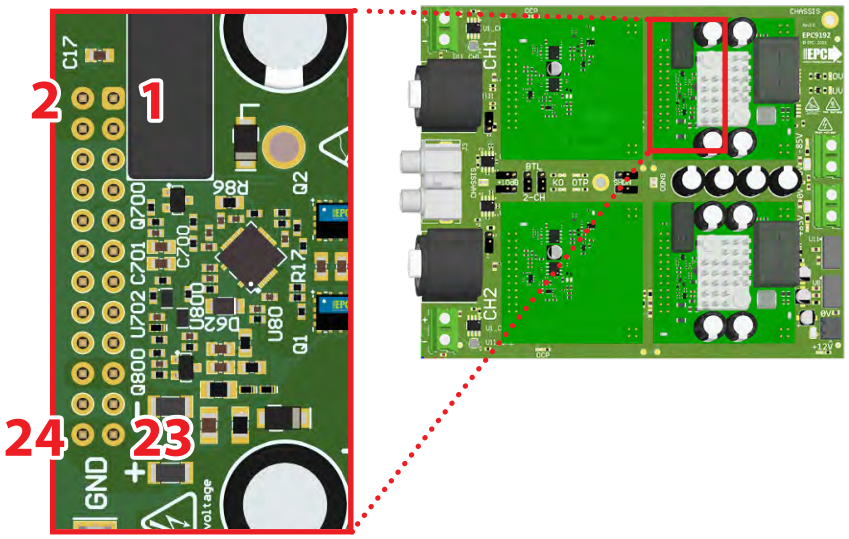


Figure 8 – Power Stage daughterboard signals

Signal description:

- **OUT**: audio power output
- **AGND**: audio ground
- **TEMP**: NTC temperature sense (offset by negative rail)
- **GND**: ground
- **ENABLE**: enable input from PWM modulator ENABLEOUT
- **PWM**: PWM input from PWM modulator
- **SQW***: feedback from half bridge switching node
- **VBOOT***: floating gate drive power supply
- **VSS+12**: 12 VDC supply referenced to negative rail, powers the gate driver from motherboard
- **VSS+5**: 5 VDC supply referenced to negative rail (generated on POWER DB, not supplied by motherboard)
- **VSS**: negative rail power supply from motherboard
- **PGND**: power ground
- **VDD**: positive rail power supply from motherboard

** Disconnected by R1 and R2, by default not populated*

To measure the switching node, we suggest the pick-up point and method as shown in figure 9. An example waveform, taken at 20 A output current, driving a 2 Ω load, is shown in Figure 10. In hard switching (rising edge with positive output current, or falling edge with negative output current), some reverse recovery sign from the parallel Schottky diode is visible at currents above about 10 A. Evaluation of the board with no Schottky diodes installed, and shorter dead time is pending.

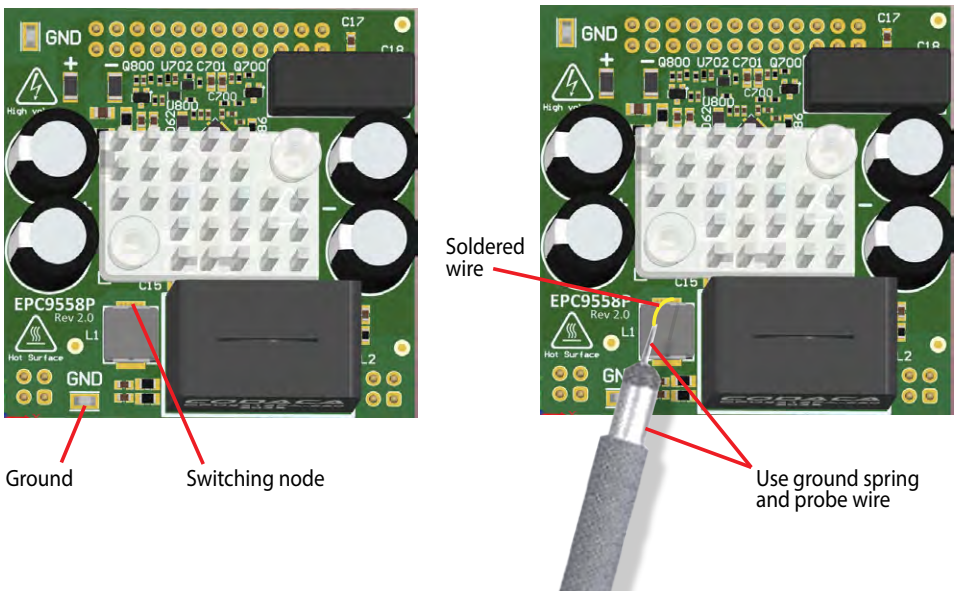


Figure 9 – Switching node waveform measurement

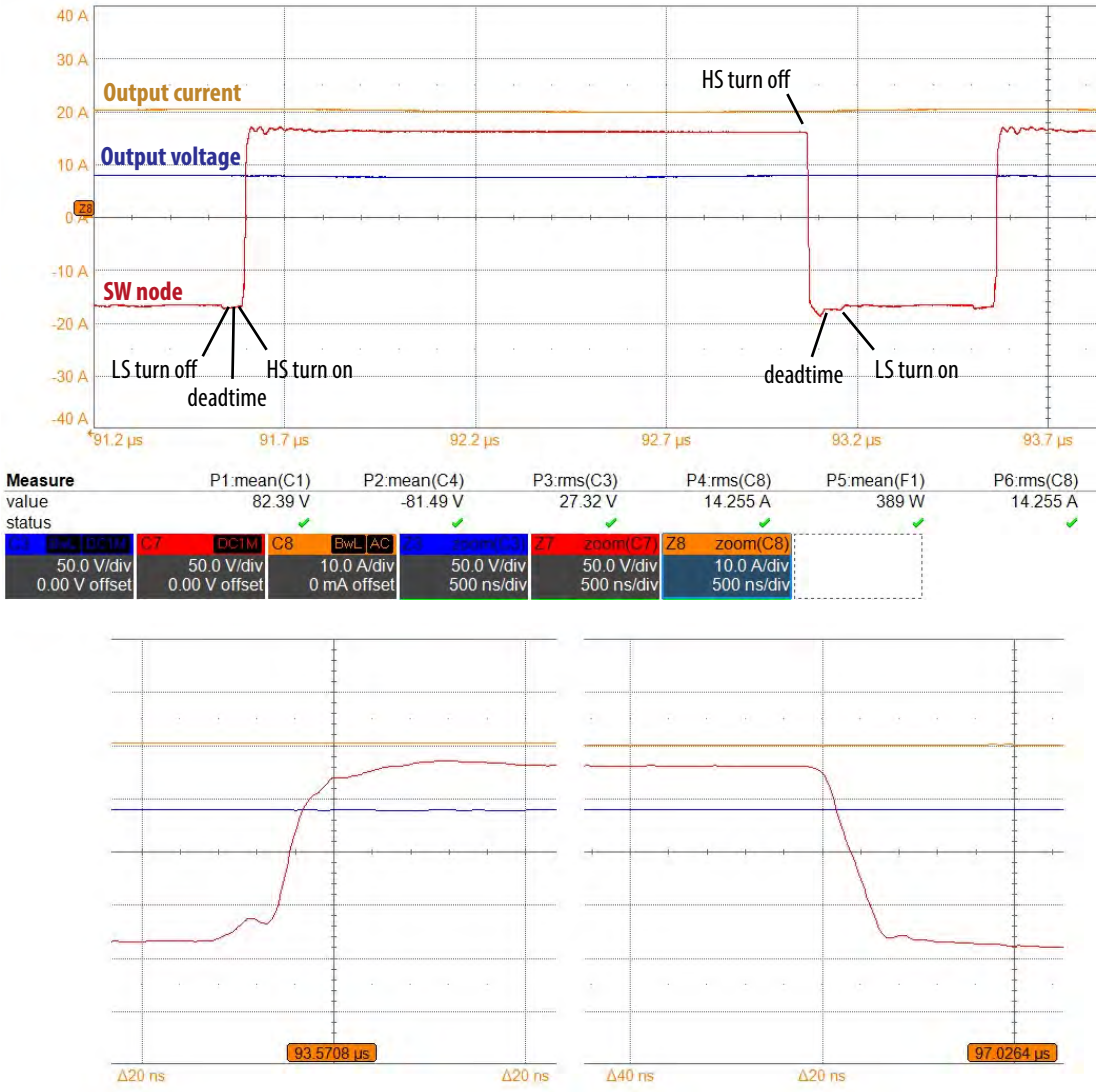


Figure 10 – Example waveforms at 20 A output, with zoom on switching node voltage edges.

THERMAL DESIGN

The cooling design has been optimized for both bottom cooling and top cooling, and is shown in Figure 11.

Bottom cooling is enhanced by the following precautions:

- Using 2 oz copper thickness in the 4 layers PCB
- Using middle caps layout to spread out the FETs and provide symmetrical cooling
- Using vias in pad plated over (VIPPO), and fitting 48 for each FET. About half of them are connected to a copper polygon in the first inner layer, crossing only 0.2 mm in the thickness direction. The other half are crossing the full PCB thickness of 1.6mm, and connected to wide copper polygons in the bottom side.
- A 1206 copper jumper (Keystone 5109) is soldered very close to drain terminal of each FET. It helps to spread the heat on PCB and increase the contact surface to the top mounted heatsink

EPC9192KIT comes with the heatsink installed. Top cooling is implemented by:

- Using high conductivity TIM gap pad, with 0.5 mm thickness, to minimize die to heatsink thermal resistance. Suggested materials are: T-Global TG-A1780 (17.8 W/mK), Shiu Li Technology T-work9000 (20 W/mK). Size is 15 x 10 mm.
- Adding custom heatsink Alpha Novatec S08FKE03. Heatsink is compressed on TIM by spring loaded push-pins. Pressure on TIM is about 50 psi. The minimum standoff of the heatsink is set to about 1 mm by four diodes (the two freewheeling in the bottom center, and the two dummies in the top corners), which also provides stability to the heatsink.

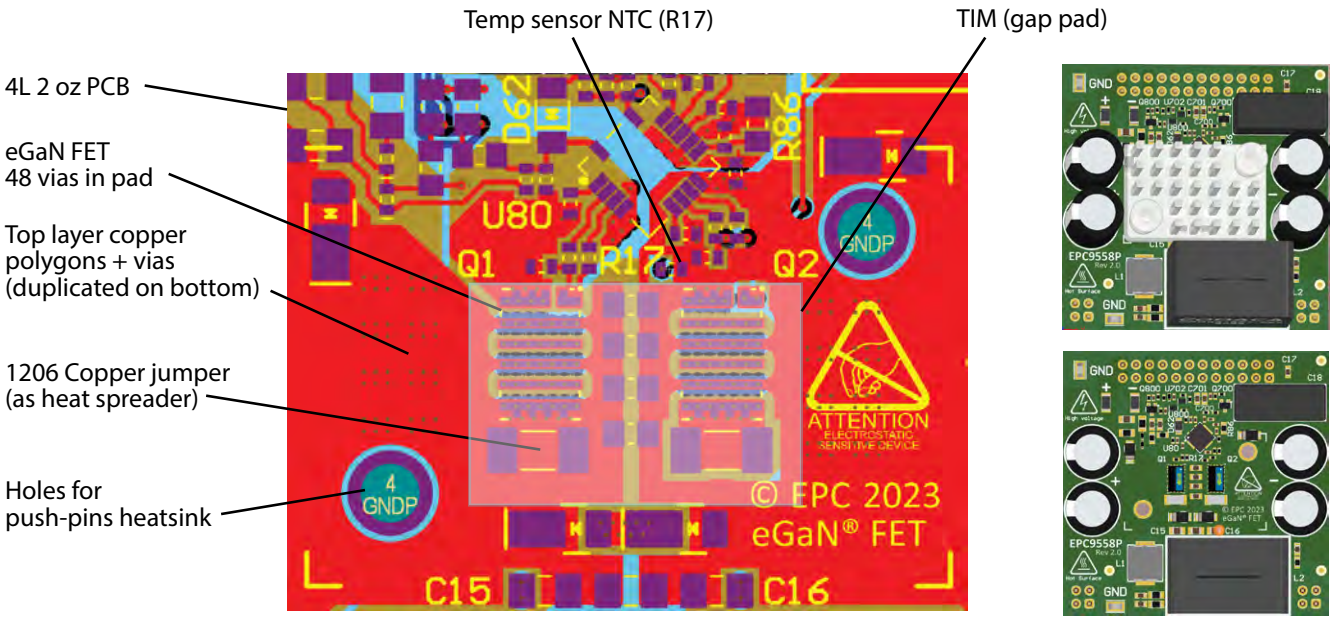


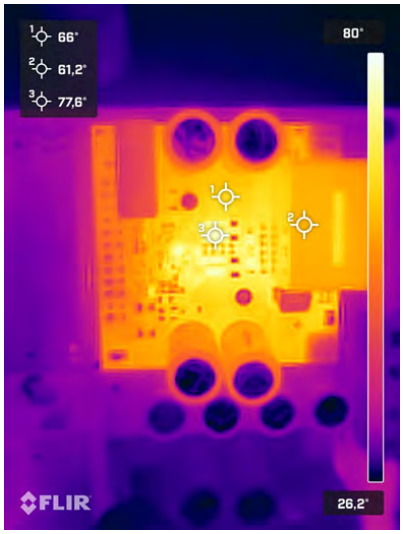
Figure 11 – Cooling solution implemented

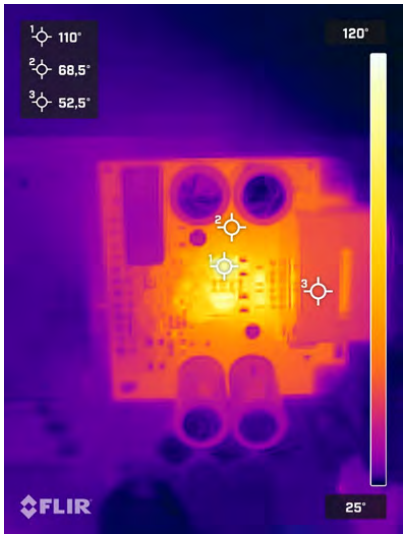
Depending on supply voltage and RMS output current, the board can be operated with or without heatsink, and with forced air or convection cooling. Some examples are provided below.

Table 5

Heatsink	Ventilation	Power Supply	Output Current	Power / Load, Crest Factor	Figure 13
Without	Natural	± 48 V	4 A_{RMS}	125 W / 8 Ω, 3 dB CF (sine) 250W / 4 Ω, 9 dB CF	(a)
Without	200 LFM	± 70 V	5 A_{RMS}	200 W / 8 Ω, 3 dB CF 400 W / 4 Ω, 9 dB CF	(b)
Installed	Natural	± 70 V	5 A_{RMS}	200 W / 8 Ω, 3 dB CF 400 W / 4 Ω, 9 dB CF	(c)
Installed	200 LFM	± 82 V	10 A_{RMS}	350 W / 8 Ω, 3 dB CF (sine) 700 W / 4 Ω, 6 dB CF	(d)

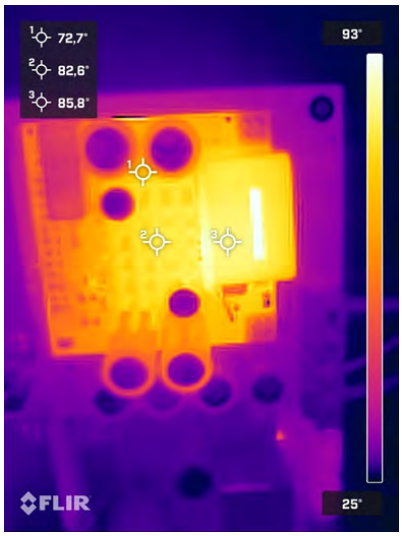
(a)

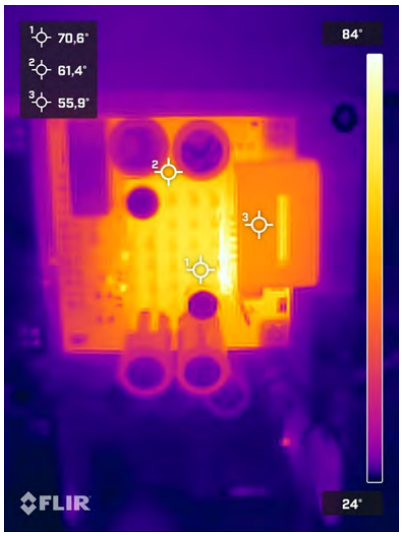




(b)

(c)



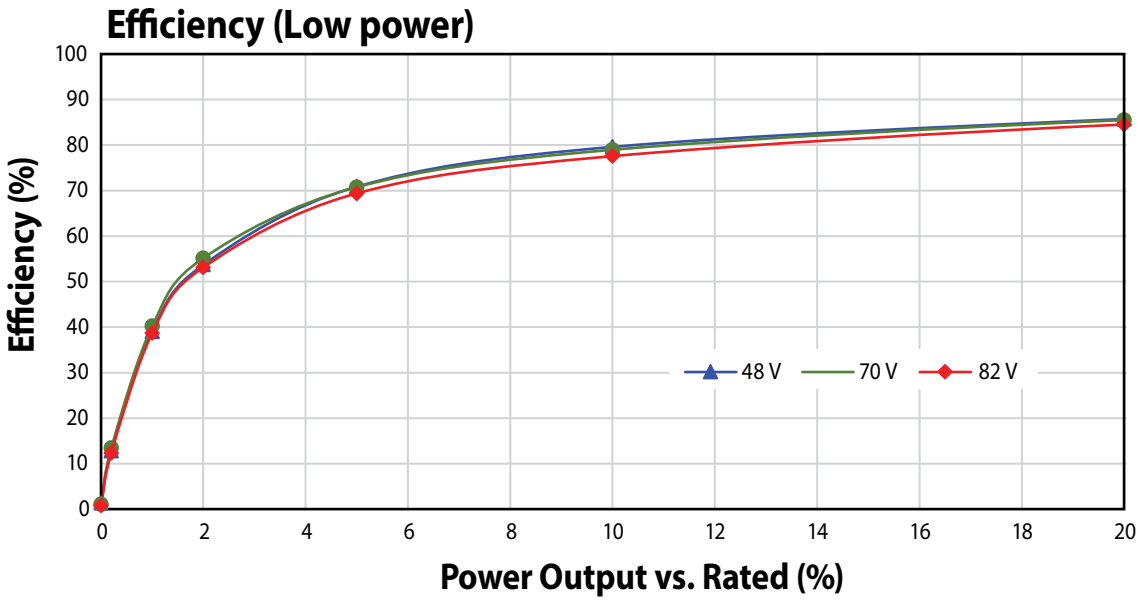


(d)

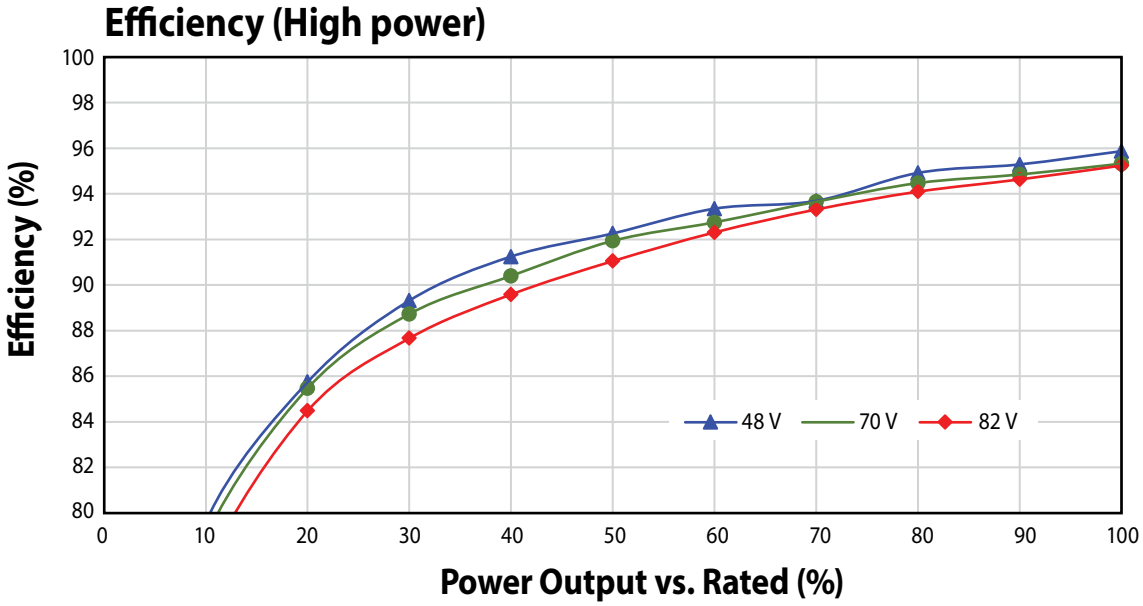
Figure 12 – Thermal images taken at various operating conditions.
(a) ±48 V supply, no heatsink, natural convection, 4 A_{RMS} output
(b) ±70 V supply, no heatsink, 200 LFM forced cooling, 5 A_{RMS} output
(c) ±70 V supply, heatsink, natural convection, 5 A_{RMS} output
(d) ±82 V supply, heatsink, 200 LFM forced cooling, 10 A_{RMS} output

EFFICIENCY

Efficiency has been measured for various supply voltages at varying output power, on 8 Ω load. Measurements on 4 Ω load are pending. Figure 13a shows efficiency in the low output power region (lower or equal than 20% of nominal power output), while Figure 13b shows efficiency in the high output power region (higher than 20% of nominal power output).



(a)



(b)

Figure 13 – Efficiency vs. Output Power of GaN transistor-based class-D amplifier in the low power range (a) and high power range (b) at ±48 V, ±70 V and ±82 V supply voltage.

USING THE BOARD

To operate the board, please follow one of the wiring diagrams in Figure 14.

Be aware that using a loudspeaker as a load can result in dangerous sound pressure levels. It is your responsibility to protect your ears.

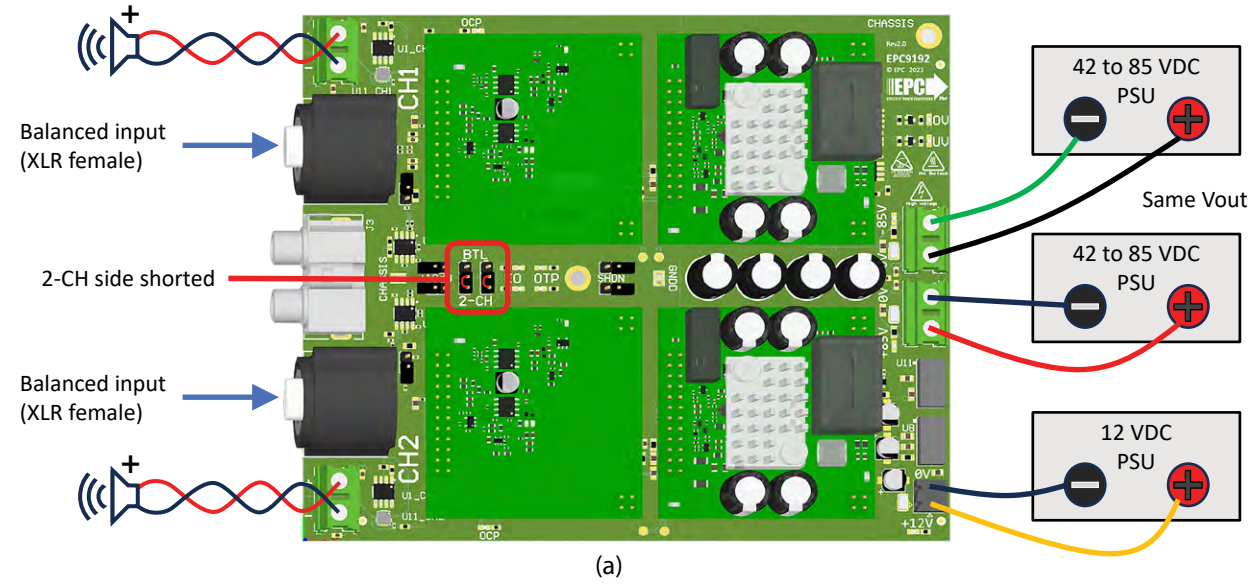
Power supply sequencing is not important, but the safest is to turn on first the 12 V housekeeping supply, and then the dual power supply for the high voltage rails. For turn off, use opposite sequence.

Power supplies should be rated accordingly, and capable of at least 2 times the output power for short term.

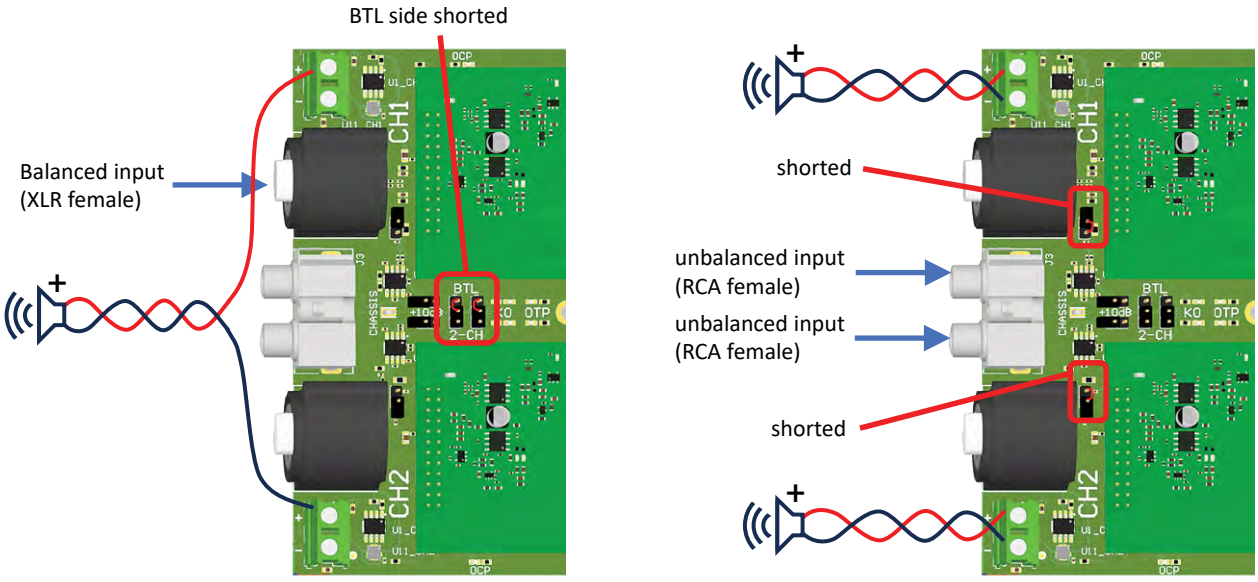
Purely capacitive loads above 0.2 µF are not supported, resulting in instability and automatic shutdown.

Please note that, due to a specific feature of the NCP51820 gate driver, the self-oscillation is started only if an input signal is applied.

The onboard bulk capacitance is 600 µF for each rail. Some power supply might not be able to regulate the voltage when delivering low frequency output, due to the ripple current. Please monitor the supply rails with a scope to ensure it is stable during operation. It is a good practice to add external bulk capacitors (i.e. 3300 µF per rail). During efficiency measurement tests, two electrolytic capacitors, 2200 µF / 100 V have been added in parallel to the high voltage power supplies as energy buffer for the amplifier, and to reduce the current ripple loading the PSUs.



(a)



(b) (c)

Figure 14 – Wiring diagrams to operate the board. (a) Balanced inputs, 2 channels. (b) Balanced input, BTL mode. (c) Unbalanced inputs, 2 channels mode (BTL mode also possible).

SETTINGS JUMPERS

There are a few jumpers to change the operating modes of the board, as shown in Figure 15:

A. "SHDN": J6, shorting this jumper will stop operation (output stage not switching)

B. "+10 dB": J2, if open, gain is 19.6 dB; if shorted gain is 30 dB

C. "BTL / 2-CH": J12 and J13

- if both jumpers are shorting the center pin to the "BTL" side, the CH2 will be driven by an inverted version of CH1 input. BTL load is between the + terminal of the two output terminal blocks. Gain will be increased by 6 dB.
- if both jumpers are shorting the center pin to the "2-CH" side, the two channels will operate independently. Two single ended loads are between the + and – of the two output terminal blocks.

D. "UNBAL GND": J4, it needs to be shorted when using unbalanced RCA inputs, and open when using balanced XLR inputs. It shorts the RCA outer contact (signal source ground) to the EPC9192KIT ground, by means of a 10 Ω / 100 nF network.

LED INDICATORS

The operating status of the board is reported by several LEDs, as shown in figure 3:

1. "OCP": turns on when overcurrent is detected
2. "KO": lit if any fault is preventing operation, including "SHDN" jumper shorted
3. "OTP": lit if overtemperature protection
4. "OV": lit if overvoltage detected
5. "UV": lit if undervoltage detected
6. "INT. CLIP": lit if excessive feedback loop error (integrator clipping), i.e. when overdriven or not operating ("KO")
7. "HF PROT": lit if HF oscillation detected (feedback loop instable), i.e. because of excessive capacitive loading.
8. "POWER": on if power supply is present (V_{AUX}, V_{DD}, V_{SS})

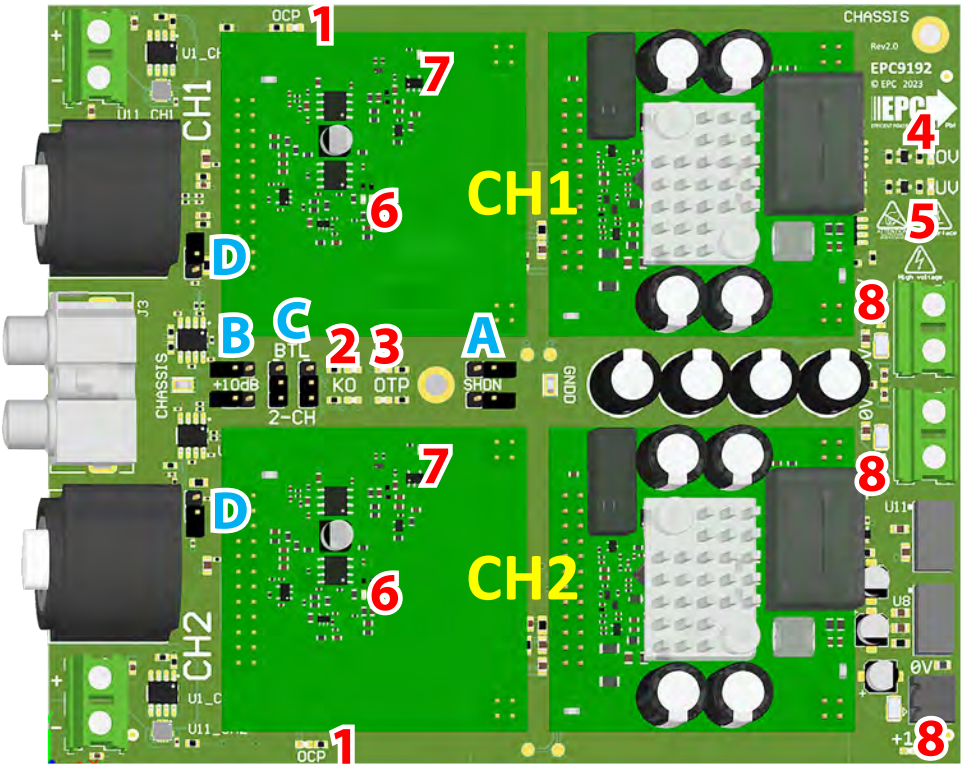


Figure 15 – Settings jumpers (blue) and indication LEDs (red)

AUDIO MEASUREMENTS

Audio measurements setup

Audio measurements have been carried out with the setup shown in Figure 16. The audio analyzers Audio Precision APx515 and APx525 have been used for the measurements, using balanced connections for the inputs and outputs. Please note that Kelvin connection of the analyzer to the terminals of the output connector of EPC9192KIT is required. The purpose is to minimize the measurement error due to the voltage drop in the cabling connecting the resistive load to the amplifier.

The high voltage PSU is a regulated LLC with +85 V, -85 V nominal outputs, specifically designed for powering audio amplifiers, capable of more than 1500 W. It was powered directly from mains (230 VAC, 50 Hz), and it used 4400 µF capacitance as filtering in each of the outputs.

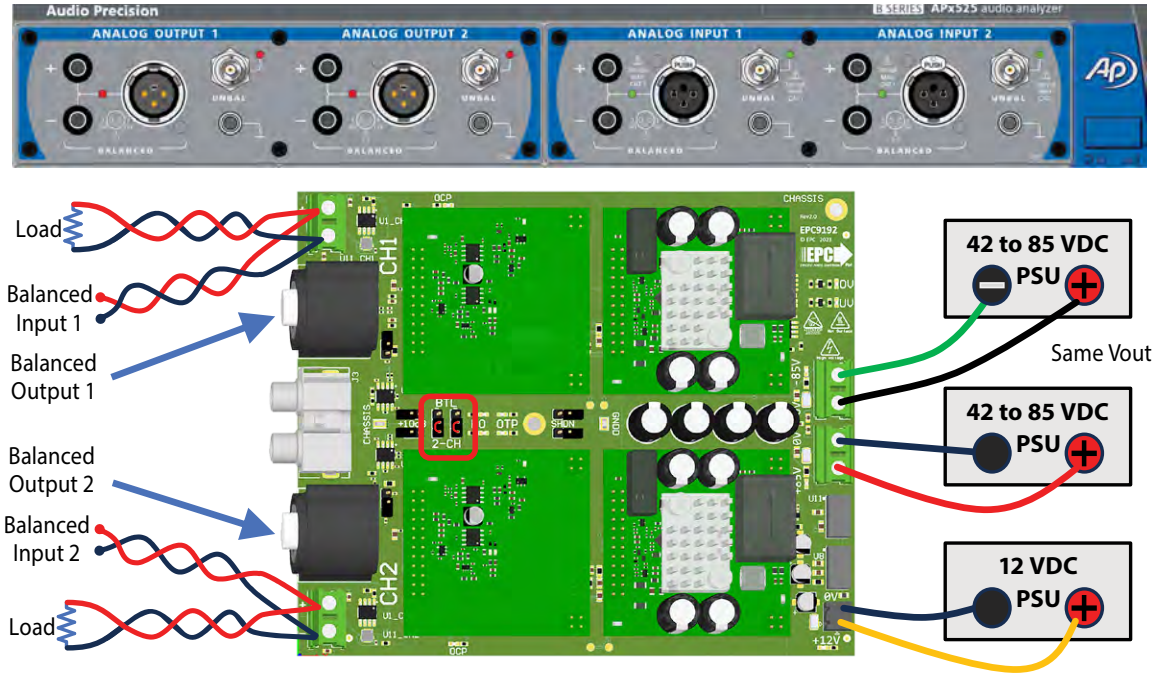


Figure 16. Audio measurement setup

Audio measurements results

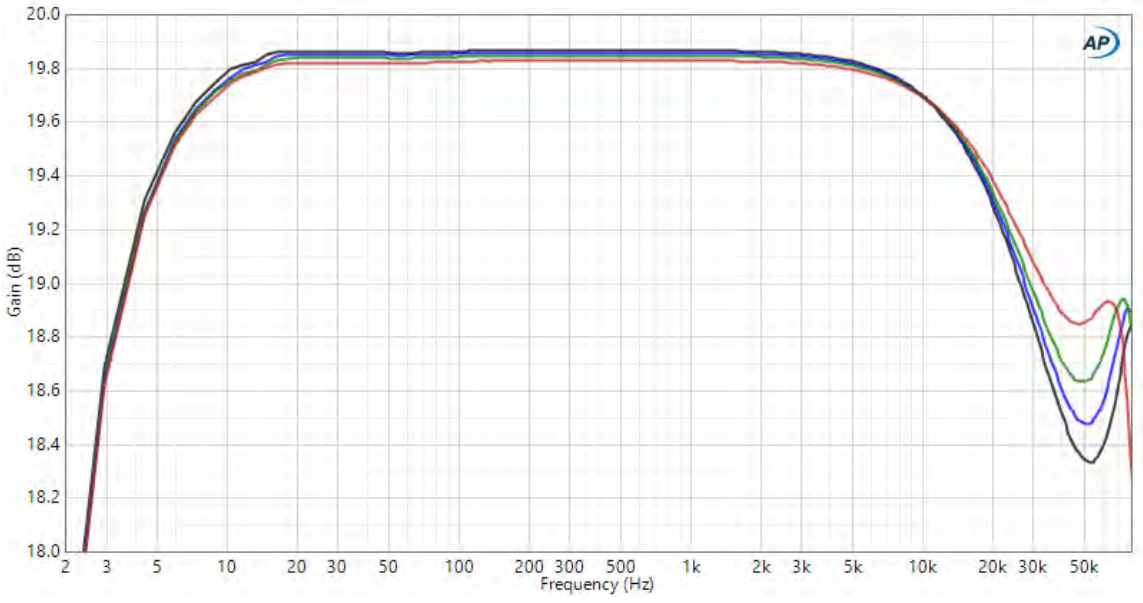


Figure 17 - Frequency Response at 2 V_{RMS} output, on open load (black), 8 Ω load (blue), 4 Ω load (green), 2 Ω load (red)

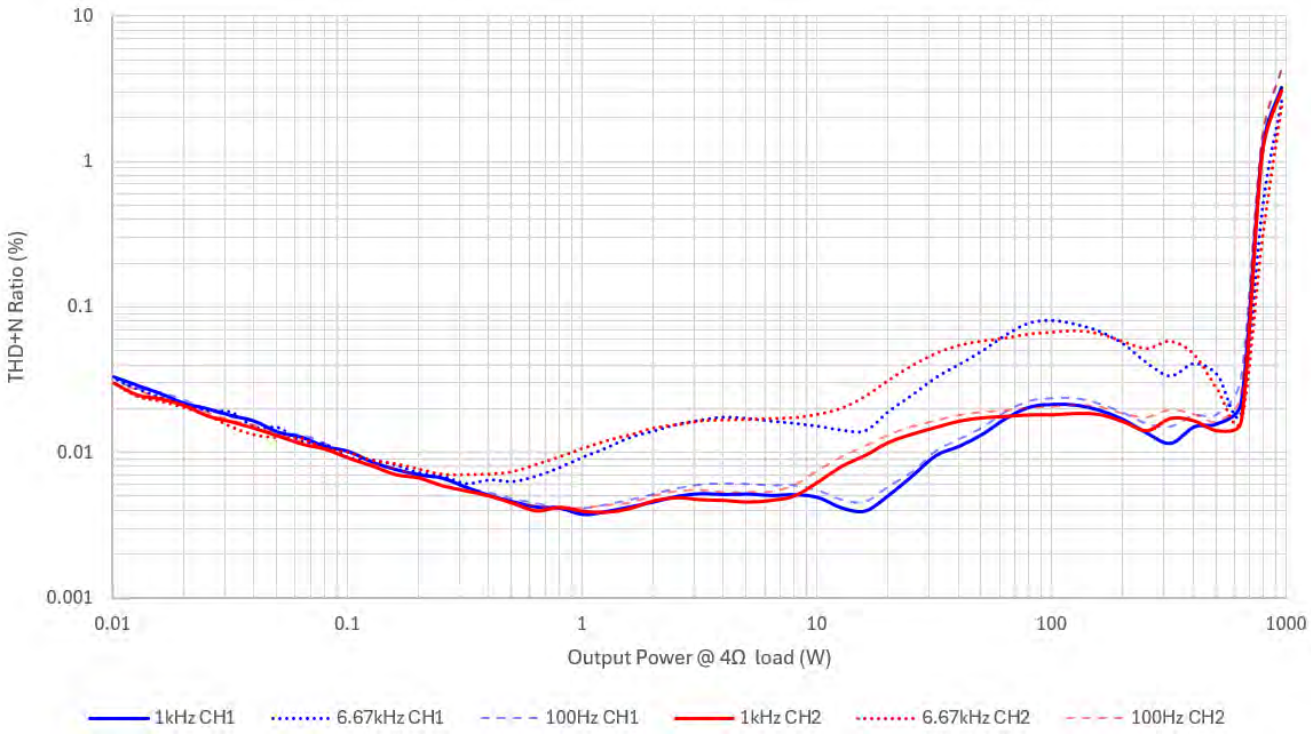


Figure 18 - THD+N vs. Output Power Level, 4 Ω load

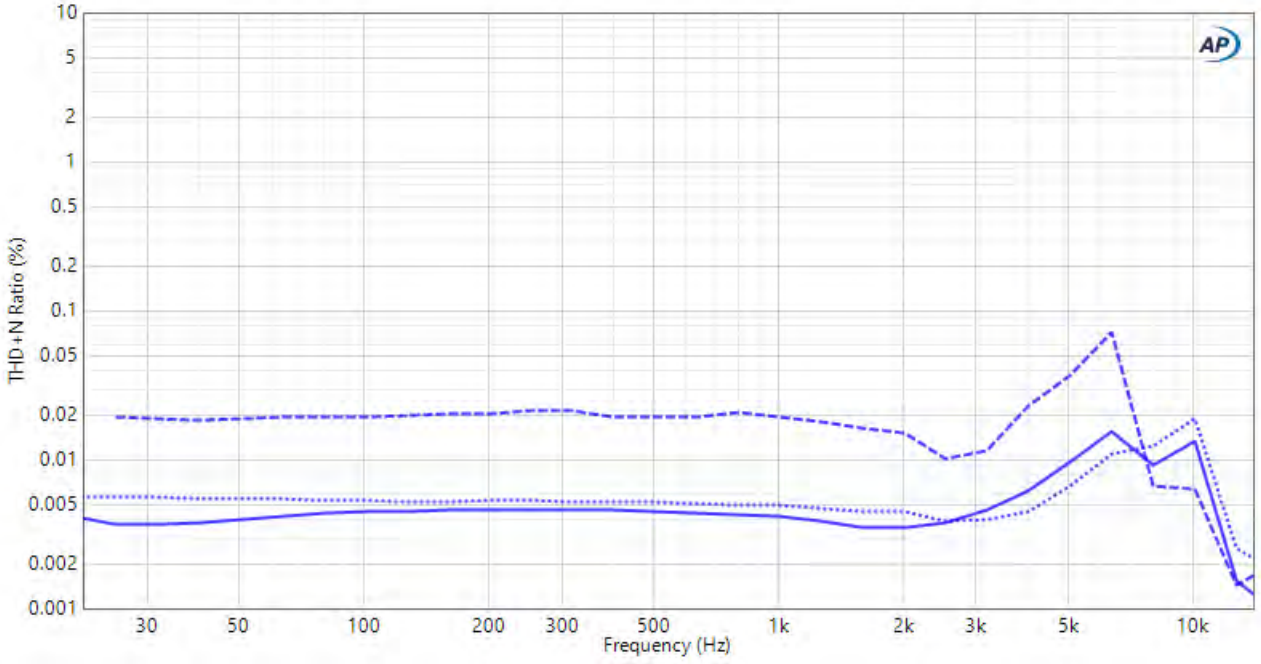


Figure 19 - THD+N vs. Frequency, at 1W (solid), 10W (dotted), 100W (dashed), 4 Ω load

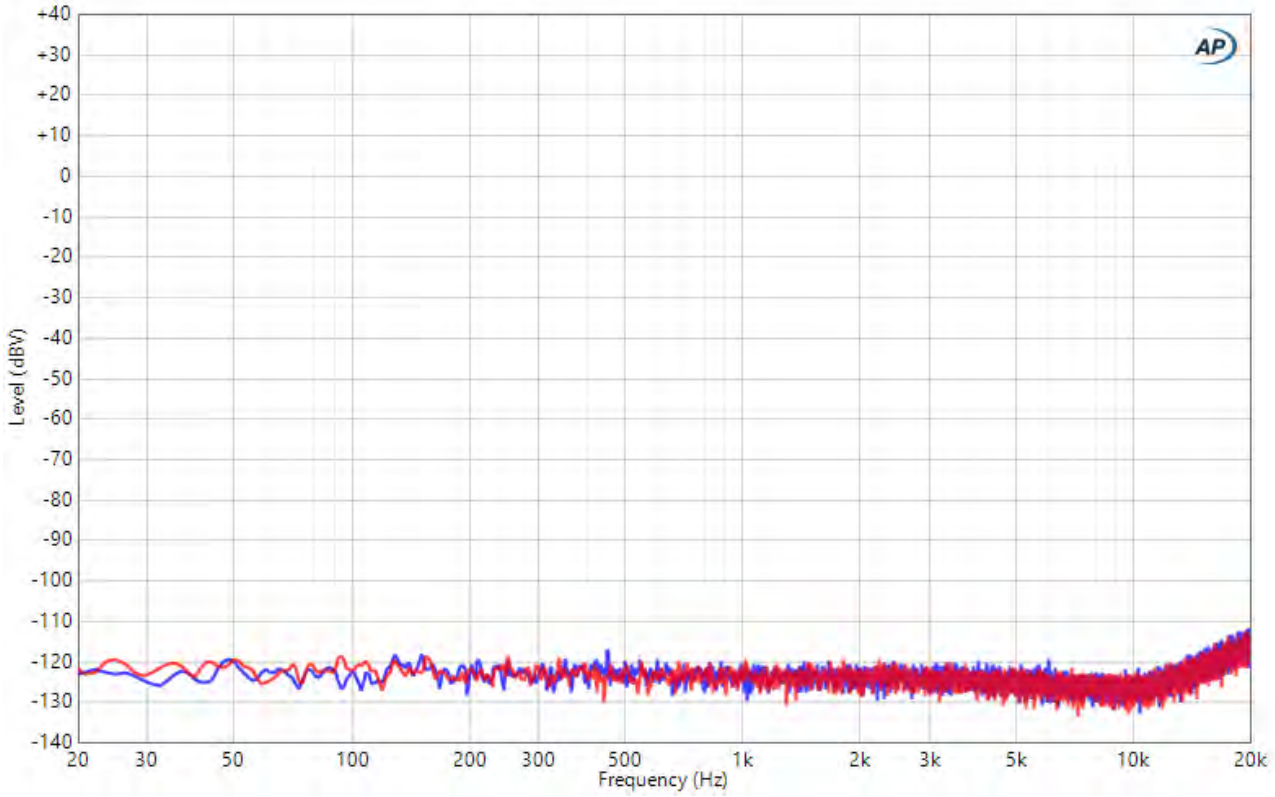


Figure 20 – FFT (32 k samples, F_s = 48 kHz), no signal input, 4 Ω load = 38 µV(A)

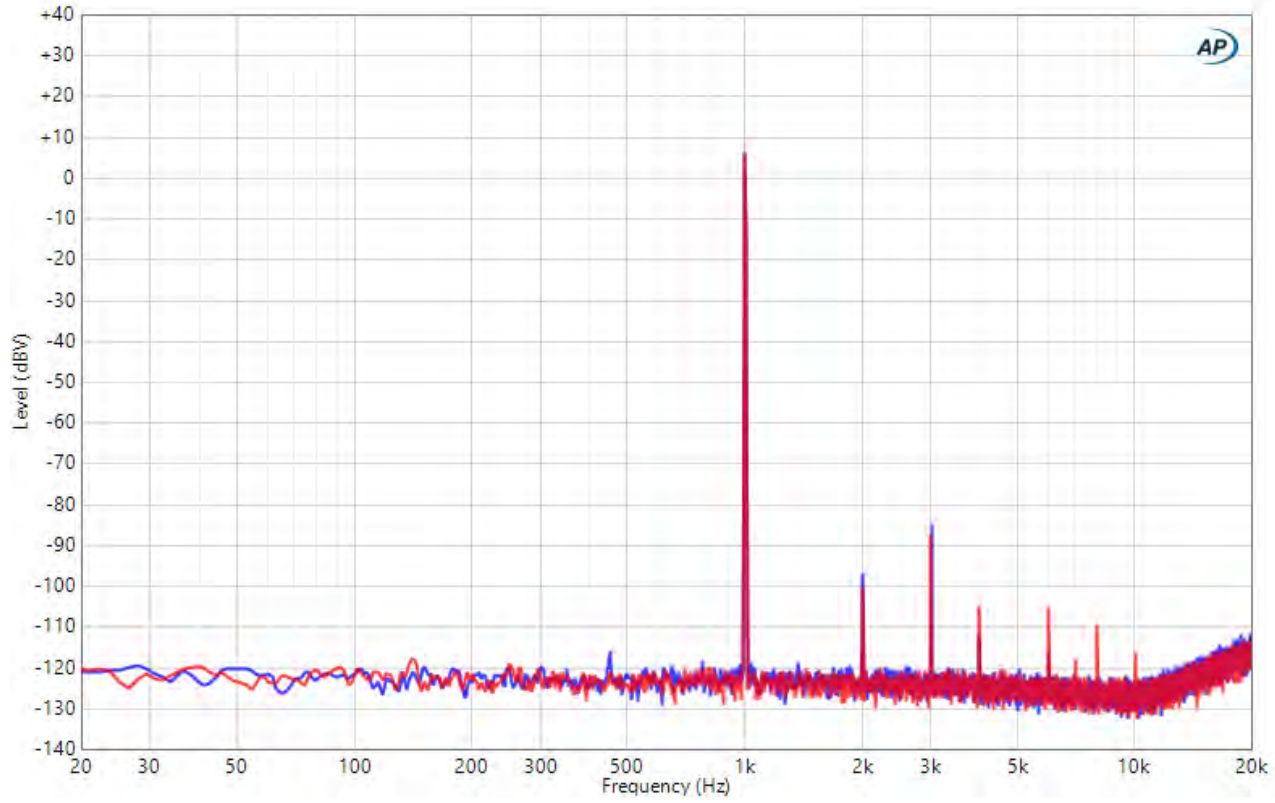


Figure 21 – FFT (32 k samples, F_s = 48 kHz), 1 kHz, 1 W on 4 Ω load

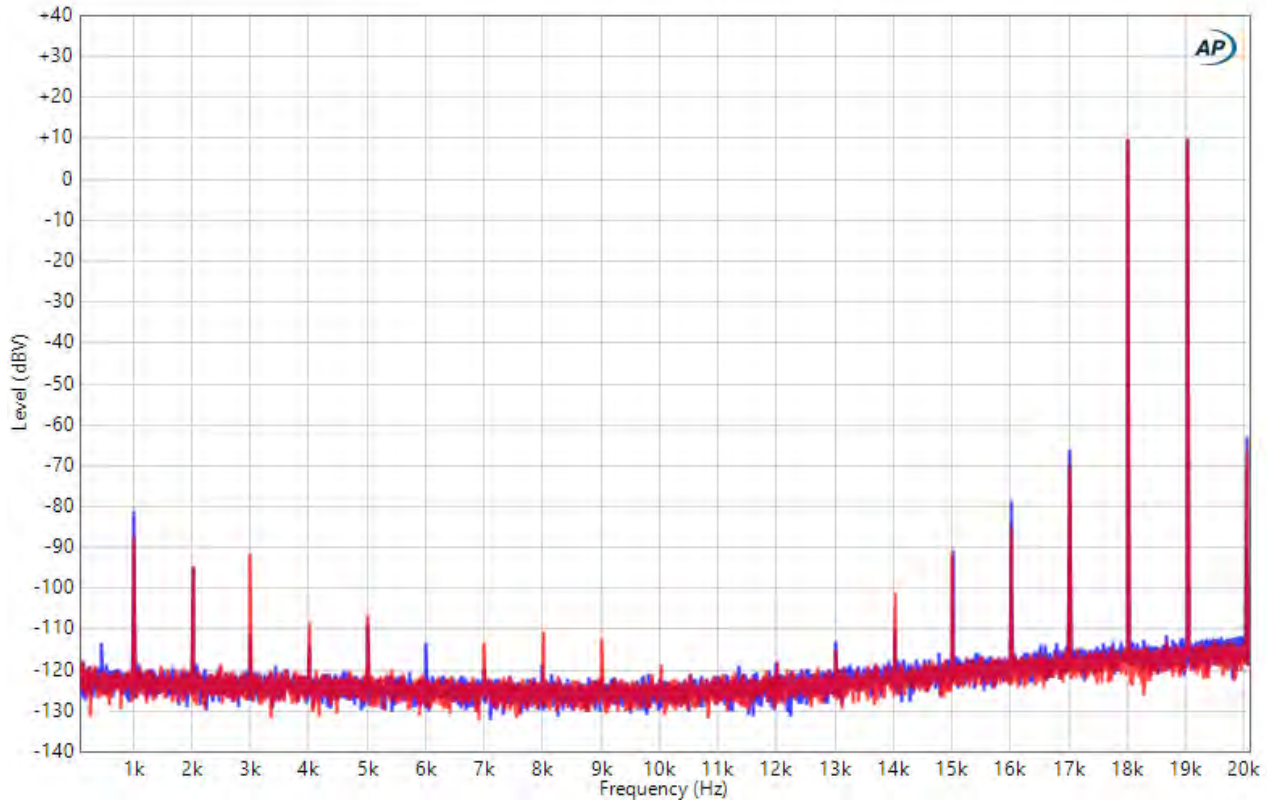


Figure 22 – FFT (32 k samples, F_s = 48 kHz), 18+19 kHz, 5 W on 4 Ω load

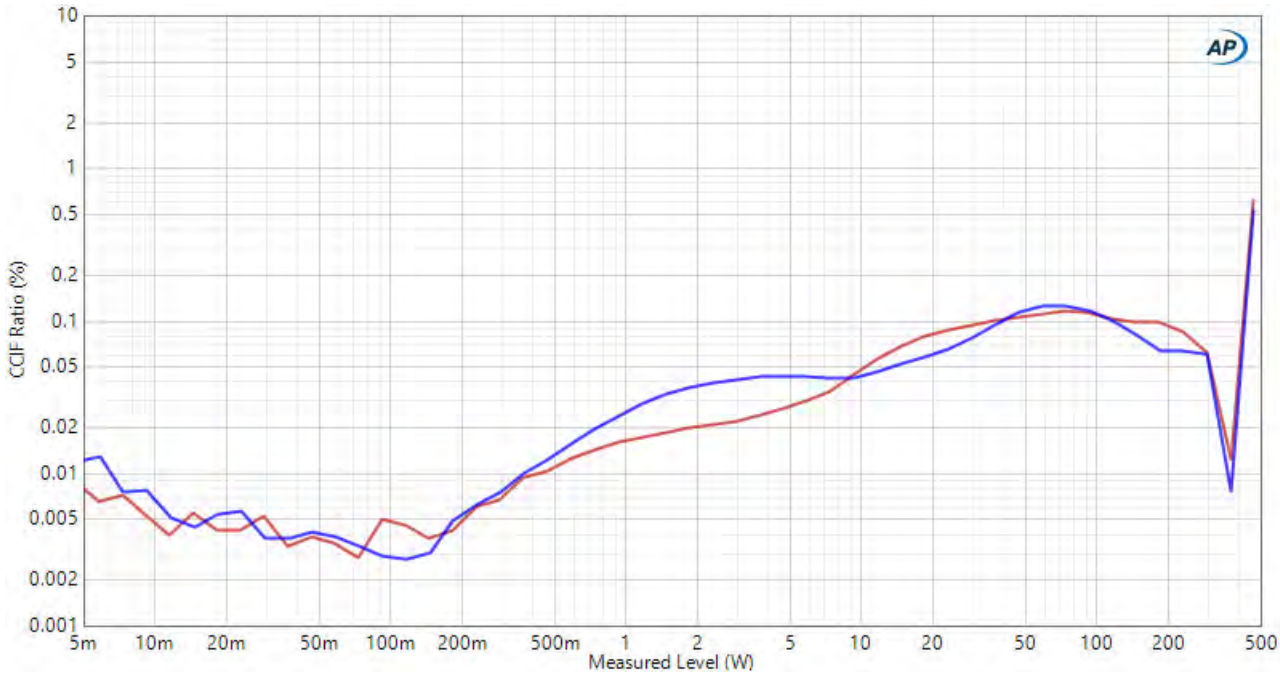


Figure 23 – CCIF IMD vs. Output Power, 18+19 kHz 1:1, d2+d3, both channels

Additional audio measurements

Additional measurements have been carried out with 8 Ω load, and an unregulated power supply built with a line frequency transformer, with 2 x 45 VAC secondaries, and a full wave rectifier with 3300 µF capacitors per rail. Unregulated output voltage was ±60 V, dropping to about ±50 V at maximum output power. Such a setup is capable of 150 W on 8 Ω and 250 W on 4 Ω, with natural cooling.

With lower supply voltage, the measured output noise was also lower, at about 33 µV(A). Rejection of the 50 Hz and harmonics from mains was good and not impacting measured noise.

The effect of shorter deadtime and higher feedback loop gain at DC has been investigated, and it is shown in Figure 26 and Figure 27. The shorter dead-time greatly improved the THD at 6.67 kHz and mid-high power. Increasing the loop gain by 12 dB at low frequency proved to reduce the output noise and impedance, to improve THD+N at 1 kHz, but to increase both the THD+N at 6.67 kHz and the IMD.

Figure 24 – THD+N vs. Output Power at 1 kHz (green) and 6.666 kHz (red), 8 Ω load

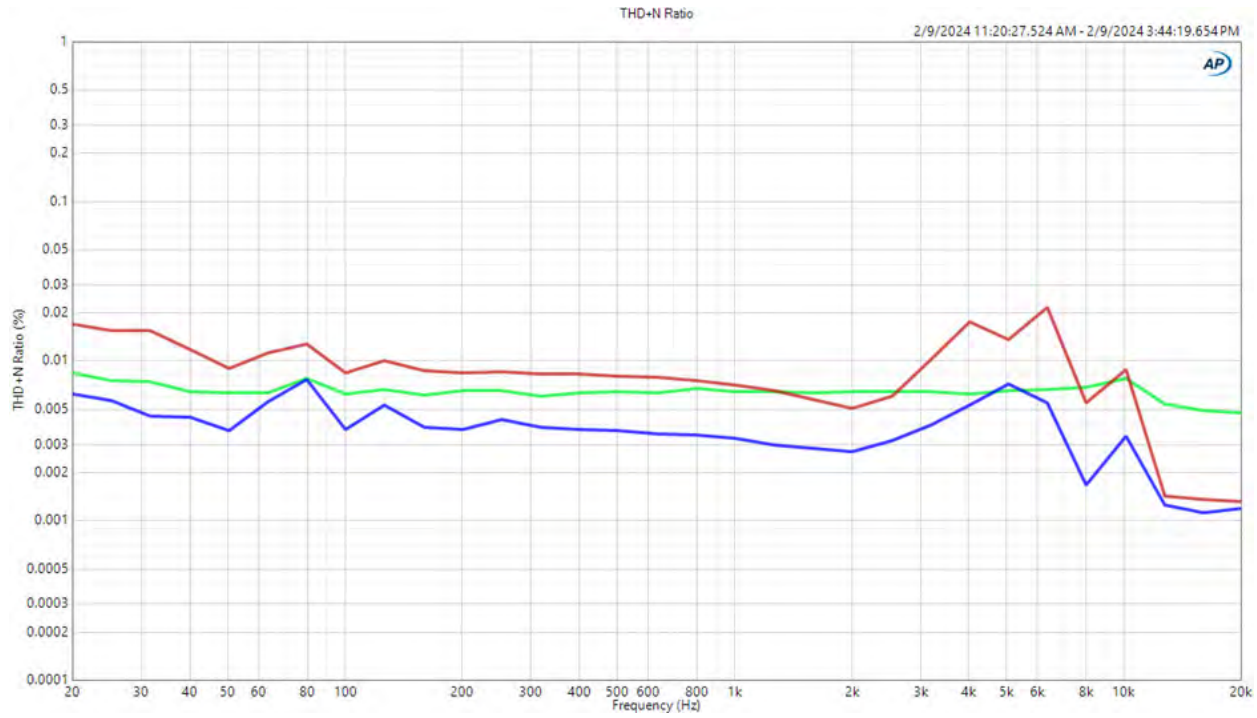


Figure 25 – THD+N vs. Frequency at 0.1 W (green), 10 W (blue) and 100 W (red), 8 Ω load

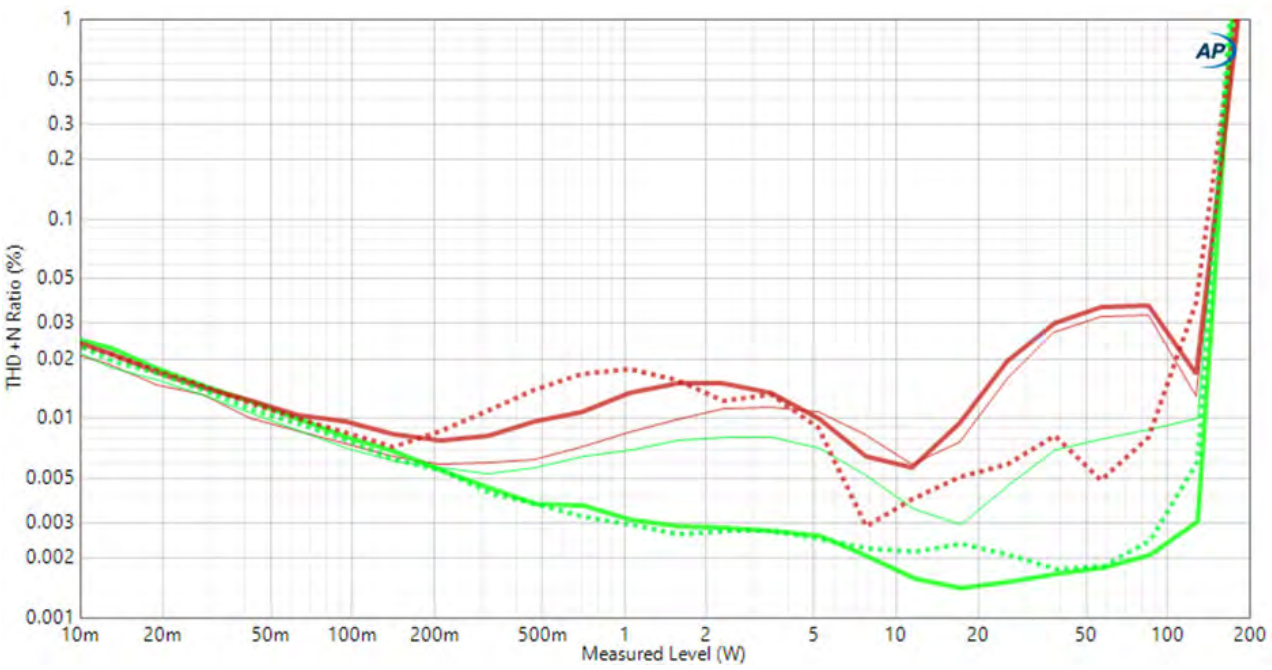


Figure 26 – THD+N vs. Output Power with R1=300 k, 50 ns dead-time (solid) and R1=300 k, 30 ns dead-time (dotted). 8 Ω load. Thin lines is the original EPC9192KIT, with R1=75 k, 50 ns dead-time. 1 kHz (green) and 6.67 kHz (red).

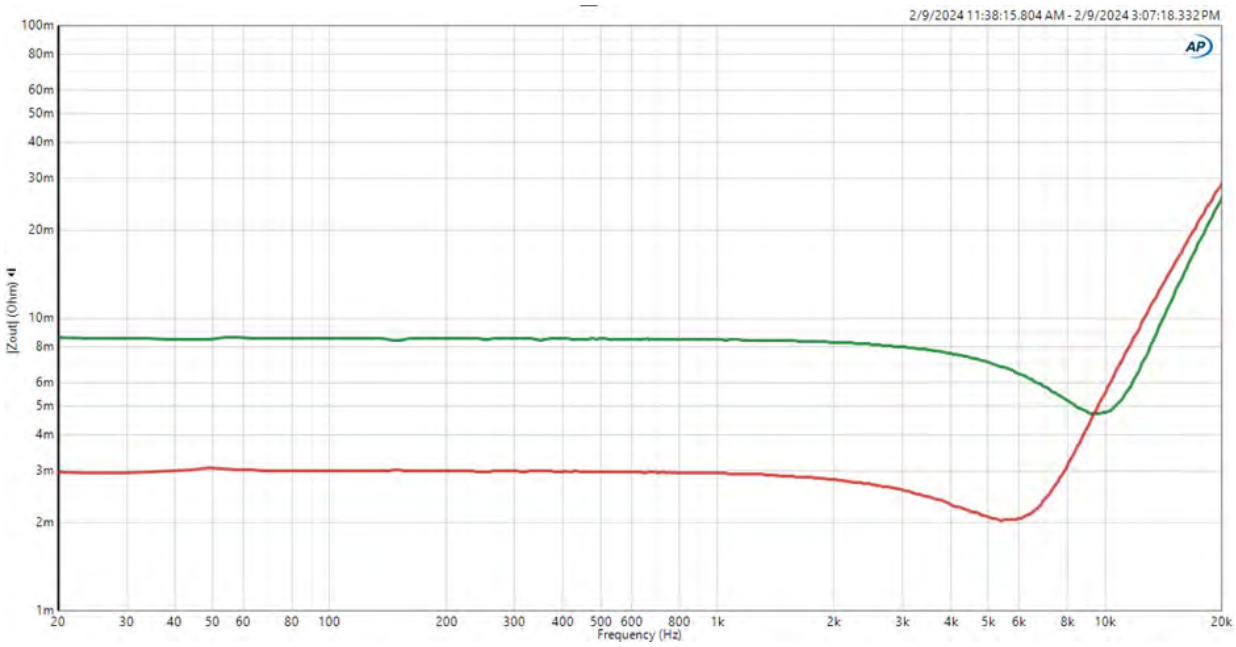


Figure 27 – Output impedance with standard feedback (green) and with R1= 300 k (red), at 1 A_{RMS}.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9192KIT landing page at: https://epc-co.com/epc/Products/DemoBoards/EPC9192KIT

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