EPC Thermal Modeling Calculator Quick Start Guide

User Instructions

Revision 3.0

EFFICIENT POWER CONVERSION

BACKGROUND

Thermal management strategies are essential for high-power devices, and with chip-scale packaging (CSP) of eGaN® FETs, many design advantages can be leveraged at the board-side and the backside (i.e., case) for improved heat dissipation. The PCB offers a first heat dissipation path from the GaN devices, which offers high conductance for CSP parts. The strategic placement of vias improve heat conduction into the inner layers of the PCB. Heat spreading in the board is dependent on the PCB thermal properties which are determined by the conductor layer count and copper thickness. The heat then dissipated from the PCB to ambient through forced air cooling.

Additional heat dissipation can be achieved by benefiting from the low thermal resistance to case side for CSP GaN. Adding a heatsink to the exposed die at the case side increases surface area for heat exchange with the ambient. Thermal interface material (TIM) is required to enhance the thermal contact at the interface between the device and the heatsink. For smaller size dies, gap fill material can also provide a heat conductance path from the die sides, further reducing thermal resistance to the sink surface.

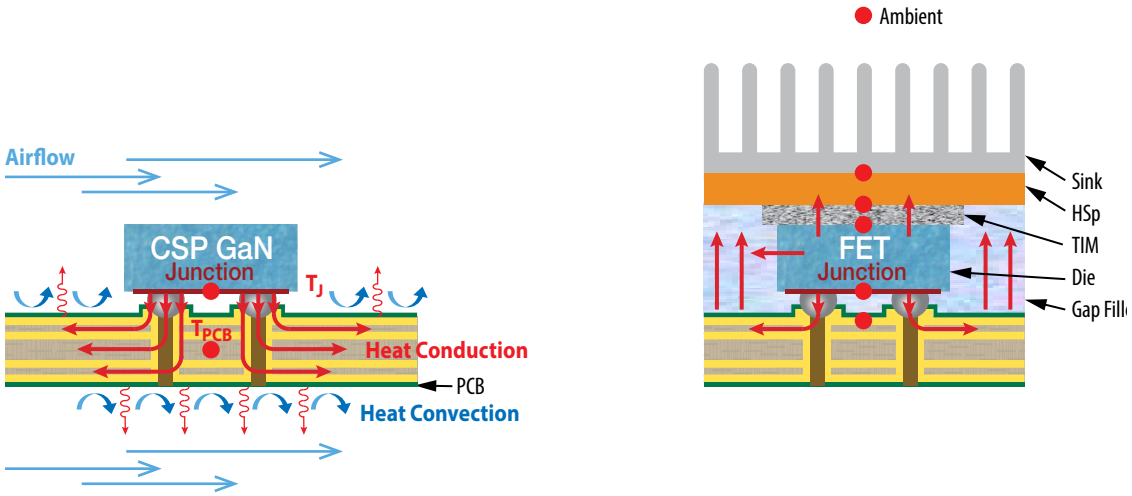


Figure 1: Heat conductance paths from CSP GaN device to ambient (a) through the circuit board and (b) through a heatsink solution

As such, the overall thermal performance and the junction temperature of GaN devices depends on several parameters pertaining to the device construction, PCB construction, and the thermal management approach used. This quick start guide presents a thermal tool which models the thermal performance of GaN devices subject to all the mentioned parameters. More details on thermal management strategies for GaN devices is presented in How2AppNote 012 "*Out of a High-Density eGaN-Based Converter with a Heatsink*."

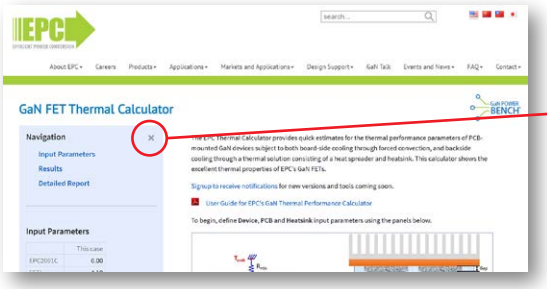
DESCRIPTION

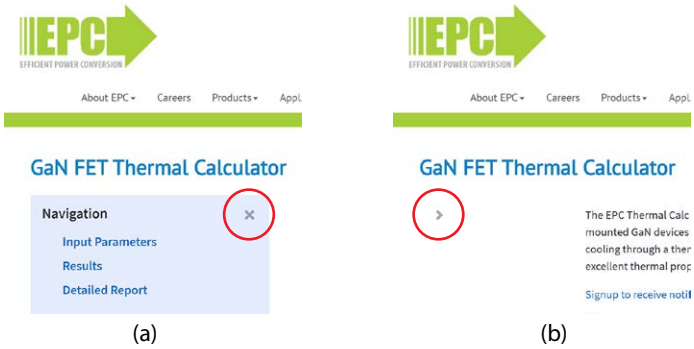
The presented Thermal Calculator, a GaN Power Bench tool, provides quick estimates for the thermal performance parameters of PCB-mounted GaN devices subject to both board-side cooling through forced convection, and backside cooling through a thermal solution consisting of a heat spreader and heatsink. The model accounts for the PCB construction (size, stack-up and via density), die sizes, power losses, TIM materials and heat sink solution. We present in this text the basic layout of the Thermal Calculator user interface and simple instructions on how to define the input parameters and run the thermal model.

The model allows to compare the thermal performance of the GaN FETs with and without backside cooling and can be used to quickly estimate the effect of using different TIM pads and TIM gap fillers. In addition, the cooling effect of the heat spreader and heatsink can be quickly assessed. Two configurations are considered: one for a single FET and another for two FETs in a half-bridge circuit. The different input parameters required for the model can be inputted using a simple and intuitive graphical user interface (GUI) after which the model calculates individual thermal resistances values (R_{th}) and the operating junction temperatures (T_J) for a defined power loss.

INSTALLATION INSTRUCTIONS

The Thermal Calculator is available on **EPC website** and will be updated regularly with more features.





Dynamicly updating Navigation and Summary panel: expanded (a) collapsed (b)

Device and Via Selection

First, the user inputs the basic setup the basis of the thermal system model.

The input parameters are defined in sequential expanding tabs starting with the device parameters, with the following user selectable options:

1. **Device Configuration**: Choices are either a **Single Device** or two-FETs in a **Symmetrical Half-Bridge** configuration.
2. **Device selection**: This selection defines the **device size** (width ***w***, and length ***l*, in mm**). A customizable selection is available in the event a specific size FET is available. For ease of use, a specific EPC FET or IC can be selected from the dropdown list to the right which imports the device dimensions (w and l). The device list is sorted by part name numerical order. Die size is also listed for reference. The die area and characteristic dimension are calculated. Characteristic diameter is used in the radial heat transfer model ($d = \sqrt{(4 \times A/\pi)}$).
3. **Power dissipation**: Sets the power dissipation in the device in Watt (W). In the half-bridge configuration, each device can be set independently. From the choice of FET and power dissipation, the power dissipation density for each device is calculated and displayed.
4. **Device spacing**: Only applicable to the half-bridge configuration. This sets the physical distance between the two devices.
5. **Vias** can be added using the "vias" checkbox, where the number of vias for each FET can be entered. There are safe guards to exclude values that are impractical. The vias type used in this model is constructed according to a IPC4761 type VII (VIPPO), with 7.8 mils diameter with 0.78 mils copper plating wall thickness, are non-conductive filled and plated over. From the number of vias and FETs size a via density is calculated and reported for each FET in vias/mm^2.

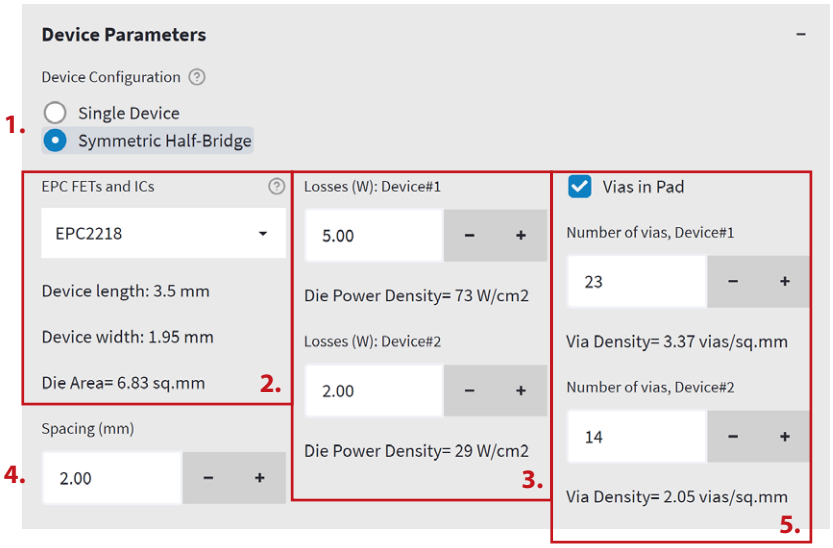
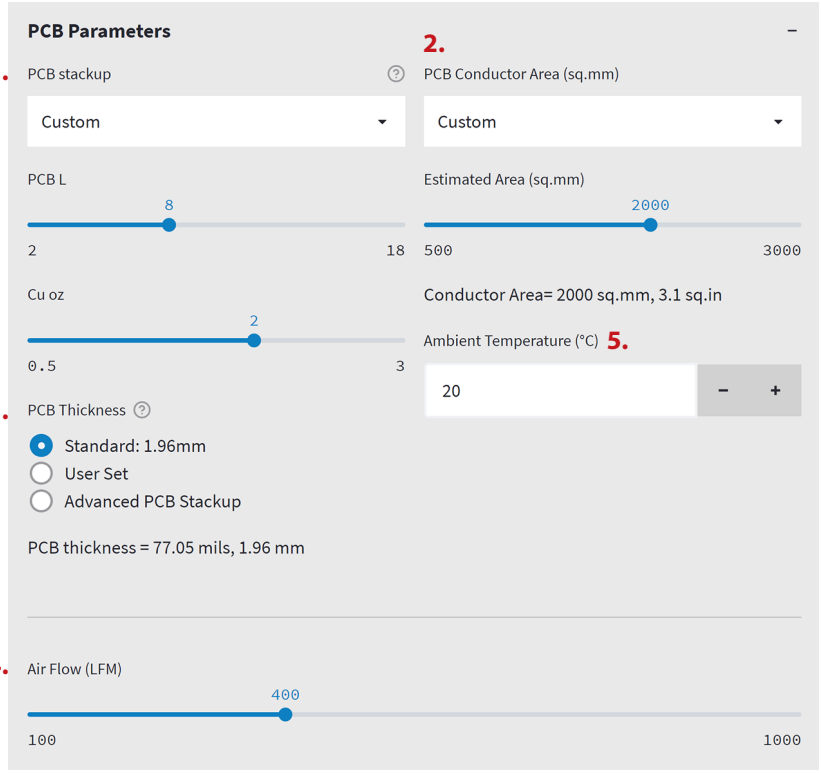


Figure 2: FET and via input selection

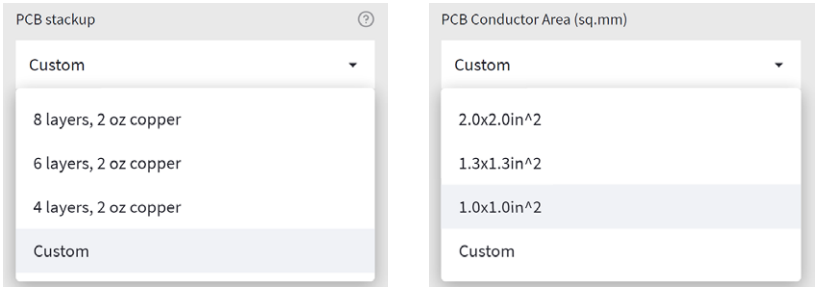
PCB Input Parameters

The next entry screen is the PCB design that provides the substate foundation to which the GaN FETs are mounted to.

1. **PCB stackup**: A selectable option from a pull-down menu with choices from 2 layers through 18 layers or a custom using the slider for the selection. Layer count can only be selected in pairs consistent the PCB manufacturability requirements.
2. **PCB Conductor Area**: A selectable option from a pull-down menu with choices from 1.0 by 1.0 inch through 2.0 by 2.0 inch. Custom values can also be manually inputted. Once selected the tool will report the PCB area in mm^2.
3. **PCB thickness:** This setting: defines the total PCB thickness according to standard estimate with interlayer dielectric thickness of 5 mils and a core dielectric thickness of 20 mils. The user can also set desired thickness using "User Set" option or define the dielectric thicknesses manually by selecting "Advanced PCB Stackup."
4. **Airflow**: Sets the airflow across the defined PCB with units in LFM
5. **Ambient temperature**: Sets the reference ambient in °C with default value of 20°C.



(a)



(b)

Figure 3: (a) PCB input parameters in the GUI, bottom image (b) shows preset selection options for PCB stackup and PCB conductor area

Back-side Cooling Option

Up to this point, only the FETs mounted to a PCB design has been defined. The designer now has the choice to complete the thermal analysis or add a back-side cooling heatsink by selecting the **Heatsink check box** (1.)

Once the heatsink checkbox is selected, the following input parameters open up to set the heatsink solution with the following options:

2. **TIM settings**: To thermally "connect" the backside of the FET and the cooling surface of the heat-spreader/ heatsink, a TIM material must be selected. Here the TIM pad thermal conductivity property can be, **k (W/m.K)** with default of 17.8 W/m.K which is recommended for GaN devices The TIM compressed thickness is set he using the **gap (mm)** entry and defined as the distance between the die surface and the sink surface with a default value of 0.3 mm.

3. **Gap Fill**: For side cooling using a paste, liquid or gel Gap Filler with thermal conductivity, **k (W/m.K)** and the amount defined using a diameter around the FETs as **Gap Fill Diameter (mm)** (4.)

5. **Heatspreader material**: This option allows the design to add a high performance heatspreader between the devices and heatsink, or simply use the heatspreader as the heatsink. The selection is defined by its material, (options are copper or aluminum selectable from a drop-down menu) side dimension, **s (mm)** (a square shape is considered) and its thickness, **t (mm)**. The material options are copper or aluminum selectable from a drop-down menu.

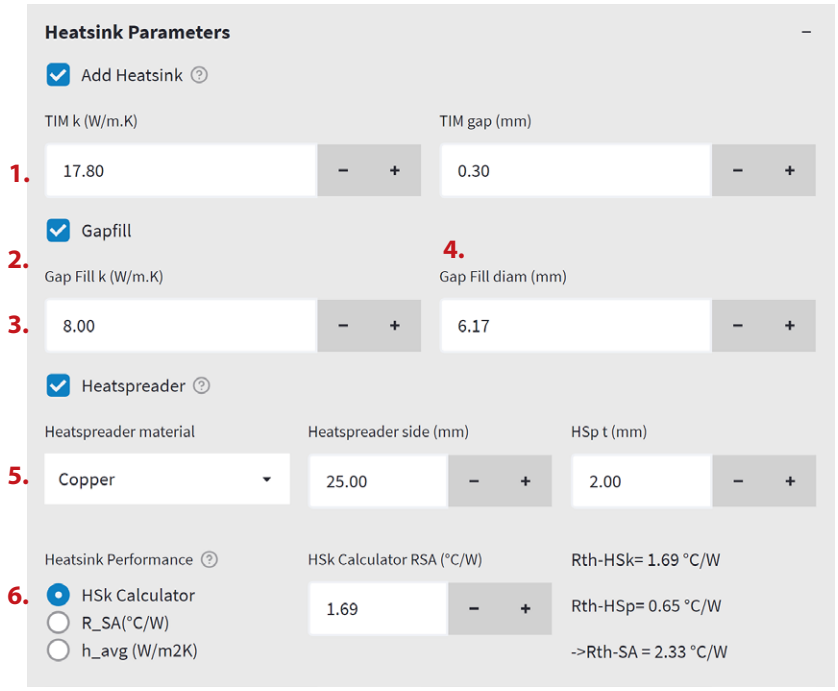


Figure 4: Back-side Cooling Input Parameters

6. **Heatsink (HSk)**: The heatsink basis is selected here with option of defining it as a thermal resistance to ambient R_{SA} **(in K/W)** or heat transfer coefficient ***h*** **(in W/m^{2}K)**. from a heatsink surface of defined area, to represent heat dissipation to ambient from the heatsink thermal ground plane through different modes of heat transfer such as natural convection to air-cooled or water-cooled heatsink, radiation heat transfer to environment, or conduction to electronics housing/case. For the widely used case of air-cooled heatsink, a calculator is provided for custom designs.

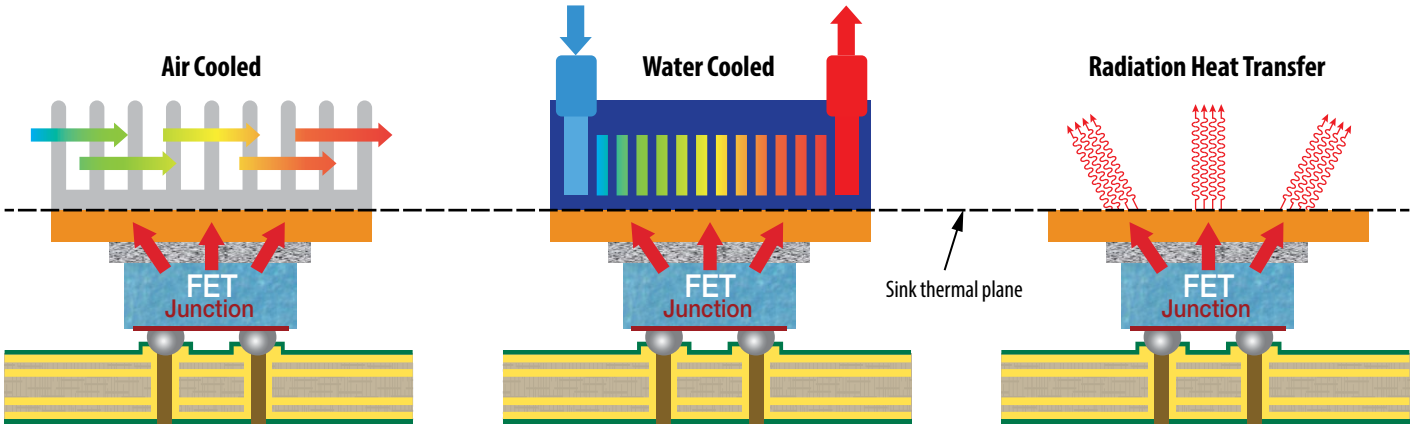


Figure 5: Modes of heat dissipation beyond the sink thermal plane

Heatsink Calculator

If the heatsink thermal resistance is unknown or a custom heatsink is required, then the design can be entered in this window, which can be activated by choosing the **Heatsink Calculator** (1.) under the **Heatsink Parameters** window.

The Heatsink Calculator (2.) is used to estimate the thermal resistance from sink to ambient for a given heatsink dimensions and materials. The model approximates the heat loss through convective and radiative heat transfer. Both natural and forced convection heat transfer are considered, where natural convection occurs for low air flow rates. The input variables considered in the model are shown and labeled (3.). The heatsink materials (Aluminum and Copper) can be selected from the dropdown menu.

After inputting the heatsink mechanical parameters, the resultant heatsink resistance to ambient **HSk R_{SA} (K/W)** is immediately calculated and presented in results panel (Figure 6). The effective heat transfer rate from the heat load surface top surface area of the heatspreader is also reported as **h_{eff} (W/m^{2}K)**.

The "**Generate Heatsink Performance Chart**" button (4.) generates a graph of heatsink thermal resistance as function of air flow rate (Figure 7) for the designed heatsink. The chart is plotted for the prescribed fin height, and for two additional cases with ±20% fin height change.

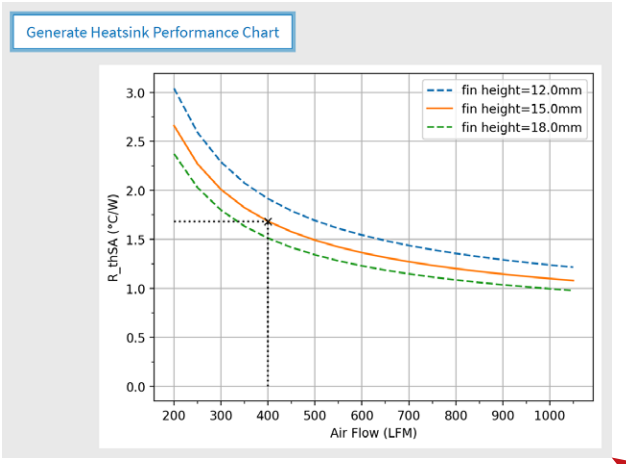


Figure 7: Heatsink Performance Chart

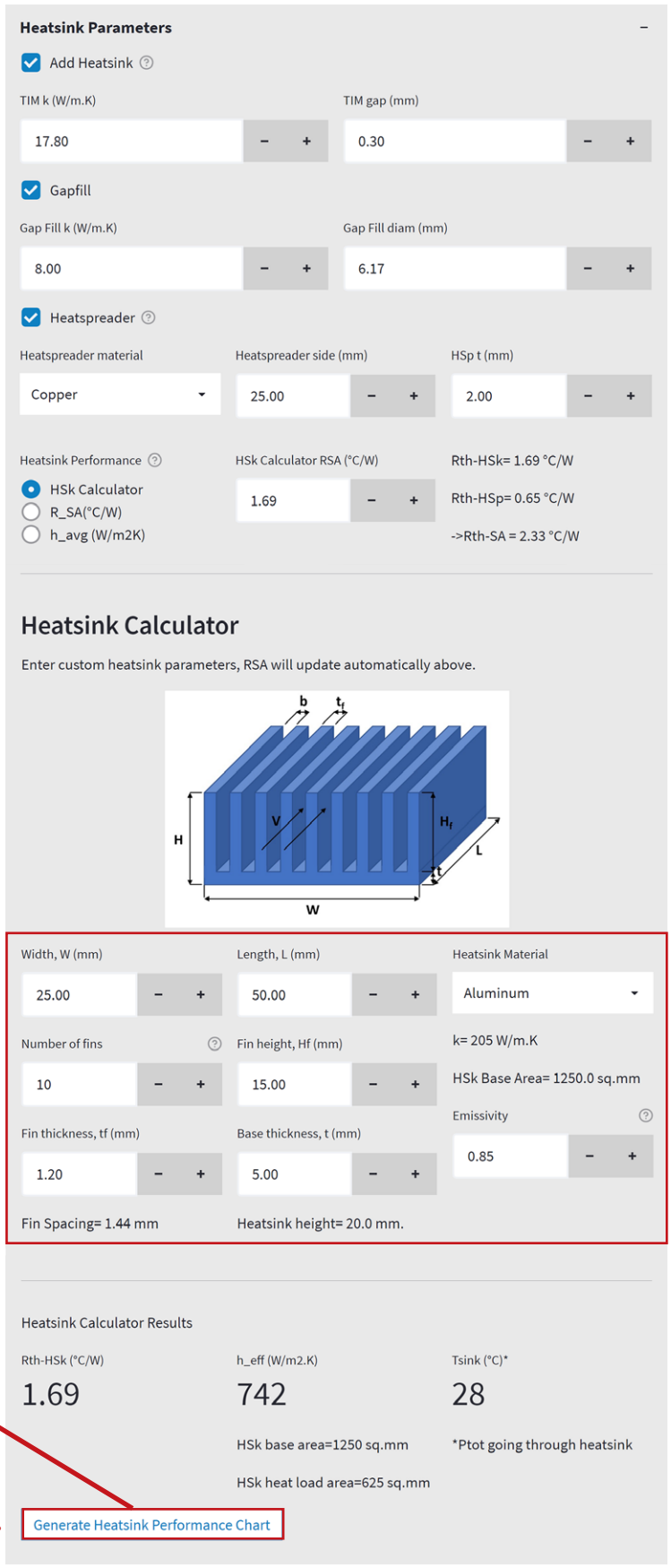


Figure 6: Heatsink Calculator results

THERMAL RESISTANCE CIRCUIT MODEL and thermal design cross-sectional view

The thermal calculator provides quick estimates for the thermal performance parameters of PCB-mounted GaN devices subject to both board-side The thermal tool actively updates and displays the thermal system cross section and equivalent lumped element circuit model as various selections are made. This gives the design visual representation of the design in real time.

Depending on the chosen parameters, a schematic of the thermal resistive network and the physical setup configuration is updated in the portion of the tool. Examples are shown in Figure 8.

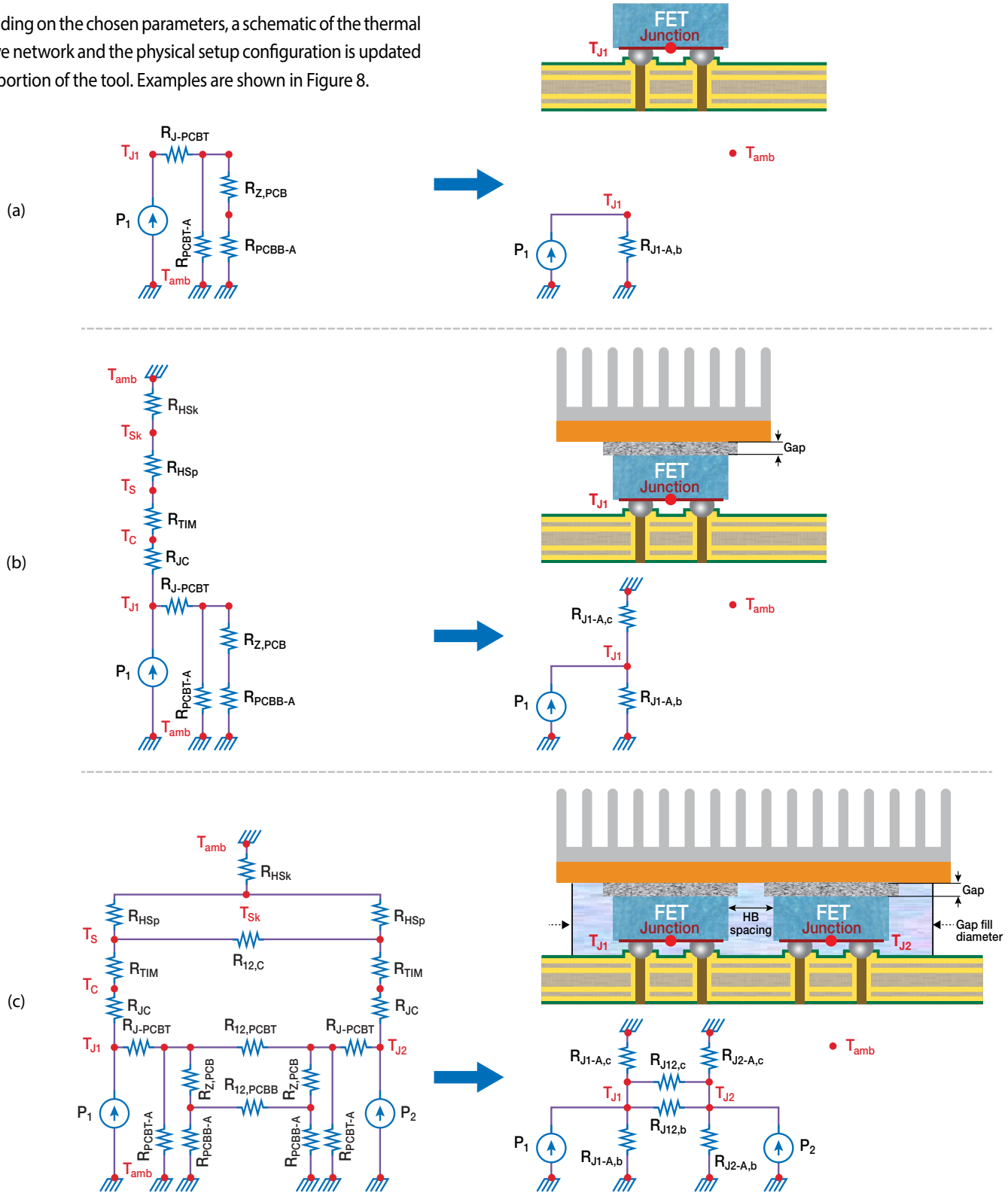
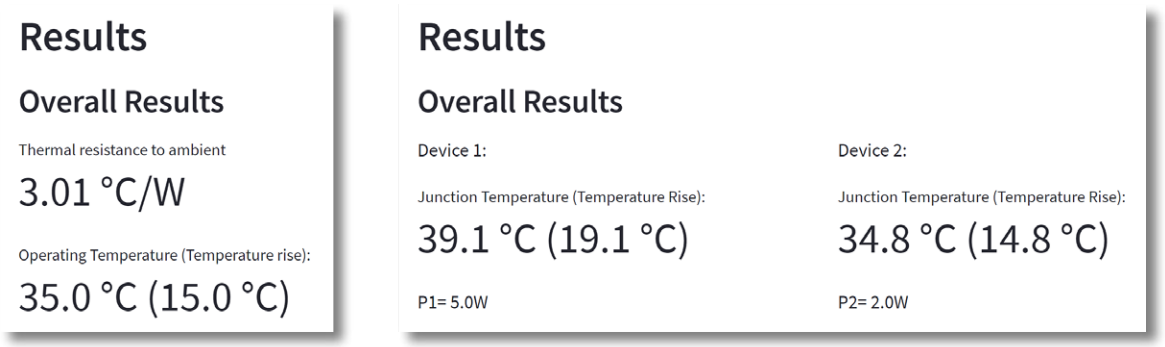


Figure 8: Schematic of the thermal configuration showing cooling solution and representative thermal resistive network for (a) a single FET, no-vias, no backside cooling, (b) a single FET with back-side cooling and thermal vias, (c) two FETs in a half-bridge configuration with thermal vias, back-side cooling, and Gap filler

MODEL RESULTS

After defining all the input parameters for the thermal system, the results are updated, and the operating temperature and temperature rise from ambient is reported for each device (Figure 9).



(a) (b)

*Figure 9: Results Report for the Calculated Thermal Parameters for a **single FET (a)** and **H-Bridge configuration (b)***

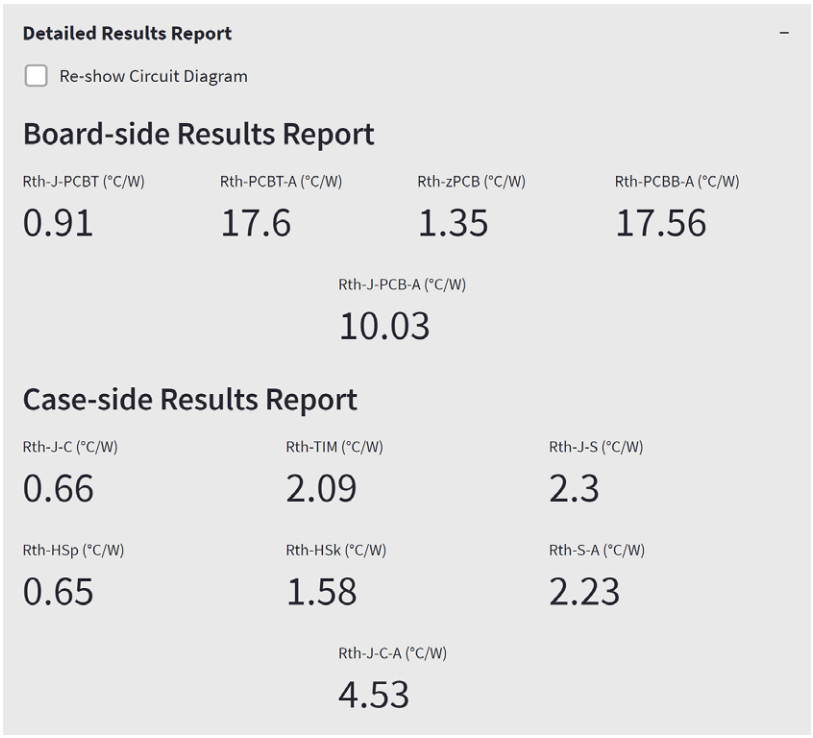


Figure 10: Detailed Report showing thermal resistances for board-side and case-side cooling

A detailed report is also generated and can be expanded to read the estimated thermal resistances of the circuit model (Figure 10). The results are divided into sections with their respective headers, and the variables are representatively named to match the labels shown in the circuit schematic (Figure 8).

In the case of a bridge configuration, the case-side and back-side resistances are combined for equivalent resistances to ambient and thermal coupling resistances. The overall circuit resistances and resulting junction temperatures are finally reported (Figure 11).

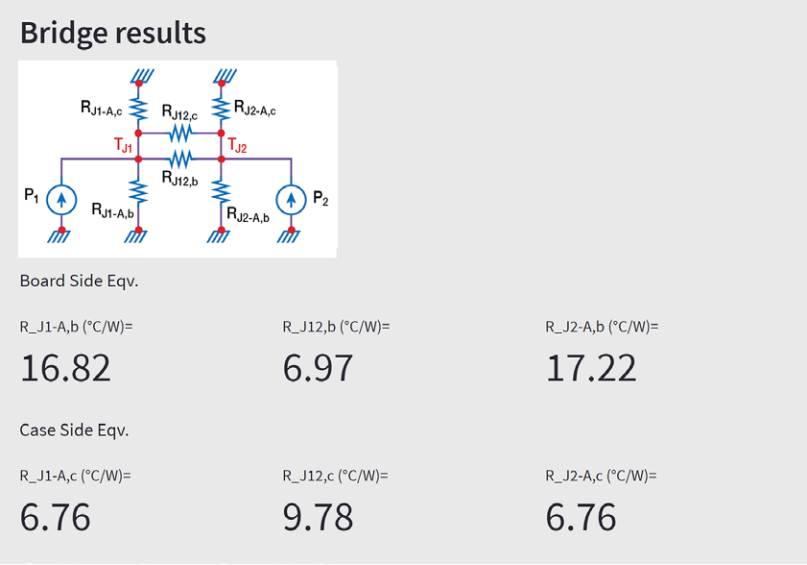
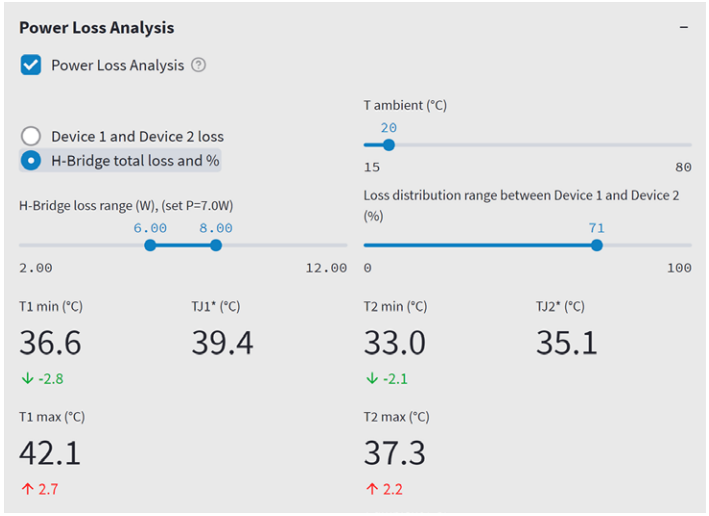


Figure 11: Detailed Report showing effective thermal resistances to ambient and coupling thermal resistance

ADDITIONAL FEATURES

One added feature offers the possibility of varying the loss estimates and assessing the effect on operating temperature. The loss ranges can be defined for a **single FET (a)**, or for each FET in an **H-bridge (b)**, or as a total loss for the H-bridge with the distribution % between high-side and low-side FET. The reported temperatures show the maximum and minimum temperature for each set of power loss. The ambient temperature can also be varied; however, no second order effects or temperature-dependent parameters are defined for the model (only defined for the heatsink calculator).

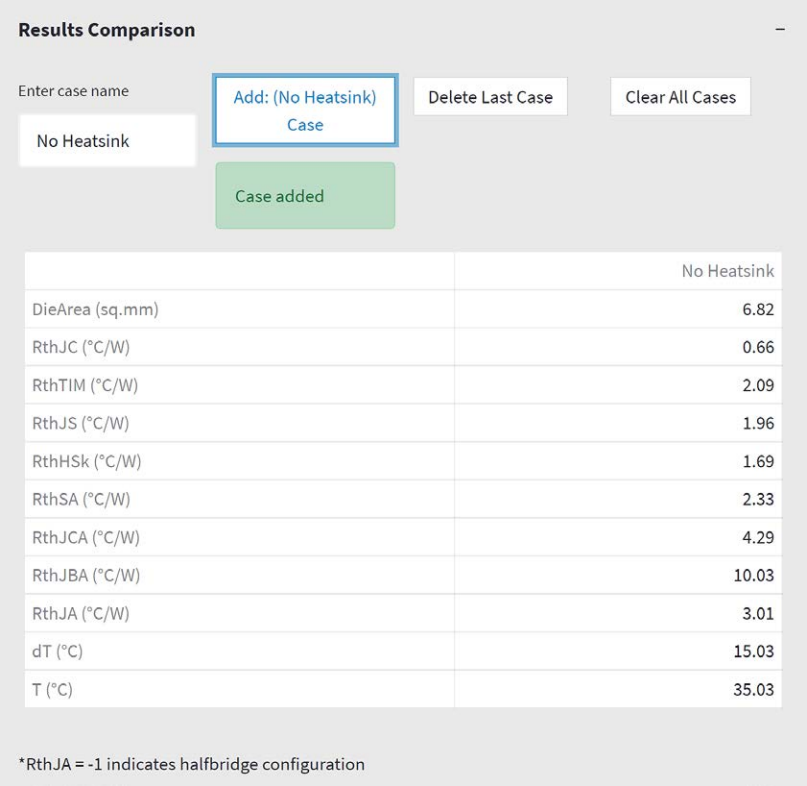
(a)



(b)

Figure 12: Power Loss Analysis showing input for loss range and the resulting temperature estimates

Another added feature allows the user to track the results from different analysis cases. This helps track the results for different configurations and compare thermal performance with different thermal cooling solutions (for example: with vias vs. no vias, with heatsink vs. no heatsink, 400LFM vs. 800LFM…). The case name can be named conveniently and the list of results summary added to a table. The results table is available for download at any point as a csv file (Figure 13).



	No Heatsink
DieArea (sq.mm)	6.82
RthJC (°C/W)	0.66
RthTIM (°C/W)	2.09
RthJS (°C/W)	1.96
RthHSk (°C/W)	1.69
RthSA (°C/W)	2.33
RthJCA (°C/W)	4.29
RthJBA (°C/W)	10.03
RthJA (°C/W)	3.01
dT (°C)	15.03
T (°C)	35.03

*RthJA = -1 indicates halfbridge configuration

Figure 13: Results comparison showing the table with summary of results

SUMMARY

A simple thermal calculator is presented to calculate thermal resistance estimates of devices mounted on a PCB as function of important design parameters such as PCB construction and stack-up, die size, via density and back-side cooling. The added thermal performance of back-side cooling is also calculated and can be quickly compared to a system with only board-side cooling, while also considering the different TIM materials and heat sinking components. The model is expanded to consider a widely implemented half-bridge configuration with 2 devices placed at a certain spacing apart. The thermal coupling is modeled with independent power losses and via density for each device. The calculator serves as a quick thermal tool for electrical designers to estimate the thermal capabilities of a GaN device and to assess the effectiveness of thermal management strategies. Added features allow additional analysis and results comparison. The tool is very effective tool used in early design stages for estimating thermal requirements, sizing and comparing thermal solutions, and assessing the thermal feasibility of circuit board designs.

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