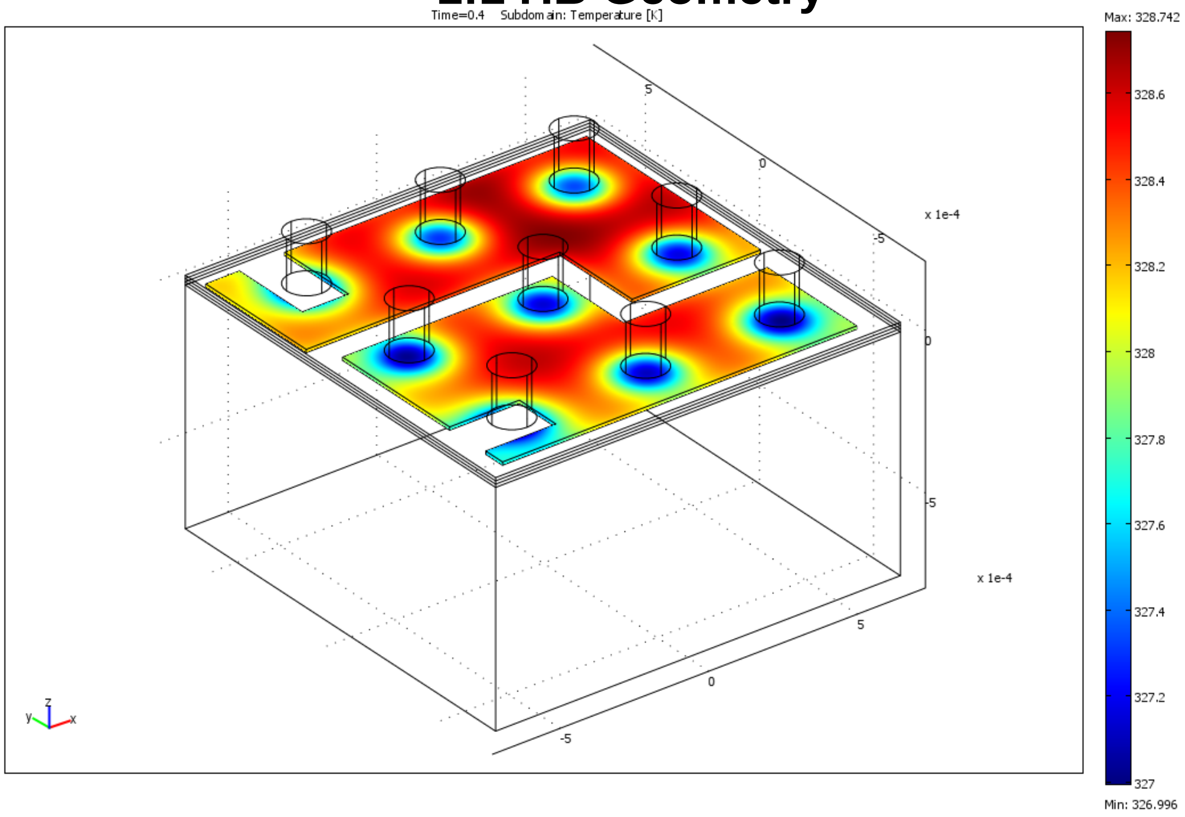
EPC2106 Thermal Simulations
$R_{\theta JB}$ & $R_{\theta JC}$

EPC2106
1:1 Half Bridge Thermal Simulation

- **Standard 5 layer thermal model used on other parts**
- **EPC2106 1:1 HB geometry**
- **Treat each FET Q1 and Q2 as separate, and calculate thermal coupling matrix**
- **$R_{\Theta JB}$ and $R_{\Theta JC}$**
- **Steady state and transient simulations**
  - Transient provide R-C network for thermal model

1:1 HB Geometry



Results Summary

$R_{\Theta JB}$

2 FET Model

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 30.4 & 28.6 \\ 28.6 & 30.9 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

This matrix equation lets you calculate the temperature rise of each FET, given the power dissipated in each FET. Subscripts Q1 and Q2 refer to high side and low side FETs respectively. $R_{\Theta JB}$, instead of being a single number, is now a 2x2 matrix. All units in C/W

$R_{\Theta JC}$

1 FET Model

$R_{\Theta JC}$ = 3.12 ° C/W

Note: See later slides for assumptions

$R_{\Theta JB}$: 2 FET Model

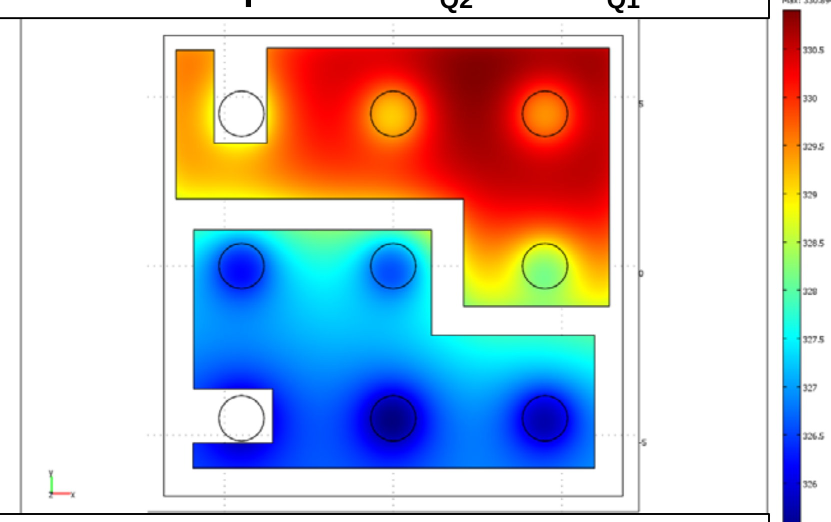
2 simulations

- All power dissipation in Q2 FET
- All power dissipation in Q1 FET

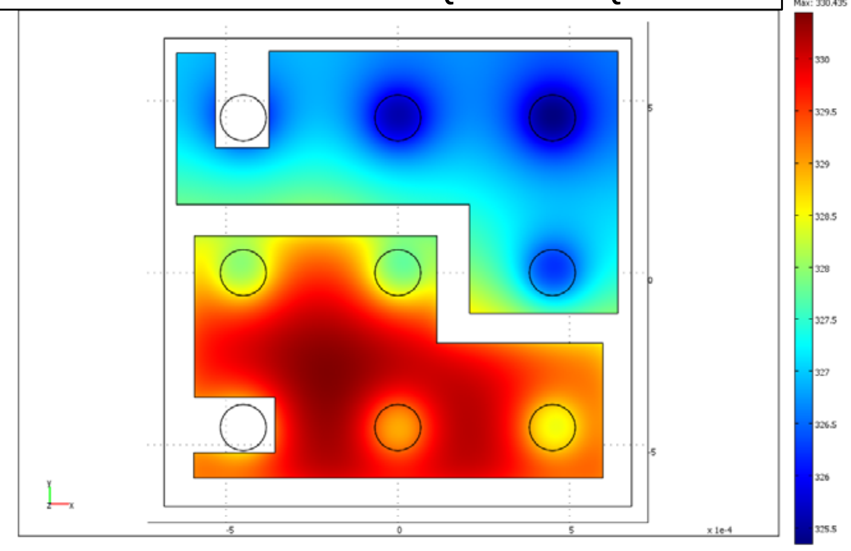
Use results to obtain 2x2 $R_{\Theta JB}$ matrix

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 30.4 & 28.6 \\ 28.6 & 30.9 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

Junction Temperature: P_{Q2} = 1W P_{Q1} = 0W



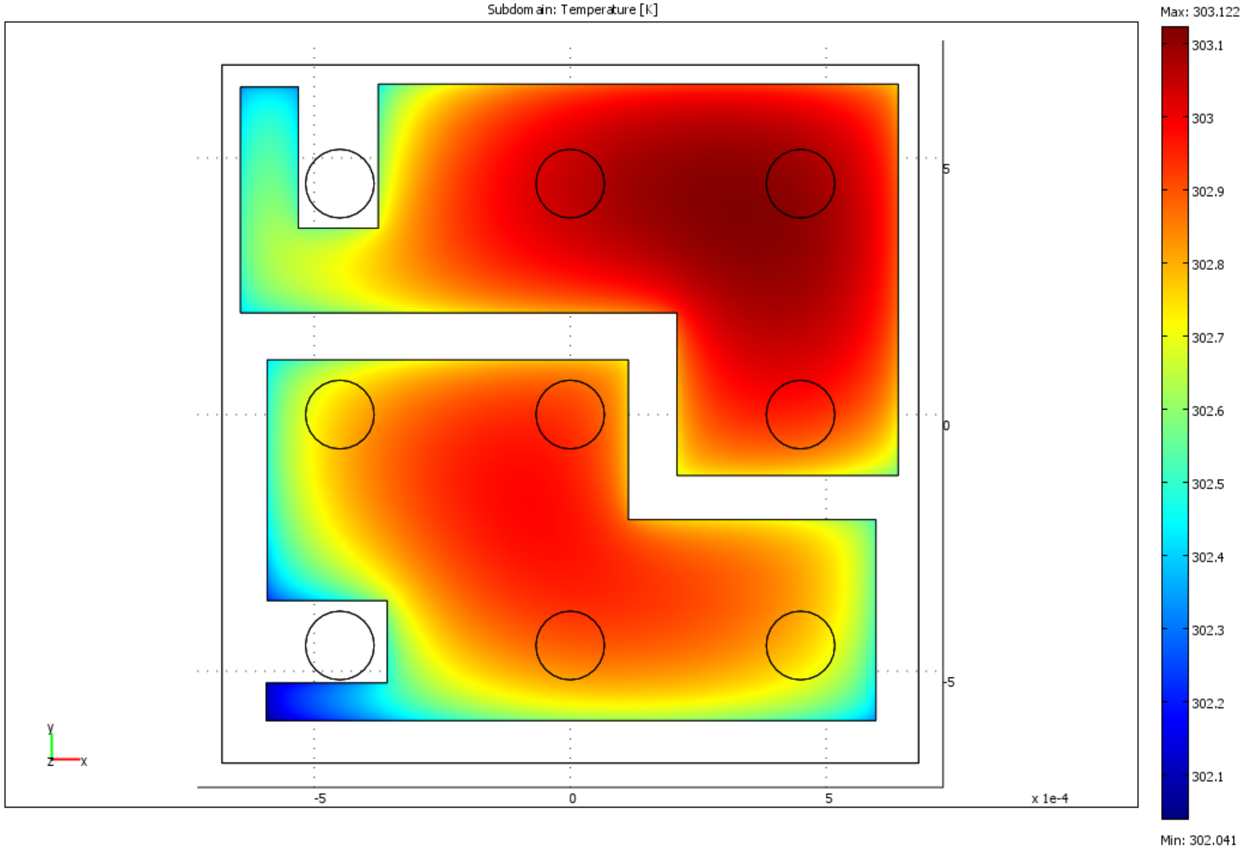
Junction Temperature: P_{Q2} = 0W P_{Q1} = 1W



$R_{\theta JC}$

- $R_{\theta JC}$ = 3.12 C/W (using max temperature rise in junction)
- 1 W total is dissipated in the entire half-bridge, with the same power density in the active areas of both Q1 and Q2 FETs
- Top of bumps are thermally floating, backside of silicon substrate set to 300 K

Junction Temperature under 1W Internal Dissipation



Transient Simulations

- **Transient simulations conducted for both $R_{\theta JB}$ and $R_{\theta JC}$ modes**
- **In both cases, 1 W total is dissipated in the device, with the same volume power density in both FETs**

EFFICIENT POWER CONVERSION

The end of the road for silicon…..

is the beginning of the eGaN FET journey!