High Efficiency High Bandwidth Four–Quadrant Fully Digitally Controlled GaN-based Tracking Power Supply System for Linear Power Amplifiers

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***Abstract*—The ever-rising demands for a high efficiency and high power density in the power electronics market are motivating an intensive research in the area of wide bandgap (WBG) devices, with Enhancement-mode Gallium-Nitride High-electron-mobility Transistors (GaN E-HEMTs) as the main representatives. Compared to the conventional Silicon (Si) devices with the same voltage rating and on-state resistance, the parasitic capacitances of GaN transistors are smaller up to 10 times. Although their turn-off energy is very small, for the high switching speeds Zero-Voltage Switching (ZVS) is preferable to avoid the turn-on power losses, especially in the application where the devices operate at MHz switching frequencies and where the blocking voltages are high. This is also very important from the thermal point of view, due to the poor junction to ambient thermal impedance of the packaging, in order to avoid high junction temperatures. Moreover, for a successful design of a power converter, the magnetic materials optimized for the high frequency range are a must, with a manganese-zinc (MnZn) ferrites as the most promising solution. In this paper, an $8\,$W, $1\,$MHz switching frequency fully digitally controllable bipolar tracking power supply with a $100\,$kHz small signal bandwidth, the tracking speeds up to $2\,$V/μs and the maximum efficiency beyond $94\,\%$ is shown, where a symbiosis of WBG devices and the newest generation high frequency magnetic materials manifests the clear benefits.**

***Index Terms*—Power amplifiers, GaN E-HEMTs, Zero-Voltage Switching (ZVS), FPGA digital control.**

I. Introduction

IN VOLTAGE source applications, where the excellent fidelity and reliability, extremely low noise, good stability and low output impedance are mandatory, linear power amplifiers (LPA) are still the preferred option. There are many reasons why they are widely used in industry: all the aforementioned characteristics are easily resolved with a relatively cheap, simple and robust solutions with a complete linear amplifier with both voltage booster and the current buffer stage in one die. On the other hand, the essential drawback of the linear power amplifiers are the increased losses in the output stage (in the common drain current buffer), especially in the case when the output voltage has high peak-to-average-power ratio (PAPR) [1], and in the case of reactive and non-linear loads. Due to the high losses, the heat sinks tend to occupy big part of the system volume. The problem aggravates when a large number of channels has to be paralleled, where the number of channels and the cost of the system are strongly compromised by the volume of the heat sinks and the ventilation system.

These issues are very well known in the literature, both in low-frequency and RF applications [2], [3]. Different approaches were proposed in [4], [5], [6] where purely switched-mode power amplifiers (SMPA) were presented. Nevertheless, SMPAs could introduce significant nonlinearities in the system and usually require a special effort in order to improve Signal-to-Noise-Ratio (SNR) [7], [8]. Another promising concept for switch-mode power amplifiers was presented in [9], where a hybrid inverter consisted of two switched-mode converters operating at very different switching frequencies, but no experimental results were shown.

In order to tackle all these problems, hybrid solutions may be used to take the advantages of both linear amplifier (excellent linearity, built-in protections) and the SMPA (high efficiency). Basically, there are two groups of the hybrid realizations. In the cases when high output current is needed, the SMPA is put in parallel with the LPA, to facilitate the bulk of the output current, while the LPA is in charge of the output voltage control [10], [11]. The other approach is to lower the voltage drop of the output stage transistors in the LPA by putting a SMPA in series [12]. In some extreme cases, where high slew-rates ($45\,$V/μs) and relatively high voltages are needed, LPA can be supplied with a set of discrete voltage levels in order to avoid high switching frequency and additional losses in the TPS [13].

In this paper, the TPS is based on the idea originated in [12]. Instead of using two DC-DC converters to modulate both supply rails of the LPA as presented in [14], [15], only one bidirectional DC-AC converter is used in order to provide bipolar voltage waveforms, as shown in Fig.1. This solution has been chosen mainly due to the very severe specification for the occupied space of the system. Compared to the solution with two DC-DC converters where each one is designed for

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the full power range, this solution leads to more power savings and less auxiliary electronics (auxiliary power supplies, control circuits, protections, etc.). Additionally, this solution brings more power savings in the LPA than in [13], removing any need for a heat-sink on top of the LPA. In the ideal case, this converter should provide the same waveform at the output as the LPA's output voltage v_{out}. Nevertheless, the small amount of the correction voltage V_{off} is still needed to prevent the ohmic region of the LPA's MOSFETs in the output stage and also to provide extra voltage overhead in the case of a small mismatch between v_{conv} and v_{out}.

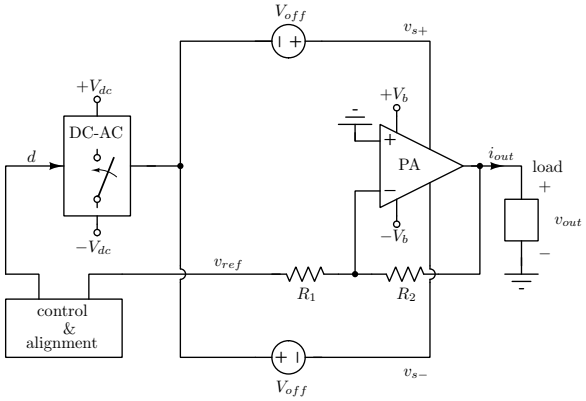

Fig. 1. Linear power amplifier with the Tracking Power Supply System.

In order to have fast dynamics of the TPS, yet a highly efficient and compact solution, Enhancement-mode Gallium Nitride High-electron-mobility Transistors (E-GaN HEMT) are used, switching at 1 MHz in a half-bridge configuration. The aim of this paper is to show that in the applications where low currents are processed with at high switching frequency and relatively high voltage is blocked by the GaN devices (100 V), ZVS is a must to optimize the system efficiency, but also to protect the devices from overheating. The output filter is comprised of two LC sections. The first inductance is designed in order to enable the complete ZVS of the devices and thus remove the turn-on losses. Although the GaN power transistors possess much improved characteristics compared to their Si counterparts, the overall performance of power converters is limited by the passive components [16]. In this case, inductors have a significant impact on the overall system efficiency. Consequently, different designs with a manganese-zinc (MnZn) ferrites optimized for MHz frequency range are presented. Finally in the Experimental results, a 8 W, 1 MHz switching frequency fully digitally controllable bipolar tracking power supply with a 100 kHz small signal bandwidth, the tracking speeds up to 2 V/μs and the efficiency beyond 94 % is shown, with the total power savings up to 4 W compared to the system without the supply modulation.

II. TPS SPECIFICATIONS AND DESIGN

The specifications for the TPS are given in Table I. The TPS must provide a four-quadrant operation, while the load type is not specified in general. The only constraint is put on the maximum output current that can be sourced/sunk at the PA's output. In this work, three different load types are considered: resistive, capacitive and constant current load. The reference has a piecewise linear waveform, with a trapezoidal voltage waveform as a representative test case. The most probable maximum slew-rate of the output voltage transitions is 1 V/μs, but yet the system must be capable to reproduce correctly 2 V/μs transitions as well.

TABLE I
THE SUMMARY OF THE SPECIFICATIONS FOR THE TPS

specification	value
output voltage range	-40 V to $+40$ V
output current range	-200 mA to $+200$ mA
small-signal control bandwidth	100 kHz
maximum transition time of the output voltage	10% of steady-states
maximum slew-rate of the output voltage	1 V/μs to 2 V/μs
minimum output filter attenuation at 1 MHz	60 dB
total occupied area of the power stage	10 cm^2

Having in mind all these specifications, especially the one for the occupied area, it is clear that the size of the converter plays very important role. In order to avoid the modulation of both supply rails ($v_{\text{s+}}$ and $v_{\text{s-}}$) independently, only one two-level switching DC-AC converter is employed. It is worth noting that the two dc inputs for this converter are not disadvantage of this system. These dc inputs are the same as the supplies for the input stage of the LPA, ($V_{\text{b+}}$ and $V_{\text{b-}}$). Nevertheless, in Fig. 2 they are shown independently. The Power Supply Rejection Ratio of the LPA's output stage may have a poor value around the switching frequency. To guarantee the small voltage ripple at the output, two stage filter is used, which can provide a sufficient attenuation of the switching noise. The TPS is controlled via double control scheme implemented in a digital control hardware: the inner control loop based on Peak-Limiting Current Control that controls the current of the inductor and the outer voltage mode control loop with the integral action that provides accurate tracking of of the the voltage references.

The system is comprised of the following parts:

- High-frequency switching two level DC/AC converter (inverter) with the two-stage output filter;
- Linear power amplifier;
- Auxiliary offset voltages;
- FPGA control board with the interconnection converters between analog continuous time and discrete-time system variables (A/D converters, D/A converters, analog comparator) needed for the feedback control loops.

The operation principle of the whole system, explained at the representative trapezoidal waveform is shown in Fig. 3. The common mode voltage of LPA supply rails has the same value as the output voltage v_{out} and the TPS output voltage v_{conv} ($v_{\text{s+}} + v_{\text{s-}} = 2\,v_{\text{out}}$), while the differential voltage between the rails is kept constant and has the value $2\,V_{\text{off}}$ ($v_{\text{s+}} - v_{\text{s-}} = 2\,V_{\text{off}}$). This means that the power dissipated on the LPA does not depend anymore on the output voltage, but only on the output current i_{out}. The instantaneous power dissipation is

$$p(t) = V_{\text{off}}\ |i_{\text{out}}| \tag{1}$$

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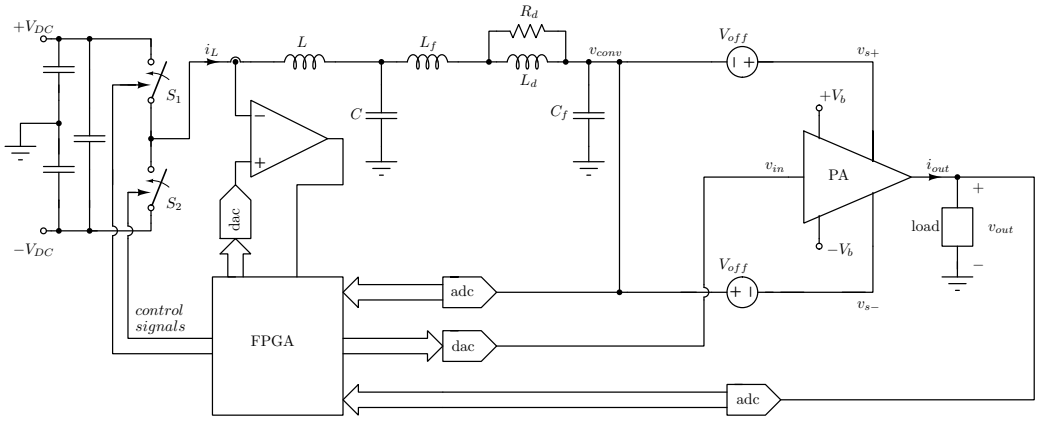

Fig. 2. Detailed schematic of the whole system comprised of the TPS (two level DC/AC converter and the two-stage output filter), the linear power amplifier and the control circuitry.

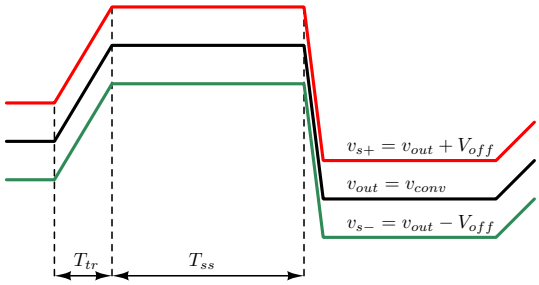

Fig. 3. Operating principle of the system at the example of an arbitrary piecewise linear waveform.

This power loss can be reduced to a very low value, depending on the minimum V_{off} required for linear operation of the power amplifier. The total power dissipation of the system will be mainly affected by the losses of the TPS which are discussed in the next sections.

III. Overview of Switching Power Devices and Zero Voltage Switching

A. GaN versus Si devices

According to the specifications given in Table I, the small-signal control bandwidth should be 100 kHz. As a rule of thumb, the switching frequency is chosen to be 10 times faster, which is 1 MHz in this case. The next step is to select appropriate power transistors that can provide a satisfactory behavior regarding the converter efficiency at these specific conditions. Electrical characteristics of power transistor are usually evaluated via three important parameters: total gate charge Q_{g}, which describes the switching speed of the devices and affects gate driving losses and the switching turn-on and turn-off losses; the parasitic output capacitance (C_{oss}) which quantify the total energy stored in the device in the off-state and affects the hard switching turn-on losses; and the on-state drain-to-source resistance (R_{on}) that affects the conduction losses. The first insight into the device characteristics is usually realized using figures of merit: $\text{FOM}_1 = Q_{\text{g}} \times R_{\text{on}}$ and $\text{FOM}_2 = C_{\text{oss}} \times R_{\text{on}}$. Since the GaN devices have at least 10 times smaller FOM_1 compared to the Si based devices with the similar voltage rating as can be seen in Fig. 4, this enables very high switching speeds and lower switching losses. Although silicon-based (Si) devices are highly reliable solution, they typically occupy more space compared to the Gallium Nitride (GaN) devices, which can be crucial in volume sensitive applications [17]. Additionally, due to the small and compact package, GaN devices could introduce lower parasitic inductances which play a significant role in the switching losses. An optimized layout design with small gate and switching loops, and reduced size of the passive components (especially inductors) can result in a significant increase in both the efficiency and the power density of the switching power converter [18], [19]. Consequently, GaN based devices have been chosen in this design.

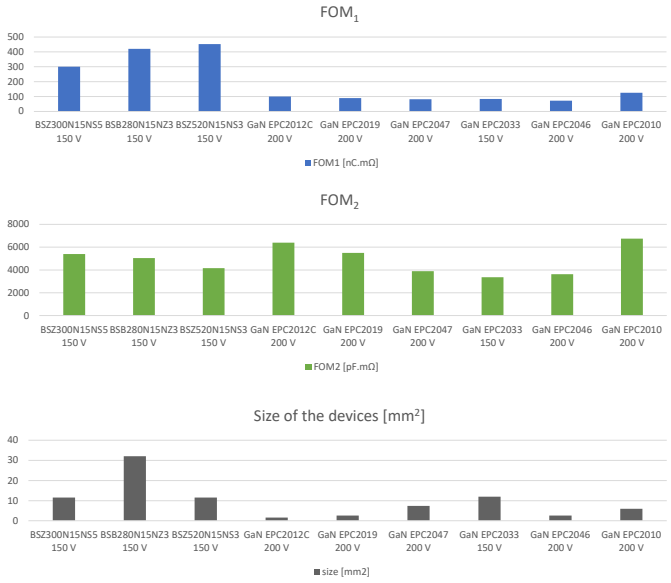

Fig. 4. Comparison of the state-of-the-art Si and GaN based devices: FOM_1, FOM_2 and the size of the devices.

B. ZVS conditions

In the case of full hard switching of GaN power transistor, turn-on and turn-off losses caused by the voltage-current

coexistence during the switching operation can be reduced to a very low value. This is due to a low value of the reverse transfer (Miller) capacitance C_{gd} and consequently the turn-on and turn-off times are small. In principle, the turn-off loss of GaN devices can be very small, especially when driving circuit parameters and packaging are properly optimized [20]. Although GaN devices have up to 10 times smaller parasitic capacitances compared to the conventional Silicon (Si) devices with the same (or similar) voltage rating and on-state resistance, these devices may still have very pronounced turn-on losses at MHz switching frequencies due to the parasitic output capacitances. These losses can compromise the system efficiency, depending on the output power, but also the driving signal integrity is jeopardized due to high $\frac{\text{d}v}{\text{d}t}$ of the switching node voltage and produced conducted common-mode [21] and radiated noise. Moreover, due to the small bumped die of the devices and poor thermal impedance of the packaging, the losses can impact the case temperature a lot. For example, for GaN EPC2012C with $Q_{\text{oss}} = 10\,\text{nC}$ transistor at $1\,\text{MHz}$ switching frequency and $V_{\text{bus}} = 100\,\text{V}$, the power loss due to the parasitic output capacitance is $1\,\text{W}$, which would lead to an incremental temperature rise of $85\,^{\circ}\text{C}$, according to the Datasheet data of the device [22] (device mounted onto a FR4 PCB substrate). Since the devices are the critical parts of the system regarding the reliability, the first inductor of the output filter (Fig. 2) is designed to achieve Zero Voltage Switching (ZVS) during the steady-states and to permit hard switching only during the transients (Fig 3), which last at most 10% of the steady-state time.

In order to achieve ZVS operation of both GaN transistors in the converter for all the steady-states of the output voltage, several conditions have to be accomplished. In [23], the conditions for soft-switching transition of a MOSFET bridge leg and an inductor L are explained. In this paper, the conditions for full ZVS are detailed when the output voltage has a non-zero value. First of all, the inductor current ripple Δi_{L} must be at least two times higher than the output current i_{out}:

$$\Delta i_{\text{L}} > 2\, i_{\text{out}} \tag{2}$$

The increase in the inductor current ripple can lead to very reduced switching losses, but also causing the rise in the conduction losses of the system. This trade-off is quantified in [24].

Although this current ripple condition is necessary to assure the possibility to discharge both high side and low side parasitic output capacitance, it is not always sufficient condition. In some cases there is a certain amount of energy that the inductor must contain just before the ZVS resonant transition, defined by the converter output voltage v_{conv} and the parasitic output charge Q_{oss} which is analyzed as follows. Q_{oss} denotes the total output charge of a device, calculated as integral of differential non-linear output capacitance $C_{\text{oss}}(v)$ over DC bus voltage V_{bus}:

$$Q_{\text{oss}} = \int_0^{V_{\text{bus}}} C_{\text{oss}}\,(v)\,\text{d}v \tag{3}$$

In Figure 5, the total charge flowing for both ZVS transitions are depicted assuming that complete ZVS occurs, with the corresponding voltage and current waveforms, where i_1 is the inductor current in the moment when the LS switch turns-off; i_2 is the inductor current in the moment when the HS switch turns-on; i_3 is the inductor current in the moment when the HS switch turns-off; and i_4 is the inductor current in the moment when the LS switch turns-on. The switch (LS or HS) turns on as soon as the the reverse conduction of the GaN device starts in order to prevent the diode conduction, since the voltage drop of the reverse conducting GaN device is higher than the body diode forward drop in a Si-based device. Although the mechanism of the reverse conduction of a GaN-based device is different from the case of a Si-based device, in this paper it is called internal GaN diode conduction.

Under the assumption that v_{conv} does not change during the transition (considered as the ideal voltage source) and that corresponding parasitic output capacitances are completely charged/discharged (full ZVS) without any dissipation in the system during the ZVS transition, the energy balance holds in the following form:

$$E_{\text{final}} = E_{\text{initial}} + \Delta E \tag{4}$$

where E_{initial} is the total initial energy before the ZVS transition contained in L and both C_{oss} capacitors, E_{final} is the total final energy after the ZVS transition contained in aforementioned passive components and ΔE is the energy delivered into the system by the DC input voltage sources V_{dc1}, V_{dc2} and by the output voltage source v_{conv}. The overview of these energies for both ZVS resonant transitions is shown in Table II. E_{oss} denotes the stored energy of parasitic output capacitance, defined as:

$$E_{\text{oss}} = \int_0^{V_{\text{bus}}} C_{\text{oss}}\,(v) \cdot v\,\text{d}v \tag{5}$$

According to the energy balance equation (4) and the values from Table II, the following conclusions can be drawn:

- If $V_{\text{dc1}} = V_{\text{dc2}} = V_{\text{dc}}$, which is also the case in the analyzed TPS, in total there is no energy interchange with the input voltage sources during the ZVS resonant transitions. The following conclusions are also derived under this assumption.
- In the case of HS C_{oss} discharging, for the negative output voltage v_{conv}, the portion of energy is absorbed by the output, which defines the minimum needed initial inductor energy before the transition:

$$\frac{Li_1^2}{2} > -2\,Q_{\text{oss}} v_{\text{conv}},\; v_{\text{conv}} < 0 \tag{6}$$

- In the case of LS C_{oss} discharging, for the positive output voltage v_{conv}, the portion of energy is absorbed by the output, which defines the minimum needed initial inductor energy before the transition:

$$\frac{Li_3^2}{2} > 2\,Q_{\text{oss}} v_{\text{conv}},\; v_{\text{conv}} > 0 \tag{7}$$

- In all other cases, when the output voltage is negative and HS C_{oss} should be discharged and when the output voltage is positive and LS C_{oss} should be discharged, the minimum initial inductor energy is not defined. Theoretically, any amount of the initial non-zero inductor energy

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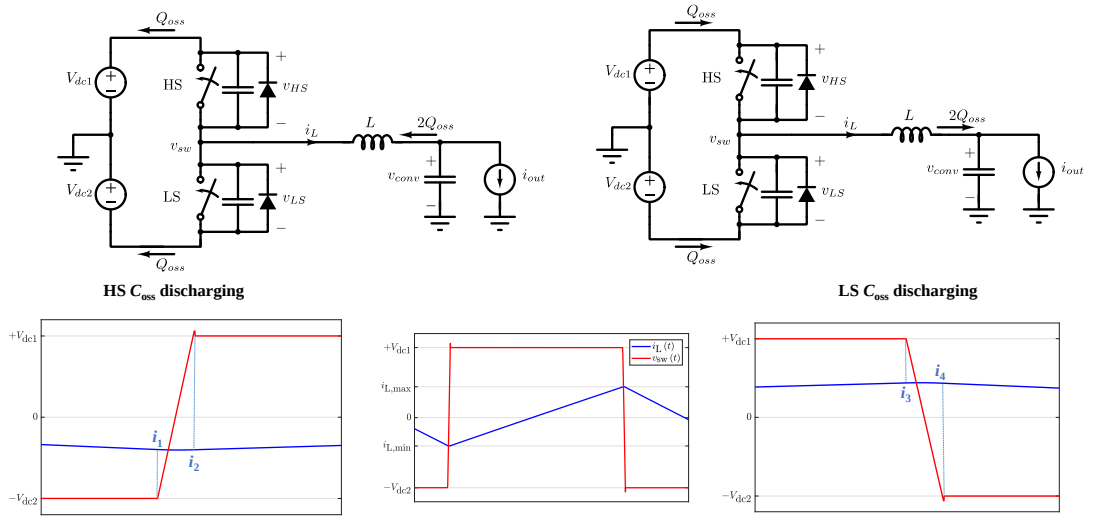

Fig. 5. ZVS resonant transitions with the corresponding waveforms of the switching node voltage and the inductor current.

TABLE II
ENERGY TRANSFER DURING THE ZVS RESONANT TRANSITION

	E_{initial}	ΔE	E_{final}
HS C_{oss} discharging	$\frac{1}{2}Li_1^2 + E_{\text{oss}}(V_{\text{bus}})$	$(V_{\text{dc2}} - V_{\text{dc1}})Q_{\text{oss}} + 2\,Q_{\text{oss}}v_{\text{conv}}$	$\frac{1}{2}Li_2^2 + E_{\text{oss}}(V_{\text{bus}})$
LS C_{oss} discharging	$\frac{1}{2}Li_3^2 + E_{\text{oss}}(V_{\text{bus}})$	$(V_{\text{dc1}} - V_{\text{dc2}})Q_{\text{oss}} - 2\,Q_{\text{oss}}v_{\text{conv}}$	$\frac{1}{2}Li_4^2 + E_{\text{oss}}(V_{\text{bus}})$

would be enough to move the output charge from the output parasitic capacitances. In the real systems, this minimum always exists due to C_{oss} charging/discharging losses [25], but also due to the losses in the series resistances and the parasitic capacitance between the switching node and the ground layer of the PCB, which are out of the scope of this model. The minimum energy needed for complete ZVS transition in that case is always higher than the minimum value presented in previous two conclusions.

Finally, the value of the first inductance L_1 (Fig. 2) can be calculated based on the previously mentioned conclusions, for the different value of the output voltage and the load current, which is presented in Fig. 6, specified in Table I and for the output charge of $Q_{\text{oss}} = 10\,\text{nC}$ (EPC2012C for $V_{\text{bus}} = 100\,\text{V}$). The lines represent the maximum inductance value L_1 (from Fig. 2) for all possible values of the TPS output voltage and for some values of the output current, including the maximum and minimum specified output currents of 200 mA and -200 mA. In some cases the requirement for the minimum inductor energy given by (6) – (7) predominates, while in the rest of the considered cases the limitation is defined by the minimum peak-to-peak inductor current ripple that has to be at least twice of the load current (2) in order to achieve full ZVS transition. It can bee seen that the most critical cases for this design are when the TPS is loaded with the maximum output current (200 mA) at the minimum output voltage (-40 V) or with the minimum output current (-200 mA) at the maximum output voltage (40 V), and the needed inductance to achieve full ZVS in all the steady-states is $L_1 = 6.5\,\mu\text{H}$. Moreover, for a certain value of the inductance, it can be determined from this graph whether the conditions for the soft-switching for the chosen power transistors and at the specified switching frequency (EPC2012C at 1 MHz, in this case) are fulfilled or not.

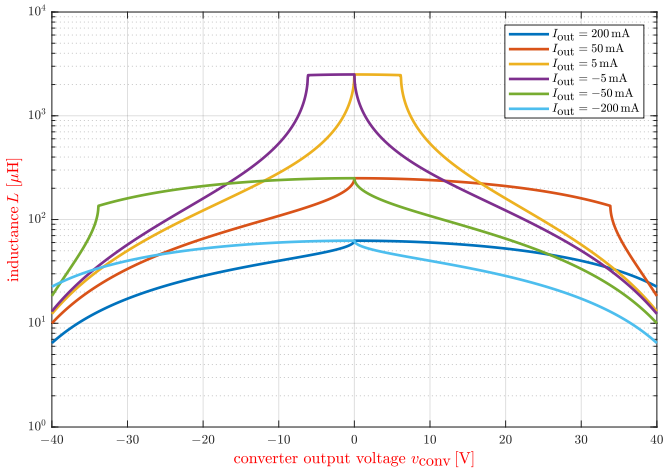

Fig. 6. Curves of the maximum value of the inductance that allow full ZVS transitions for all operating conditions.

C. Comparison of total semiconductor losses

Upon initial review of the FOM_1 and FOM_2 of the selected devices (Fig. 4), the conclusion is that the devices EPC2012C and EPC2010 show the worst behavior and EPC2033 and EPC2046 the best behavior. The devices listed in Fig. 4 are not all designed for the same application, but the total power loss that each one of these devices can contribute to the system for

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a specific application is not clear in advance. Since the off-the-shelf devices have been used, the application-driven design process of the transistors could not be afforded. The considered eGaN devices from EPC that accomplish $V_{\mathrm{DS,max}}$-$I_{\mathrm{D,max}}$ ratings of the system with a standard 20% derating are listed in Fig. 7. In order to evaluate the predicted performance, the total power losses in these devices are calculated for a representative test case: a symmetrical trapezoidal voltage wave at the TPS output with the maximum steady-state voltages of $\pm 40\,\mathrm{V}$ and with a slew-rate of $1\,\mathrm{V}/\mu\mathrm{s}$. The switching frequency in all cases is $1\,\mathrm{MHz}$. It is assumed that all the devices have ZVS in the steady-states which is allowed by the proper value of the inductance L, calculated in each case according to (6) and (7). The previous will inevitably increase the inductor current ripple for the devices with high C_{oss}, thus provoking more conduction losses in the devices and also in the inductor.

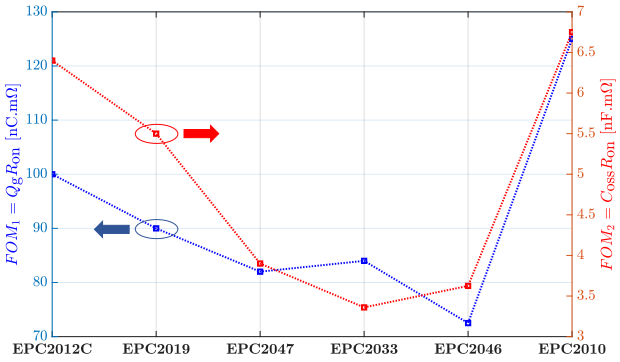

Fig. 7. Figures of merit of the considered GaN power transistors.

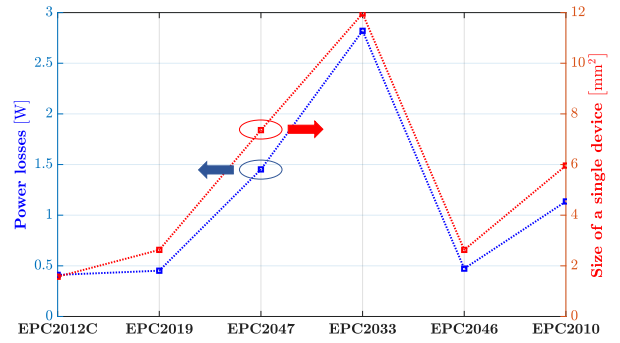

Fig. 8. Estimated power losses in the considered GaN power transistors.

Due to the specific operating conditions of the TPS, where the transistor have to block relatively high voltage (100 V), switching at 1 MHz and to conduct relatively small amount of DC current (200 mA in the steady-states) which is well bellow the absolute maximum current of the selected devices, the devices with the lower parasitic input and output capacitances show better behavior, as can be seen in Fig. 8. Surprisingly, the devices with very low FOMs, such as EPC2047 and EPC2033 exhibit the worst behavior regarding the power losses, while the EPC2012C although with the highest FOMs shows superior behavior. Moreover, this device has the smallest size among all the candidates and for that reason is selected, as the size is one of the most important constraints in the design. According to this analysis, the final choice of the GaN devices based on the FOM data only, may bring to a wrong conclusion, since the total estimated power losses are not in a proportion with both FOM_1 and FOM_2. The final decision has to be made when all the specifics of a certain application have been taken into account, such as ZVS operation and the output voltage and the load conditions in this design.

IV. Optimal Design of the Output Filter

The idea of the two-stage passive filter originates from the specification for the very low output voltage noise. Additionally, some other static and dynamic specification have to be met in the design. As described in previous section, the value of the first filter inductance (Fig. 2) is calculated so that the ZVS is possible in all the steady-states, under all load conditions. The rest of the passive components in the output filter has to be designed accordingly, in order to fulfill several specifications, that can be summed up in the following points:

- Firstly, the TPS must be able to track the voltage references with the slew-rates up to $2\,\mathrm{V}/\mu\mathrm{s}$. It is shown that the maximum slew-rate is basically limited by the maximum allowed capacitive current during the transients, defined by the maximum continuous drain current of the switching devices, which is 5 A in this case.
- The output voltage noise has the upper limit defined by the maximum permissible noise level at the LPA output and by the LPA's PSRR at the high frequencies ($f \geq f_{\mathrm{sw}}$). In this case, the minimum acceptable attenuation introduced by the output filter is 60 dB. The second filter stage employs $R_{\mathrm{d}}-L_{\mathrm{d}}$ series damping, instead of shunt $R_{\mathrm{d}}-C_{\mathrm{d}}$ [26], because the latter would lead to more pronounced transient capacitive currents, which is explained in the next subsection.
- In the case of a load step, the output voltage of the TPS must maintain its value in the safety margin defined by the auxiliary offset supply voltages, which mostly depends on the open-loop filter output impedance. In this design it is adopted that for the load step of 0.5 A, the maximum transient output voltage dip does not exceed 2 V.
- Finally, the second filter stage which provides additional attenuation of the switching noise and introduces a phase lagging in the loop gain of the control system below the second resonance frequency as well. Since the bandwidth of the control loop is designed to be sufficiently faster than the resonance frequency of the first filter stage, the first resonance is damped by the means of the control loop. That means that the second resonance of the output filter must be damped with a lossy passive element (a damping resistor R_{d}). In all calculations it is is assumed that the double control scheme is employed: an inner current loop based on the peak limiting current control, which is in charge of the current of the first inductor L, with the model based on the approach from [27], while the output voltage of the second capacitor C_2 is controlled by an outer conventional PI regulator. The targeted crossover frequency of the closed loop system

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is 100 kHz. All the designs with the relatively large overshoot in the step response ($> 10\%$) and a relatively low phase margin ($PM < 50\,^{\circ}$) are discarded.

All of these calculation are performed numerically by means of Laplace transformation, in order to avoid simplifications possibly leading to a wrong or non-optimal results and the potential candidates are first verified in simulation. In order to present all results in a systematic and organized way, the concept of the design space (DS) is employed [4], [28], based on the aforementioned requirements.

A. Problem with capacitive currents and nonlinear constraints

A typical waveform of the averaged inductor current (averaged on the switching period T_{sw}) is shown in Fig. 9. During the steady states, this current is equal to the output current of the TPS and the LPA. Nevertheless, during the transients it may significantly increase or decrease, depending on the type of the transition at the v_{conv}. If the output voltage rises with a slew-rate $SR_1 = \frac{V_2 - V_1}{\Delta t_1}$, than the average value of the current increases to $i_1 = i_{\text{out}} + SR_1\, C_{\text{tot}}$, while in the event of the falling edge of v_{conv} with a slew-rate $SR_2 = \frac{V_2 - V_1}{\Delta t_2}$, the average current reduces to $i_2 = i_{\text{out}} - SR_2\, C_{\text{tot}}$. The C_{tot} denominates the total output capacitance of the filter equal to $C_{\text{tot}} = C + C_{\text{f}}$. The estimation of the transient currents is based on the small-ripple approximation of both voltages of the capacitors C and C_{f}. One may notice that the average transient current i_{Lf} of the second filter inductor L_{f} and the parallel section of the damping elements L_{d}, R_{d} depends only on the value of the capacitor C_{f}. This circumstance is used as the advantage, so that with the proper arrangement of C and C_{f} the second stage has to support much lower transient current and both L_{f} and L_{d} can be small off-the-shelf components. On the other hand, the inductor L has to support a high ripple, to allow the ZVS operation in steady states, and also additional current during the transients, and it must be carefully designed custom made inductor. It is important to keep the transient capacitive current as smaller as possible hence it has an important impact on the losses in the TPS. During the transitions, ZVS is partially or completely lost, depending on how fast the transitions are, because of the insufficient current ripple. This leads to increase in both the conduction and switching losses in the devices, but also to the increase in the winding and core losses in the inductor. Moreover, the inductor L must be designed in order not to saturate for large excursion of the flux in the core during the transient. Although the transitions last only a tenth of the steady-state time, they have a significant impact on overall system losses, thus in reducing the system efficiency.

Having in mind the system specifications regarding the output voltage range and the maximum slew-rate of $2\,\text{V}/\mu\text{s}$, the maximum expected large signal bandwidth of the TPS is defined by the following expression [29]:

$$f_{\text{LS, max}} = \frac{SR_{\text{max}}}{0.8 \times 2\pi \frac{V_{\text{out, max}}}{\sqrt{2}}} \approx 14\,\text{kHz}. \tag{8}$$

This value is significantly smaller than the value of the small-signal bandwidth of the converter, mainly due to limited current carrying capability of the converter and not due to the filter design. The maximum transient current limit represents an imposed non-linear constraint regarding the large signal response of the output voltage.

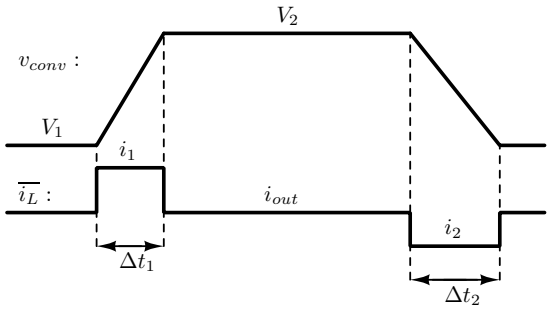

Fig. 9. Average inductor current during the transitions and the steady-states of the output voltage. The rise time and the fall time of the inductor current are neglected, since they are much smaller compared to the times Δt_1 and Δt_2.

It has already been stated that the second stage solution was motivated due to the specification for 60 dB for the minimum attenuation provided by the output filter. This assertions can be easily clarified by a simple calculation. For the specified attenuation at the given switching frequency of 1 MHz, the resonance frequency of the single stage LC filter is located around 31.6 kHz, which leads to the output capacitor value of $4.22\,\mu$F. In another words, with this design the inductor should support additional 8.44 A of average current, during a transition with a slew-rate of $2\,\text{V}/\mu\text{s}$, which is completely unacceptable. As can be seen, the fast analysis based on second DS constraint only is enough to explain why the single stage passive filter is not the appropriate solution and that the output filter must be distributed in two stages.

B. Final design of the output filter

After the design space analysis based on the aforementioned constraints, the combination of elements that fulfills all the criteria has been chosen, as can be seen in Table III. Total occupied footprint space of the components in the filter is about $2.7\,\text{cm}^2$ that gives only of 27% contribution to the total maximum occupied area of the power stage, while the total volume of the components is about $2.05\,\text{cm}^3$. The measured and calculated input to output transfer function of the designed output filter, showing the good agreement of the values until 1 MHz when unforeseen parasitics start to dominate, as can be seen in Fig. 10. The calculated attenuation of 66.4 dB at 1 MHz with modeled circuit parasitics corresponds to 62.2 dB of measured attenuation at the same frequency, which results in a discrepancy of 4.2 dB.

V. Comparison of the High Frequency Inductors

In this type of applications it is hard to find the optimal solution for the inductor design for all the possible test cases, especially for the converters operating at MHz switching frequencies [30]. Nevertheless, the symmetrical trapezoidal test waveform, with the maximum slew-rate of the edges of $2\,\text{V}/\mu\text{s}$ and with the steady-states that last at least ten

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TABLE III
THE VALUES AND THE HARDWARE REALIZATION OF THE OUTPUT FILTER ELEMENTS

component	value	hardware realization	occupied footprint space [mm^2]	total volume [mm^3]
L_1	6 μH	E13/7/4 core geometry	144	1872
C_1	1.3 μF	2 $\times$ TDK MLCC 1206	20.68	31.02
L_2	640 nH	Coilcraft XEL4030-641MEC	19.36	60.16
C_2	220 nF	Murata MLCC 1206	10.34	15.51
L_d	1.2 μH	Coilcraft XEL4020-122MEB	19.36	60.16
R_d	1.5 Ω	SMD 1% 0603	4.2	3.78

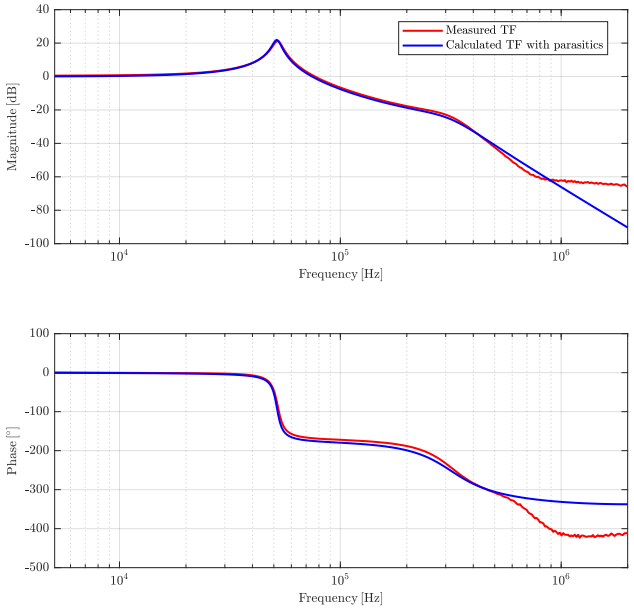

Fig. 10. Calculated and measured Bode plots of the input-to-output transfer function of the output filter.

times more than the transitions, is assumed as the most representative waveform, according to a specific application. The most critical point regarding the maximum magnetic flux density in the magnetic core and the maximum core and winding losses is when the output voltage is passing through 0 V, since the inductor current ripple is highest at that point and the DC bias current may have large value, depending how fast the transition is. This point is selected as the design case for the inductor L_1. The inductor design using enameled copper wires and three different core materials optimized for the high frequency domain is considered. Soft ferrite cores based on a manganese-zinc (MnZn) material are employed: Ferroxcube 3F46 and Hitachi Metals ML91S and ML91S. The overview of the core losses per volume for each one of the materials is given in Table IV, for a $f = 1$ MHz sine wave test at $T = 100$°C and the maximum flux density of $B_\mathrm{max} = 50$ mT. According to the datasheet data, the best performance regarding the core losses is expected of ML91S core material, since it has the minimal core loss per volume among these three high frequency materials.

The estimated power loss for the mentioned designed case and for the constant zero output voltage is calculated via improved generalized Steinmetz equation (iGSE) [31] for the

TABLE IV
A QUICK OVERVIEW OF THE CORE LOSSES PER VOLUME OF THE CHOSEN FERRITES AT $T = 100$°C AND THE MAXIMUM FLUX DENSITY OF $B_\mathrm{MAX} = 50$ MT

core material	P_v [$\frac{\mathrm{mW}}{\mathrm{cm}^3}$]
Ferroxcube 3F46	150
Hitachi Metals ML91S	100
Hitachi Metals ML95S	240

core losses, while the winding losses are calculated using the 3-D Finite Element Analysis (FEA) tool in Maxwell. For this case, where the dc inductor current has the value equivalent to a 2 V/μs transition at the output ($i_\mathrm{out} + SR\,(C + C_\mathrm{f}) = 3.7$ A) and the peak-to-peak current ripple has the maximum value (4.17 A) the estimated power loss is 1.03 W (0.18 W of core losses (3F46 material considered) and 0.85 W of winding losses). All the test cases for the inductors in this design are less aggressive.

Three inductors were made with the same winding arrangement and the same value of the air gap. The turns are more concentrated on the inner part of the legs, trying to move them from the vicinity of the air gap and hence to reduce winding losses in the inductors due to the fringing magnetic field from the gap, which can be consulted in Fig. 11.

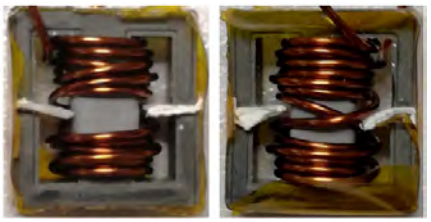

Fig. 11. A photograph of the designed inductor from both sides, E13/7/4 core geometry, $N = 13$, $\phi_\mathrm{Cu} = 0.6$ mm, $l_\mathrm{gap} = 0.35$ mm.

The power losses for each one of the inductors were compared for different load cases, having the maximum inductor temperature as the main performance indicator. Total power losses in the indcuctor are estimated on the basis of the maximum measured inductor temperate T_max, using the following equation:

$$P_\mathrm{loss} = \frac{T_\mathrm{max} - T_\mathrm{amb}}{R_\mathrm{th}} \tag{9}$$

where

$$R_{\text{th}} = 53 \cdot V_{\text{eff}}^{-0.54} = 90.799\,\frac{^{\circ}\text{C}}{\text{W}} \tag{10}$$

is the thermal resistance empirically obtained for EE cores, as explained in [4] and [32], $V_{\text{eff}} = 0.369\,\text{cm}^3$ is the effective core volume for E13/7/4 core geometry expressed in cm^3 and T_{amb} is the ambient temperature.

The overview of the tests that have been performed with the estimated values of the power losses in each one of the inductors is shown in Table V. Thermal images obtained by Fluke camera for two different test cases are shown in Fig. 12, where the case with the highest current ripple is presented and in Fig. 13. where the most aggressive test from the point of view of the converter dynamics is performed, with the maximum output voltage and the maximum output current. It can be concluded that the inductors based on ML91S and 3F46 materials have similar behavior in the majority of the test cases with the maximum inductor temperature below 90°C and below $0.7\,\text{W}$ of estimated power losses accordingly, while the one with ML95S material always exhibits more power losses that was also predicted by the preliminary datasheet data (Table IV).

VI. Control System Design

In order to achieve a fast, yet a stable enough response of the TPS, closed loop regulation of the system is implemented. In Fig. 14, a simplified schematic of the TPS with the control loops is shown. The switching network is replaced with the controlled voltage source v_{sw} loaded by the two stage output filter. The dynamics of the LPA is modeled with an independent current source i_{PA}, assuming that the closed-loop input impedance seen from the supply port is practically infinite. The output voltage v_{sens} is sensed and sampled via ADC converter. Digital proportional-integral regulator ($K_p + \frac{K_i}{1-z^{-1}}$) calculates the value of the control voltage v_{ctrl} once per switching period [33], which is the reference for the inner current loop. The regulator is designed to enable $100\,\text{kHz}$ small signal control bandwidth.

The current of the inductor L is controlled by the inner current loop, implemented as Peak Current Limiting Control, in order to provide high performances of the system regarding the dynamics. It is very well known that for the peak current-mode control when the duty cycle exceeds 50%, an external ramp slope is needed to avoid the subharmonic oscillation. According to the model proposed in [27] where this phenomena is mathematically explained, the system has a double-pole at half of switching frequency. In this implementation the compensation ramp is counter-based, generated digitally in the control board with the counter clock frequency N_r times higher than the switching frequency of the TPS. The compensated reference is then sent to DAC (N_b-bit data) and converted into an analog signal, which is compared with the sensed value of the inductor current, using an analog comparator. The output of the analog comparator produces a digital signal, as shown in Fig. 15, which is fed back to the FPGA and processed in the block for debouncing and dead-time control and finally sent to the drivers of the power transistors.

VII. Experimental Verification of the TPS Performance

The experimental setup of the TPS with all elements shown in Fig. 2 has been designed and tested. Complete hardware specifications of the fabricated prototype with the values of the passive components and part numbers are given in Table III and Table VI. In Figure 16 a photograph of the small daughter board with EPC2012C transistors, driver, auxiliary components and the output filter stage is demonstrated. The total occupied space of the TPS power stage, with the power transistors and the output filter is below $10\,\text{cm}^2$.

A representative test waveform that clarify the conclusions drawn in the subsection about ZVS operation is shown in Fig. 17 (the second quadrant operation, $v_{\text{conv}} = -40\,\text{V}$, $i_{\text{out}} = 10\,\text{mA}$). Two mechanism of partial ZVS that occur in PWM constant switching frequency converter are shown. The first one is related with insufficient energy for the complete charge displacement. The inductance L has value of about $15\,\mu\text{H}$, which is more than the maximum permissible for the complete ZVS for this operation conditions (Fig. 6). The switching node voltage v_{sw} (blue line) starts to increase when the LS switch is turned off. Since the inductor does not possess the minimum energy required for HS transistor discharging (6), the v_{sw} rises only $38\,\text{V}$, instead of needed $100\,\text{V}$ for the zero voltage turn-on of the HS transistor. The dead-time in this case is set to bee too long, more than $200\,\text{ns}$, to show the incapability for the complete ZVS transition. On the other hand, when HS transistor turns-off, the complete ZVS transition is possible, but the dead-time is not enough for the transition to finish. The LS turns-on with about $84\,\text{V}$. Both mechanisms of the incomplete parasitic output capacitance discharging can occur in the real situations, leading to the increased switching losses.

It has been mentioned before that the forward voltage of the internal diode of the e-GaN devices can have relatively big value. In this particular case, according to the reverse drain-source characteristic of the EPC2012C device, the source-to-drain voltage is about $2.75\,\text{V}$ for a $3\,\text{A}$ of source-to-drain current. In Fig. 18 two events with the diode conduction of the synchronous GaN device are shown. In the fist case, the interlocking dead-time is about $10\,\text{ns}$ longer than needed, while in the second case it is properly set. To get rid of the additional power loss in the devices due to the incorrect timing of the reverse conduction, variable dead-time control is implemented in this design to keep the diode conduction to the minimum.

Increased currents during the transients impact both switching losses because of the full hard switching, especially in the case of $2\,\text{V}/\mu\text{s}$ case (Fig. 19a), but also the conduction losses due to the increased dynamic on-state drain-to-source resistance R_{on} . In Fig. 19b, it can be clearly seen that the current increase of $4.6\,\text{A}$ results in the HS drain-to-source voltage collapse of about $2\,\text{V}$ (LS is conducting the current), which means that the average dynamic R_{on} is about $0.45\,\Omega$, about 4.5 times higher than the expected resistance from the datasheet [22]. This rough estimation is in accordance with the results from [34], [35]. It is also reported in [35] that depending on the off-state voltage and the switching frequency under hard or soft switching, dynamic R_{on} exhibit different

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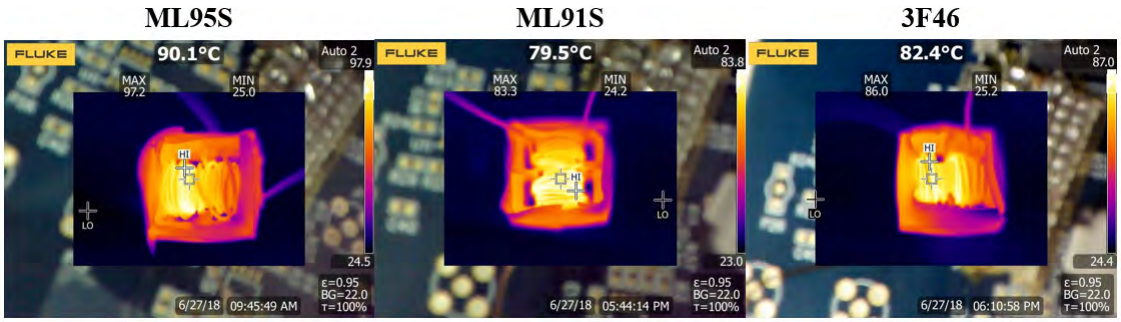


Fig. 12. Thermal camera images of the designed inductors for $v_{\text{conv}} = 0$ and $i_{\text{out}} = 200\,\text{mA}$ constant current load.

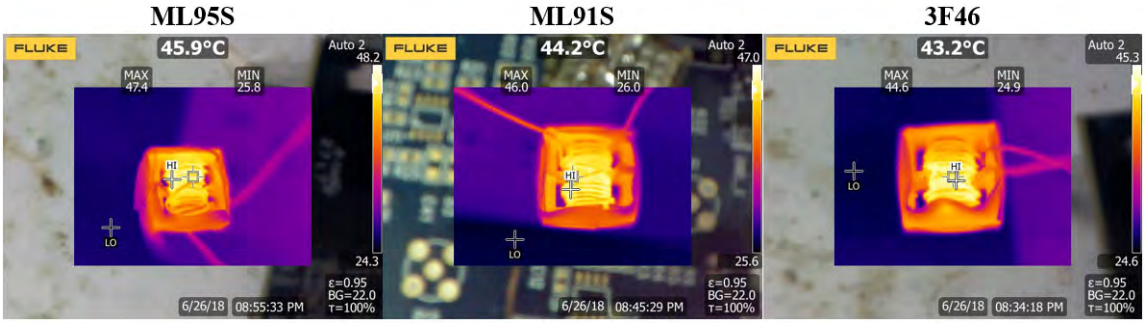


Fig. 13. Thermal camera images of the designed inductors for a $\pm 40\,\text{V}$, $2\,\text{V}/\mu\text{s}$ trapezoidal test waveform and $R = 200\,\Omega$ load.

TABLE V
THE OVERVIEW OF THE MEASURED TEMPERATURES AND THE ESTIMATED POWER LOSSES OF THE DESIGNED INDUCTORS FOR DIFFERENT TEST CASES

test case	Hitachi Metals ML95S		Hitachi Metals ML91S		Ferroxcube 3F46	
	T_{max} [°C]	P_{loss} [W]	T_{max} [°C]	P_{loss} [W]	T_{max} [°C]	P_{loss} [W]
$v_{\text{conv}} = 0$, no load	92.1	0.739	90.3	0.719	85.6	0.667
$v_{\text{conv}} = 0$, $i_{\text{out}} = 200\,\text{mA}$	97.2	0.795	83.3	0.642	86.0	0.672
$\pm 40\,\text{V}$, $1\,\text{V}/\mu\text{s}$, no load	42.7	0.195	40.7	0.173	40.7	0.173
$\pm 40\,\text{V}$, $1\,\text{V}/\mu\text{s}$, $R = 200\,\Omega$ load	44.2	0.212	42.9	0.197	42.5	0.193
$\pm 40\,\text{V}$, $2\,\text{V}/\mu\text{s}$, no load	44.8	0.218	43.6	0.205	43.1	0.200
$\pm 40\,\text{V}$, $2\,\text{V}/\mu\text{s}$, $R = 200\,\Omega$ load	47.4	0.247	46.0	0.231	44.6	0.216

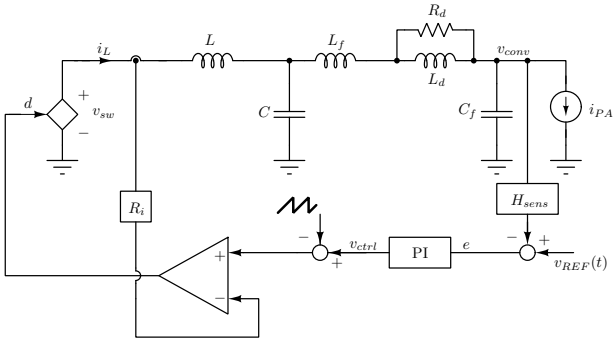


Fig. 14. A simplified schematic of the TPS with peak current mode control.

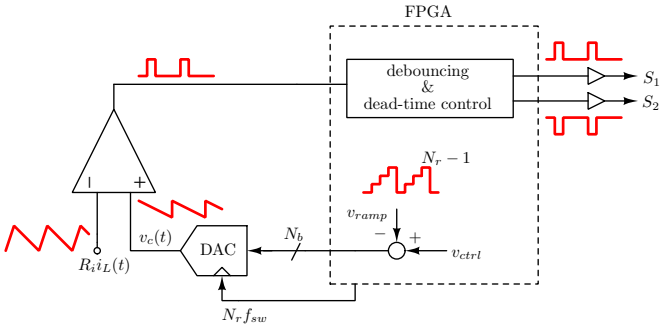


Fig. 15. Implementation of the employed peak current mode control.

behavior, due to different device technologies. This anomaly compromises the converter efficiency and in this case it gives a significant contribution to total power losses of the converter.

The steady-state power efficiency and the power losses of the TPS are measured at a wide range of the output power (form 0 to 8 W). The measured values are in a very good correspondence with the calculated values, with very small discrepancies. The TPS efficiency exceeds 94% for the high output power, while the total power losses inserted in the system are always smaller than 1.3 W, as can be observed from

TABLE VI
HARDWARE SPECIFICATIONS OF THE FABRICATED PROTOTYPE

parts	part numbers
power transistors	EPC2012C
gate driver	ADuM3223
power amplifier	Apex PA164
A/D converter	12-bit AD9627
D/A converter	14-bit AD9704
FPGA control board	Virtex-5

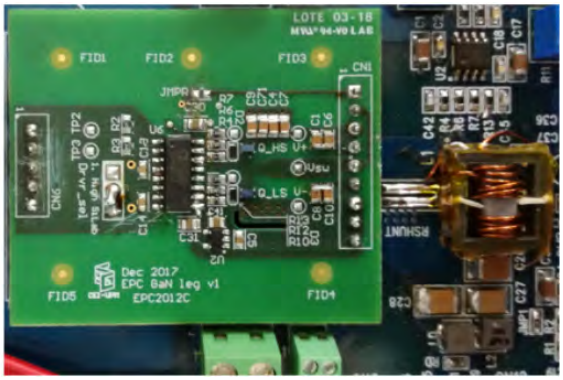


Fig. 16. A photograph of the designed TPS with the GaN EPC2012C power transistors and the output filter.

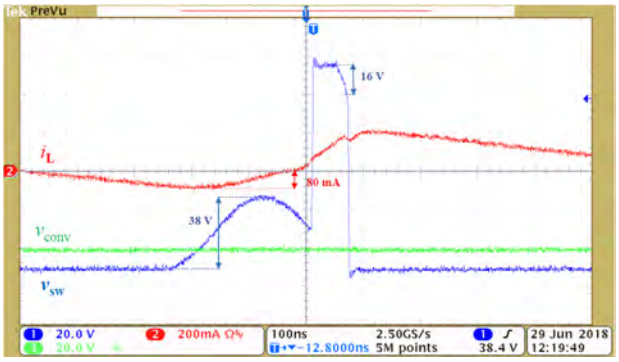
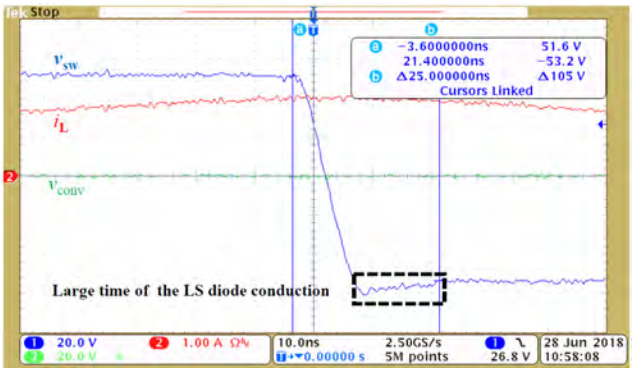
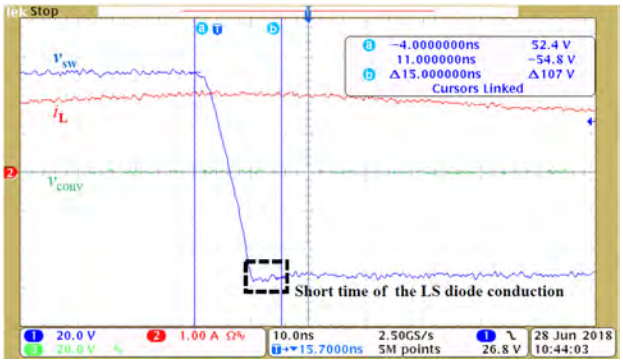


Fig. 17. Two mechanisms of partial ZVS with the waveforms of the switching node voltage v_{sw} (scale: 20 V/div), the current of the inductor L_1 (scale: 200 mA/div) and the TPS output voltage v_{conv} (scale: 20 V/div). Time scale: 100 ns/div (the same labels for the waveforms and the same line colors are used are used in Fig. 18 and 19).

Fig. 20. This figure shows the efficiency and the corresponding power losses for different levels of the output power (up to 8 W), for the same resistive load (around 200 Ω) and different levels of constant output voltage (0 to 40 V). The maximum output power of the converter in the steady states is 8 W according to the specifications from Table I. Nevertheless, for a variable output voltage (Fig. 3, Fig. 9) the power switches and the inductor L have to support much higher currents during the transient, due to the charging/discharging of the capacitors in the output filter. Therefore, both powers switches, because of the increased power dissipation during the transients and thermal issues of the devices, and the inductor L, because of the potential core material saturation, are over-sized for a much higher average current (around 3.6 A) than the nominal output current (200 mA). Due to this, the local maximum

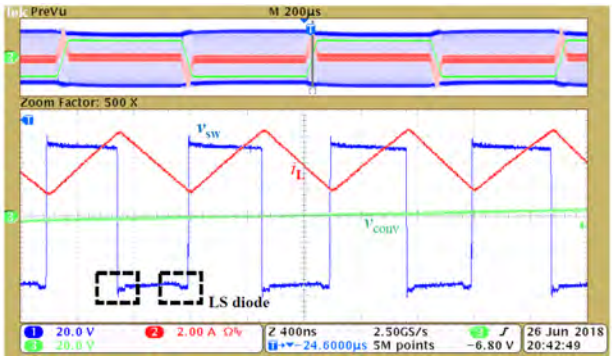


(a) An example of incorrect timing of the LS diode conduction.

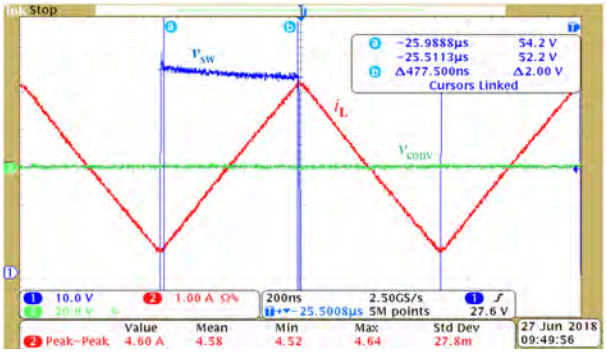


(b) An example of correct timing of the LS diode conduction.

Fig. 18. LS GaN parasitic diode conduction after the complete ZVS transition.



(a) Hard switching during the output voltage transition, $SR = 2$ V/μs.



(b) Drain-to-source on-state voltage drop due to the dynamic on-state resistance.

Fig. 19. Two additional contribution to the total power losses: hard switching during the transients (a) and dynamic on-state resistance (b).

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of the efficiency curve in whole range of the steady-state output power does not exist. Additionally, in the case of the higher output voltage the current ripple is smaller and maximum current ripple occurs at the zero output voltage. The higher the output voltage is, the smaller the current ripple and smaller conduction losses in both power transistors and passive components and core losses in the inductor are. Therefore, the efficiency curve is monotonically increasing and power loss curve is monotonically decreasing in the whole range of the output power shown in Fig. 20.

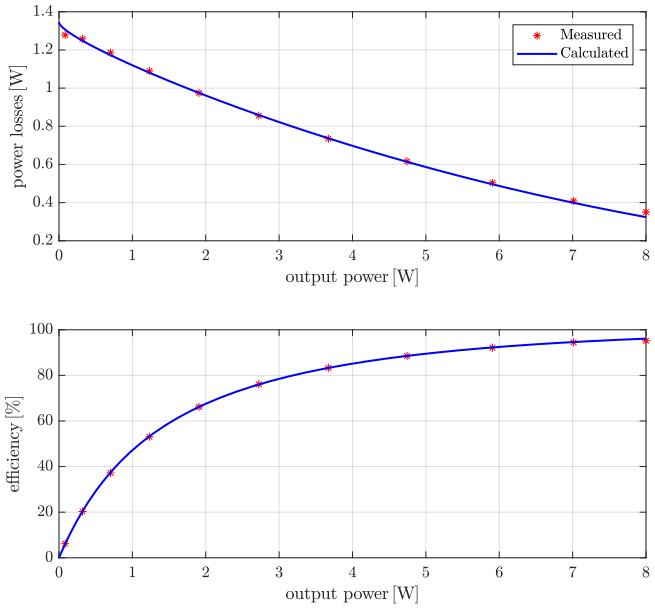

Fig. 20. Calculated and measured TPS steady-state power losses and efficiency versus the output power.

In Table VII the values of the estimated and measured power losses in the TPS for different test cases are exposed. The highest power loss is observed for the zero output voltage since due to high peak-to-peak excursion of the inductor current (around 4.5 A) and consequently increased conduction losses.

Finally, the TPS is tested together with the LPA for various dynamic characteristics of the output voltage references in the closed loop. In Fig. 21, the waveforms of the converter output voltage v_{conv}, both supply rails $v_{\text{s+}}$, $v_{\text{s-}}$ and the LPA output voltage in the case of a 1 V/μs trapezoidal test signal are shown. The steady-state output voltages and the output current are at the specified maximums (Table I). The auxiliary offset supply voltages (see Fig. 2) are set to $V_{\text{off}} = 5\,\text{V}$, which is enough to avoid nonlinearities at the LPA output due to any inaccuracy in the v_{conv}. Experimental waveforms with trapezoidal voltage references and different types of loading (resistive and capacitive load) are given in Fig. 22-23. Additionally, a test with sine wave reference and a capacitive load is shown in Fig. 24. The four-quadrant operation with these tests is completely experimentally proven, since all four voltage-current combinations are present in the aforementioned waveforms.

Power savings in the system with the TPS up to 4 W are obtained, depending on the load type and the output voltage range (see Fig. 25). It is worth noting that, for example, in the fourth test case ($\pm 40\,\text{V}$, 1 V/μs, $R = 200\,\Omega$), the maximum case temperature of the GaN devices is about 45 °C without any force cooling, while it increases to 120 °C when the partial ZVS due to the short dead-time occurs.

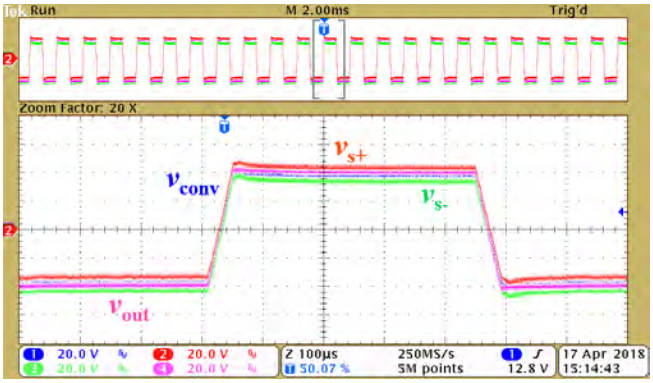

Fig. 21. Closed loop response of the system in the case of a 1 V/μs trapezoidal test signal, CH1: the TPS output voltage v_{conv} (blue), CH2: positive supply rail voltage $v_{\text{s+}}$ (red), CH3: negative supply rail voltage $v_{\text{s-}}$ (green), CH4: the LPA output voltage v_{out} (pink). Voltage scale: 20 V/div, time scale: 100 μs/div.

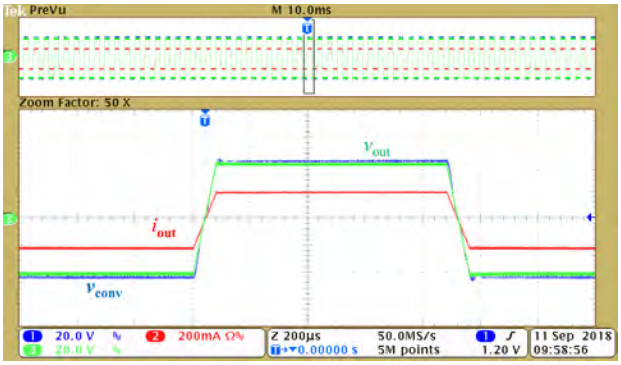

Fig. 22. Closed loop response of the system in the case of a 1 V/μs trapezoidal test signal and a 200 Ω resistive load, CH1: the TPS output voltage v_{conv} (blue), CH3: the LPA output voltage v_{out} (green), CH2: the LPA output current (red). Voltage scale: 20 V/div, time scale: 200 μs/div.

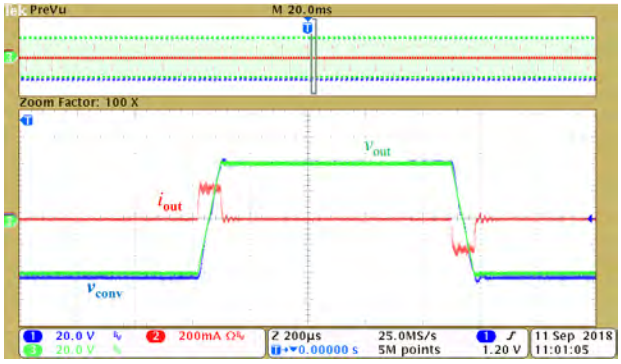

Fig. 23. Closed loop response of the system in the case of a 1 V/μs trapezoidal test signal and a 550 nF capacitive load, CH1: the TPS output voltage v_{conv} (blue), CH3: the LPA output voltage v_{out} (green), CH2: the LPA output current (red). Voltage scale: 20 V/div, current scale: 200 mA/div, time scale: 200 μs/div.

For a sake of clarity of the improvement in the LPA performance by modulating its supply rails via the TPS, the

TABLE VII
THE OVERVIEW OF THE ESTIMATED AND MEASURED POWER LOSSES IN THE TPS FOR DIFFERENT TEST CASES

test case	P_{out} [W]	estimated P_{loss} [W]	P_{loss} [W]	efficiency [%]
$v_{\text{conv}} = 0$, no load	0	1.34	1.20	0
$v_{\text{conv}} = 0$, $i_{\text{out}} = 200\,\text{mA}$	0	1.37	1.25	0
$\pm 40\,\text{V}$, $1\,\text{V}/\mu\text{s}$, no load	0	0.42	0.45	0
$\pm 40\,\text{V}$, $1\,\text{V}/\mu\text{s}$, $R = 200\,\Omega$ load	7.13	0.48	0.50	93.40
$\pm 40\,\text{V}$, $2\,\text{V}/\mu\text{s}$, no load	0	0.72	0.79	0
$\pm 40\,\text{V}$, $2\,\text{V}/\mu\text{s}$, $R = 200\,\Omega$ load	7.13	0.80	1.02	87.48

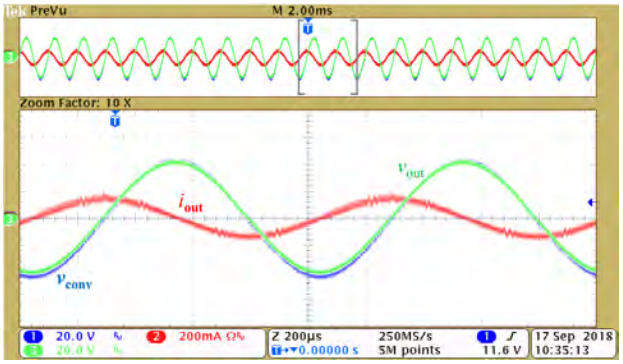

Fig. 24. Closed loop response of the system in the case of a 1 kHz sinusoidal test signal and a 220 nF capacitive load, CH1: the TPS output voltage v_{conv} (blue), CH3: the LPA output voltage v_{out} (green), CH2: the LPA output current (red). Voltage scale: 20 V/div, current scale: 200 mA/div, time scale: 200 μs/div.

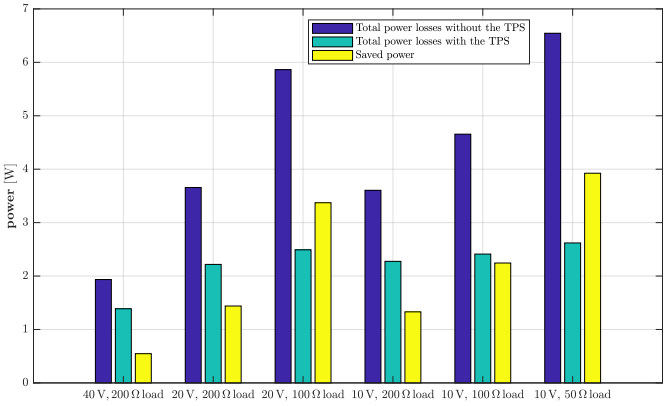

Fig. 25. Comparison of the total power losses in the system with and without the TPS, with the corresponding power savings in the most common test cases, the voltage levels correspond to the amplitude voltage of a 1 V/μs trapezoidal tests.

case temperatures of Apex LPA are shown for the test case of 10 V, 50 Ω load and also without any heat-sinks. The LPA case temperature in the system with the TPS is only 37.9 °C, while without the TPS the temperature it exceeds 120 °C. In other words, the LPA alone without the TPS cannot operate safely unless a big enough heat-sink is not placed because of the high power dissipation.

According to the estimated and measured values of power losses in whole system, power loss breakdown is calculated (Fig. 27), for two tests with the maximum output voltage swing ($\pm 40\,\text{V}$, 200 Ω load and two different slew-rates

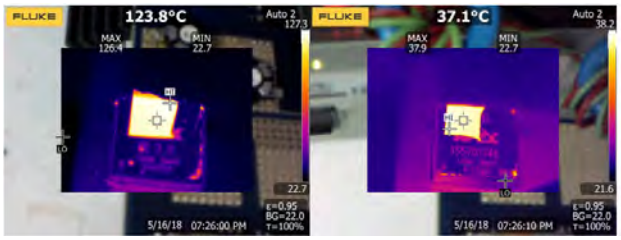

Fig. 26. Thermal camera images of the Apex LPA PA164 in the case the constant voltage supplies (left) and with the TPS (right) in the case of $\pm 10\,\text{V}$ $1\,\text{V}/\mu\text{s}$ trapezoidal tests and $50\,\Omega$ load.

(1 V/μs and 2 V/μs). In both cases, the losses in the LPA dominate (over 60% of the total power loss). Regarding the GaN devices, the conduction loss dominates over the switching and conduction losses, due to the increased dynamic on-state resistance, especially because high RMS currents occur in the transients. Total power loss contribution of the output filter is below 20% in both analyzed cases.

VIII. CONCLUSIONS

In this paper, high efficiency high bandwidth fully digitally controlled Tracking Power Supply (TPS) system for Linear Power Amplifiers (LPA) is shown, which can provide four quadrant operation. It is explained and backed up with the experimental results that Enhancement-mode Gallium-Nitride High-electron-mobility Transistors (GaN E-HEMTs) with employed ZVS enable design of a small, compact and low weight two-level DC-AC power converter. The converter operates at 1 MHz switching frequency and the input voltage of 100 V, providing the maximum output power of 8 W. Using traditional Silicon based devices, a design with such a high switching frequency, high input voltage and very stringent occupied area requirement ($< 10\,\text{cm}^2$) would not be possible. ZVS operation of the GaN devices is not only important because of the system efficiency, but also plays the important role in the thermal management of the devices, due to the poor junction to ambient thermal impedance of the packaging. Since the ZVS is a key enabler of a high efficiency and reliable design, the RMS value of the current is higher than in the case when hard switching is allowed. Therefore, the inductor design is also very sensitive point. For that purpose, the performance of the inductors based on three manganese-zinc (MnZn) ferrites with less pronounced core losses are compared and the power losses in the inductor are optimized for the worst case. The rest of the passive components in the

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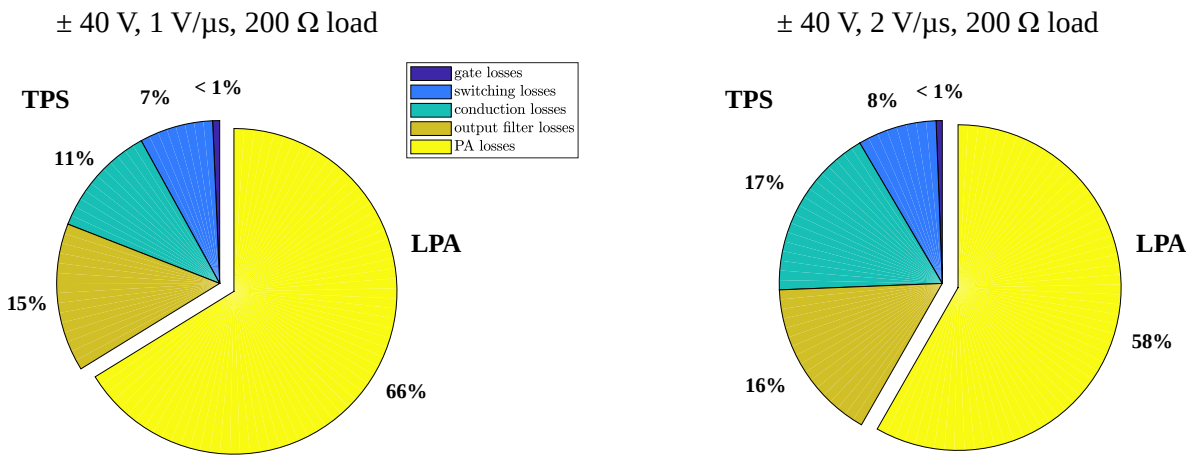

Fig. 27. Power loss breakdown for two test cases from Table VII, with the detailed power losses in the devices. The total power losses in each one of the cases are 1.45 W and 1.90 W, respectively.

two stage output filter are dimensioned with the fixed value of the inductor that allows complete ZVS in all the steady-states. It is illustrated that the TPS significantly improves the performance of the LPA, providing power savings up to 4 W in the experimental tests, which additionally reflects in the temperature difference of the LPA. Thanks to the employed TPS system, the measured temperature difference can arise beyond 80 °C. Consequently, the massive heat-sink of the LPA is completely removed.

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