Selecting eGaN® FET Optimal On-Resistance

Johan Strydom, Ph.D., V.P., Applications, Efficient Power Conversion Corporation

In this white paper the die size optimization process for selecting the eGaN FET optimal on-resistance is discussed and an example application is used to show specific results. Since 'optimum' means different things to different people, this process is aimed at maximizing switching device efficiency at a given load condition.

DEVICE LOSSES MODELING

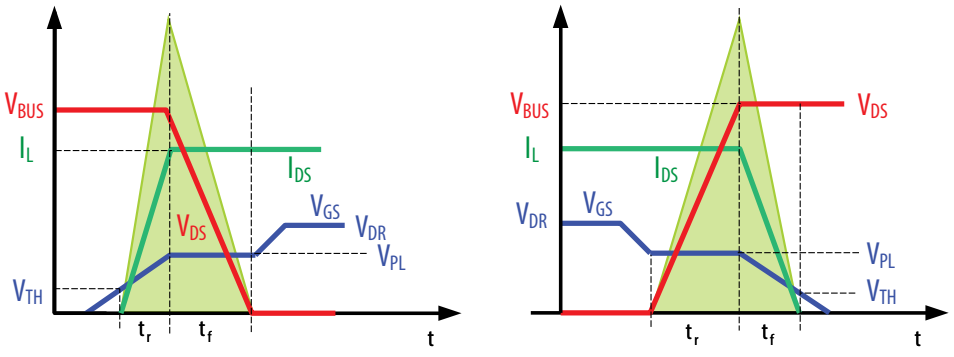
Previously published articles showed that eGaN FETs behave for the most part just like silicon devices and can be evaluated using similar performance metrics. Since these devices behave like silicon MOSFETs, they can also be optimized in a similar fashion; by balancing static and dynamic losses through adjusting die size. Static losses include loss components unaffected by changes in switching frequency, while dynamic losses are very much frequency dependent. An assumption is that all device parameters will scale with die size but that the device Figures of Merit (FOMs) will remain unchanged. Although applications may be varied, the different loss components are easily summarized [3, 4, 5]; only their relative sizes change with application and operating frequency. With eGaN FETs, the relative weights of the loss components will also differ from silicon MOSFETs and thus result in different 'optimum' die size values. To better understand this, lets first break down the total semiconductor losses within a power FET (P_{SEMI}) as follows:

$$P_{SEMI} = P_{COND} + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS} \quad (1)$$

where:

	Configuration	Equation
1	P_{COND} is the device channel conduction loss when on	$\left(I_L \cdot \sqrt{D}\right)^2 \cdot \frac{R_{DS(on),A}}{A}$
2a	$P_{T\text{-}ON}$ is the device turn-on commutation loss (Figure 1a)	$\frac{V_{BUS} \cdot I_L}{2} \frac{R_G \cdot (Q_{GD,A} + Q_{GS2,A}) \cdot A}{V_{DR} - V_{PL}} \cdot f_{SW}$
2b	$P_{T\text{-}OFF}$ is the device turn-off commutation loss (Figure 1b)	$\frac{V_{BUS} \cdot I_L}{2} \frac{R_G \cdot (Q_{GD,A} + Q_{GS2,A}) \cdot A}{V_{PL}} \cdot f_{SW}$
3	P_{DR} is the device gate drive loss	$Q_{G,A} \cdot A \cdot V_{DR} \cdot f_{SW}$
4	P_{QRR} is the device diode reverse recovery loss	$Q_{RR,A} \cdot A \cdot V_{BUS} \cdot f_{SW}$
5	P_{QOSS} is the device output capacitance charge loss	$\frac{Q_{OSS,A} \cdot A}{2} \cdot V_{BUS} \cdot f_{SW}$
6	P_{DIODE} is the device diode conduction loss	$I_L \cdot V_F \cdot \Delta t \cdot f_{SW}$

'A' refers to the normalized die area and subscript A refers to the parameter per normalized die area.
See appendix for terms, assumptions and approximations made.



(a) Turn-on (b) Turn-off

Figure 1: Idealized switching waveforms used for calculating switching loss.

Note that not all devices will have all these loss components, e.g. a synchronous buck converter would have practically no turn-on or turn-off losses in the synchronous rectifier. Furthermore, to optimize multiple devices in a converter, the losses stemming from the interaction between devices also need to be considered (e.g. the diode reverse recovery losses of one device may be dissipated in another FET. This occurs in circuits such as synchronous buck converters where synchronous FET related losses are dissipated in the control FET, but by optimizing the control FET only, this loss component will remain unchanged. Thus for optimization purposes, this issue is resolved by considering all the losses induced by a device to be relevant for its sizing, regardless of where the power is dissipated.

DIE SIZE OPTIMIZATION

By considering each of these device loss components in eq. (1) in turn, some conclusions can be drawn:

- The conduction losses (item 1) are frequency independent
- Commutation loss (items 2a and 2b) are both frequency and load current dependent and can be combined as follows:

$$P_{COMM} = \frac{V_{BUS}}{2} k \cdot Q_{SW,A} \cdot A \cdot I_L \cdot f_{SW} \tag{2}$$

where: $k = k_{ON} + k_{OFF}$, $k_{ON} = \frac{R_G}{V_{DR} - V_{PL}}$, $k_{OFF} = \frac{R_G}{V_{PL}}$ and $Q_{SW,A} = Q_{GD,A} + Q_{GS2,A}$

- Loss components in items 3, 4 and 5 are all frequency dependent, but current independent and can be combined. While Q_{RR} is current related, MOSFET vendors neglect to present their characteristic adequately over current, temperature and di/dt to accurately calculate these losses:

$$P_{CHARGE} = \left(\frac{Q_{OSS,A}}{2} \cdot V_{BUS} + Q_{G,A} \cdot V_{DR} + Q_{RR,A} \cdot V_{BUS} \right) \cdot A \cdot f_{SW} \tag{3}$$

- Diode losses, item 6, are assumed die size independent (only a weak function of die size) and neglected for the optimization process.

If we now define two new variables ΔI_{EQ} and ΔI_{EQRR} as:

$$\Delta I_{EQ} = \frac{Q_{OSS,A} \cdot V_{BUS} + 2 \cdot Q_{G,A} \cdot V_{DR}}{V_{BUS} \cdot k \cdot Q_{SW,A}} \tag{4a}$$

$$\Delta I_{EQRR} = \frac{2 \cdot Q_{RR,A}}{k \cdot Q_{SW,A}} \tag{4b}$$

Then combining eq. (2) and eq. (3) and substituting eq. (4a) and (4b), the switching losses are:

$$\begin{aligned} P_{SW} &= \left[\frac{V_{BUS}}{2} k \cdot Q_{SW,A} \cdot I_L + \left(\frac{Q_{OSS,A}}{2} \cdot V_{BUS} + Q_{G,A} \cdot V_{DR} + Q_{RR,A} \cdot V_{BUS} \right) \right] \cdot A \cdot f_{SW} \\ &= \left[\frac{V_{BUS}}{2} k \cdot Q_{SW,A} \cdot I_L + \frac{V_{BUS}}{2} k \cdot Q_{SW,A} \cdot \left(\Delta I_{EQ} + \Delta I_{EQRR} \right) \right] \cdot A \cdot f_{SW} \\ &= \left[\frac{V_{BUS}}{2} k \cdot Q_{SW,A} \right] \cdot \left(I_L + \Delta I_{EQ} + \Delta I_{EQRR} \right) \cdot f_{SW} \cdot A \\ &= P_{SW,A} \cdot A \end{aligned} \tag{5}$$

Thus the non-current dependent losses in eq. (3) can be modeled as an equivalent switching loss with an equivalent current ΔI_{EQRR} for reverse recovery related losses, and ΔI_{EQ} as the remaining charge related losses as defined in eq. (4). The Q_{RR} related losses term can be neglected for eGaN FETs where Q_{RR} is equal to zero, but is included for MOSFET compatibility. Thus from eq. (5) and item 1 from eq. (1), the total device losses for optimization purposes can be written as:

$$P_{SEMI}(A) = P_{SW,A} \cdot A + \left(I_L \cdot \sqrt{D}\right)^2 \cdot \frac{R_{DS(ON),A}}{A} \tag{6}$$

To find the optimum (minimum loss) point, we set the derivate to zero and calculate A:

$$\frac{dP_{SEMI}(A)}{dA} = 0 = P_{SW,A} - \left(I_L \cdot \sqrt{D}\right)^2 \cdot \frac{R_{DS(ON),A}}{A^2}$$
$$\therefore A = I_L \cdot \sqrt{D} \cdot \sqrt{\frac{R_{DS(ON),A}}{P_{SW,A}}} \tag{7}$$

If we normalize all charge values to 1 Ω $R_{DS(on)}$, then the optimum device on-resistance is given by:

$$R_{OPT} = \frac{1}{I_L \cdot \sqrt{D}} \cdot \sqrt{\left[\frac{V_{BUS}}{2} k \cdot Q_{SW,A}\right] \cdot \left(I_L + \Delta I_{EQ} + \Delta I_{EQRR}\right) \cdot f_{SW}} \ \ \Omega \tag{8}$$

The normalized eGaN FET device specific parameters are given in Table 1 for a typical 'hot' operating temperature of 100 °C junction. Thus with eq. (8) and the values from Table 1, the optimum required die resistance can be readily calculated for a given bus voltage.

Normalize to typical $R_{DS(on)}$ at 100°C (~1.45 x $R_{DS(on)}$ at 25°C)				
	40 V eGaN FETs	40 V eGaN FETs	100 V eGaN FETs	200 V eGaN FETs
V_{BUS}	12 V	24 V	48 V	100 V
$Q_{GS2,A}$ @ rated I_{DS}	5 pC/Ω	5 pC/Ω	7 pC/Ω	13 pC/Ω
$Q_{GD,A}$ @ V_{BUS}	9 pC/Ω	10 pC/Ω	21 pC/Ω	51 pC/Ω
$Q_{G,A}$ @ 5 V rated V_{DR}	46 pC/Ω	46 pC/Ω	73 pC/Ω	145 pC/Ω
$Q_{OSS,A}$ @ V_{BUS}	57 pC/Ω	97 pC/Ω	290 pC/Ω	1085 pC/Ω
$Q_{RR,A}$ @ rated I_S	0 pC/Ω	0 pC/Ω	0 pC/Ω	0 pC/Ω
V_{PL} @ rated I_{DS}	2.2 V	2.2 V	2.3 V	2.4 V
V_F @ rated I_{DS}	2.2 V	2.2 V	2.3 V	2.4 V
$k_{ON} = \frac{R_G}{V_{DR}-V_{PL}}$	2.6/2.8 = 0.93 2 Ω pull up	2.6/2.8 = 0.93 2 Ω pull up	2.6/2.8 = 0.96 2 Ω pull up	2.6/2.8 = 1.0 2 Ω pull up
$k_{OFF} = \frac{R_G}{V_{PL}}$	1.1/2.2 = 0.5 0.5 Ω pull up	1.1/2.2 = 0.5 0.5 Ω pull up	1.1/2.3= 0.48 0.5 Ω pull up	1.1/2.4= 0.46 0.5 Ω pull up
$k = k_{ON} + k_{OFF}$	1.43 / A	1.43 / A	1.44 / A	1.46 / A
$Q_{SW,A}$	14 pC/Ω	15 pC/Ω	28 pC/Ω	64 pC/Ω
ΔI_{EQ}	4.0 A	5.0 A	7.7 A	12.4 A
ΔI_{EQRR}	0 A	0 A	0 A	0 A

Table 1: eGaN FETs normalized to 1 Ω typical $R_{DS(on)}$ for difference voltage ratings.

This process may best be explained by example, but first the decision as what load conditions are to be used for optimization must be chosen. To explain this, consider the following sets of efficiency curves for the same application shown in Figure 2.

- Full Load Optimization: will result in the best full load efficiency at the cost of reduced light load and peak efficiency.
- Medium Load Optimization: will result in the best medium load efficiency at the cost of full load efficiency. This is likely to result in the most 'flat' efficiency curve.
- Light Load Optimization: Best light load efficiency achieved at a significant cost of full load efficiency. May be useful where certain light load efficiency standards need to be met or minimum energy consumption standards need to be met.

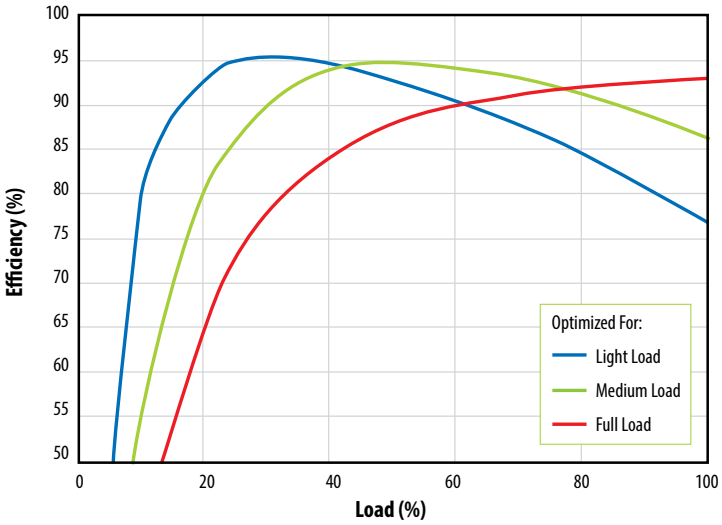


Figure 2: Conceptual efficiency curves optimized for difference load conditions.

Thus the load current should be chosen based on where on the efficiency curve should peak (or as close as possible). This selection is complicated by the fact that the device losses are not the only current dependent circuit losses, i.e. bussing resistance and inductor DCR also increase quadratically with load current. Thus the die size optimization should be skewed towards higher dynamic losses to compensate, but with multiple devices each device can account for some arbitrary fraction of the total circuit resistance losses. If R_{EQ} is an equivalent circuit resistance to be compensated for, then the adjusted optimum on-resistance ($R_{OPT-ADJ}$) is given by:

$$R_{OPT-ADJ} = \frac{\frac{P_{SW,A}}{I_L^2}}{\left(\frac{R_{EQ}}{2} + \sqrt{\left(\frac{R_{EQ}}{2}\right)^2 - \frac{P_{SW,A}}{I_L^2}\cdot D}\right)}\ \Omega \qquad (9)$$

eGaN FET OPTIMIZATION EXAMPLE

Consider a high frequency Buck converter with the following specifications [6]:

V_{IN} = 45 V, V_{OUT} = 22 V, f_{SW} = 1 MHz, I_{LMAX} = 30 A

For optimization, peak die or circuit efficiency is to be achieved at 15 A (50% load). From Table 1, we get ΔI_{EQ} = 7.7 A, ΔI_{EQRR} = 0 A, k = 1.44 /A and $Q_{SW,A}$ = 28 pF / Ω (using the 48 V). Also needed are D = 22/45 = 0.49 and I_L = 15A.

For the adjusted optimum on-resistance a total equivalent circuit resistance of 8 mΩ is estimated from [6]. Since the high-side control FET losses dominate total device losses, lets arbitrarily choose 7 mΩ of this be compensated for in the high-side. Since equivalent resistance losses are compensated by increasing switching losses, it makes sense to compensate most (if not all) of these losses in the device with higher switching loss.

A) Control FET optimization

For the control FET, the on-state duty cycle is 'D', there are no Q_{RR} losses, but there are Q_{OSS} and hard switching losses. Thus from eq. (9) we get:

$$R_{OPT}(100°C) = \frac{1}{15A\cdot\sqrt{0.49}}\cdot\sqrt{\left[\frac{45V}{2}1.44/A\cdot 28pF/\Omega\right]\cdot(15A+7.7A+0A)\cdot 1MHz}$$

$$R_{OPT}(100°C) = \frac{1}{15A\cdot\sqrt{0.49}}\cdot\sqrt{0.0206W\Omega} = 14.1m\Omega$$

thus R_{OPT}(25°C) = ~9.7 mΩ typical

Considering the equivalent circuit resistance, the adjusted optimum on-resistance is from eq. (9)

$$R_{OPT-ADJ}(100°C) = \frac{0.0206W\Omega / 15A^2}{\left(\frac{7m\Omega}{2} + \sqrt{\left(\frac{7m\Omega}{2}\right)^2 + 0.0206W\Omega \cdot 0.49/(15A)^2}\right)} = 8.3m\Omega$$

thus $R_{OPT-ADJ}$ (25°C) = ~5.7 mΩ typical

B) Synchronous FET optimization

For the synchronous FET, the load current I_L at switching is taken as zero, while there are no turn-on or turn-off commutation losses in the synchronous FET, Q_{OSS} induced losses and Q_{RR} losses are present (zero for eGaN FET). Also the on-state duty cycle is '1-D'. Thus from eq. (9) we get:

$$R_{OPT}(100°C) = \frac{1}{15A \cdot \sqrt{0.51}} \cdot \sqrt{\left[\frac{45V}{2} 1.44/A \cdot 28pF/\Omega\right] \cdot (0A + 7.7A + 0A) \cdot 1MHz}$$

$$R_{OPT}(100°C) = \frac{1}{15A \cdot \sqrt{0.51}} \cdot \sqrt{0.007W\Omega} = 7.6m\Omega$$

thus R_{OPT} (25°C) = ~5.2 mΩ typical

Considering the equivalent circuit resistance, the adjusted optimum on-resistance is from eq. (9) for the remaining 1 mΩ:

$$R_{OPT-ADJ}(100°C) = \frac{0.007W\Omega/(15A)^2}{\left(\frac{1m\Omega}{2} + \sqrt{\left(\frac{1m\Omega}{2}\right)^2 + 0.007W\Omega \cdot 0.51/(15A)^2}\right)} = 6.2m\Omega$$

thus $R_{OPT-ADJ}$ (25°C) = ~4.3 mΩ typical

As can be seen from this example, the optimum on-resistance changes significantly for any large (same range as the device on-resistances) additional circuit resistance being compensated for. Obviously, these additional circuit losses could be minimized prior to compensation and any such additional optimization adjustment would be minor. To see the impact of adjusting for some of the equivalent circuit resistance, the control FET and synchronous FET optimum resistance are plotted versus load current for this same example in Figures 3 and 4 respectively.

EXPERIMENTAL RESULTS

To evaluate the validity of this optimization approach, some experimental efficiency curves were taken for the same buck converter used in the example above [6]. The same circuit was built and only the EPC devices were changed, as outlined in Table 2, using various combinations of the EPC2001 [7] and EPC2016 [8] eGaN FETs. The efficiency and power loss curves as function of load current for these three cases are plotted and shown in Figure 5. Their estimated optimized points are color coded and added as dots to Figures 3 and 4. Table 2 shows good correlation between the adjusted on-resistance and actual current levels at peak efficiency.

OPTIMIZATION COMPARISON WITH MOSFETS

To see how this optimization process compares when using MOSFETs, it is necessary to find representative high performance MOSFETs and normalize them in a similar manner. The resultant values are given in the appendix, Table 3 for reference. Using the same design example as before, the resultant optimum on-resistance values for the control and sync FETs are plotted versus load current in Figures 6 and 7 respectively. The reverse recovery losses (Q_{RR}) for these MOSFETs taken from the datasheets are rather large and could be mitigated by the addition of a freewheeling Schottky diode. Therefore the resultant MOSFET on-resistance, neglecting Q_{RR}, losses is also shown in Figure 7. This clearly shows the similarity between eGaN FETs and MOSFETs and shows that an optimal eGaN FET would in all cases have a lower resistance than a similarly optimized MOSFET device. This results from the reduced dynamic losses offered by the eGaN FET due to its lower FOM [1].

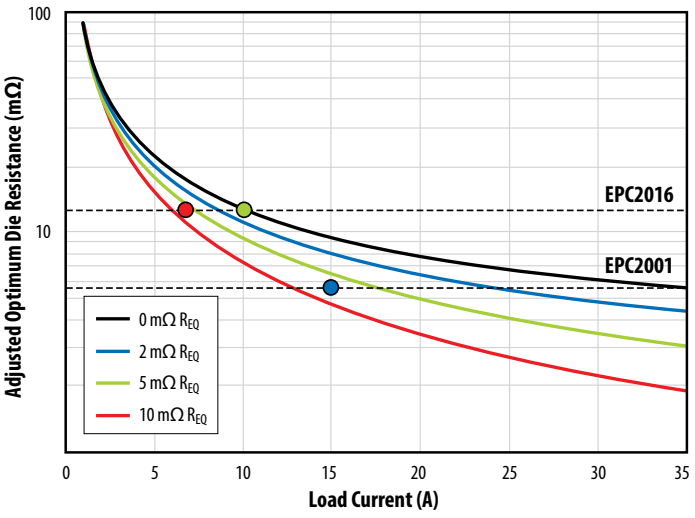


Figure 3: Adjusted optimum on-resistance (25 °C) for the control FET for a 45 V to 22 V / 1 MHz buck converter for varying values of equivalent circuit resistance REQ. Solid circles represent experimental test cases from Table 2.

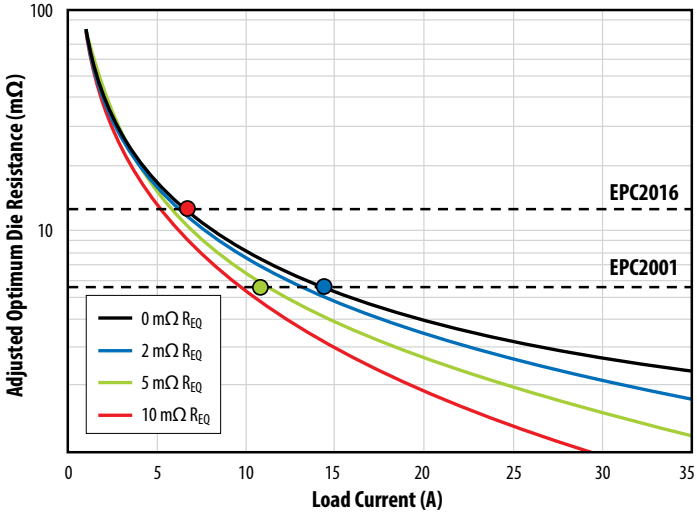


Figure 4: Adjusted optimum on-resistance (25 °C) for the synchronous FET for a 45 V to 22 V / 1 MHz buck converter for varying values of equivalent circuit resistance REQ. Solid circles represent experimental test cases from Table 2.

TESTED eGaN FET combinations	Load current at optimum on-resistance Equation (8)		Load current at adjusted optimum on-resistance (amount of R_{EQ} adjusted)		Load current at peak efficiency*
	Control FET	Sync-FET	Control FET	Sync-FET	
EPC2016 + EPC2016	10.6 A	6.8 A	6.8 A (8 mΩ)	6.8 A (8 mΩ)	~ 8 A
EPC2016 + EPC2001	10.6 A	14.4 A	10.6 A (0mΩ)	10.3 A (8 mΩ)	~ 10 A
EPC2001 + EPC2001	34 A	14.4 A	14.3 A (8 mΩ)	14.4 A (8 mΩ)	~ 14 A

** Taken from Figure 5*

Table 2: Experimental test cases and calculated optimum on-resistances

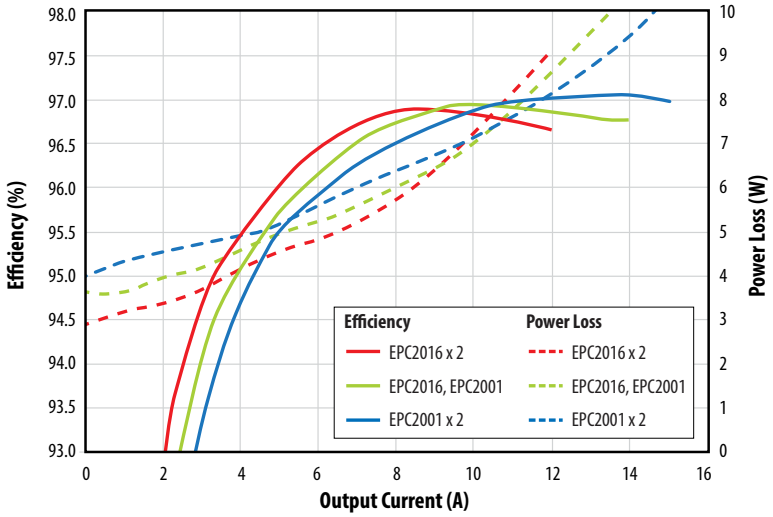


Figure 5: Efficiency and loss curves for different eGaN FETs per Table 2, 45 V_{IN}, 22 V_{OUT}, 1 MHz.

EFFECT OF PACKAGE AND LAYOUT ON OPTIMIZATION

It has been shown [9, 10, 11] that common source inductance (CSI) will significantly increase switching loss for hard switching devices. Equations for the estimation of this increase are complex and somewhat varied. This loss increase, although significant has also been shown to be die size independent for a given device technology [12] and therefore has little impact on die size optimization process. For eGaN FETs in practice, however, the CSI would be a weak function of die size as all the wafer level chip-scale package (WLCSP) inductances will scale with die size, but this complexity is beyond the scope of this paper. Such an inverse relationship between CSI and die size means that some small portion of switching losses actually decreases with increasing die size, even though this may seems counter intuitive.

SUMMARY

Using the simple optimization method presented here is a quick way to find the optimum eGaN FET on-resistance value. As with many simple solutions, the accuracy is limited and the actual optimum resistance may deviate. Furthermore, the optimum combination of die size and on-resistance is also a function of the non-device related equivalent circuit conduction resistance. This paper presents a method for optimization that compensates for these additional current-dependent losses. Experimental results show good agreement through accurate predictions of load current at peak efficiency.

Since eGaN FETs will always optimize to a lower on-resistance than MOSFETs, the overall peak efficiency will therefore be higher (total conduction and switching losses equal at peak) than MOSFETs (given the assumptions made). If the same on-resistance is used, the eGaN FET efficiency will peak at a lower current.

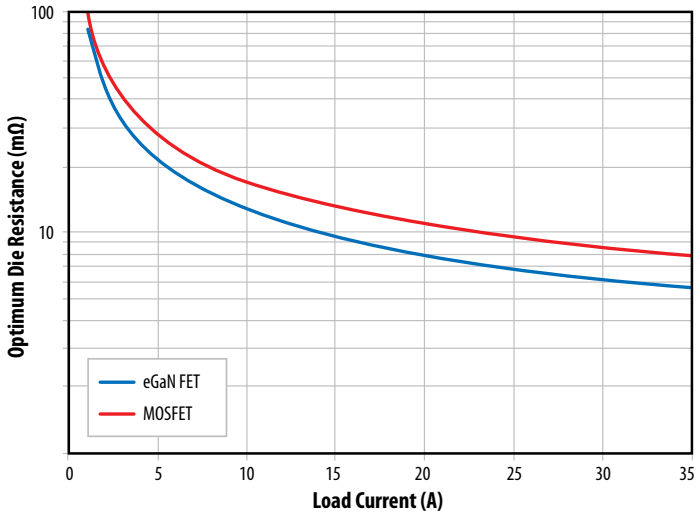


Figure 6: Optimum on-resistance (25 °C) for the control FET (high side) for a 45 V to 22 V / 1 MHz buck converter.

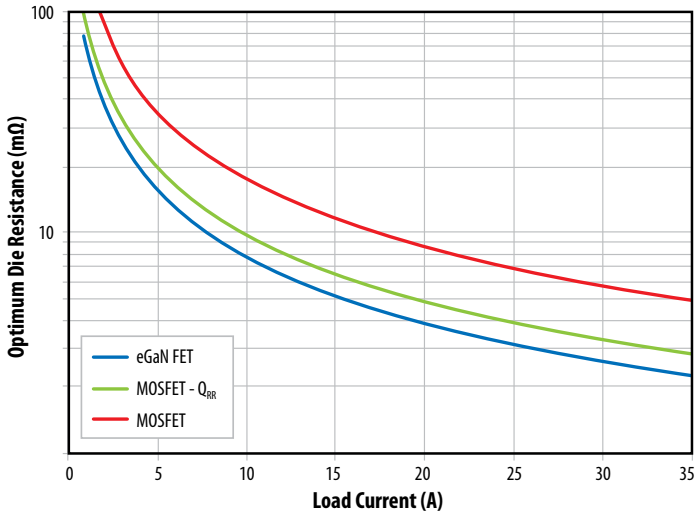


Figure 7: Optimum on-resistance (25 °C) for the synchronous FET (low side) for a 45 V to 22 V / 1 MHz buck converter.

References:

[1] J. Strydom, "eGaN® FET-Silicon Power Shoot-Out Part 1: Comparing Figure of Merit (FOM)", Power Electronics Technology, Sept. 2010, http://powerelectronics.com/power_semiconductors/power_mosfets/fom-useful-method-compare-201009/

[2] J. Strydom, "The eGaN FET-Silicon Power Shoot-Out: 2: Drivers, Layout", Power Electronics Technology, Jan. 2011, http://powerelectronics.com/power_semiconductors/first-article-series-gallium-nitride-201101/

[3] Jon, Klein, "Synchronous buck MOSFET loss calculations with Excel model", Fairchild Semiconductor, App. note AN-6005, http://www.fairchildsemi.com/an/AN/AN-6005.pdf

[4] Jon Gladish, "MOSFET Selection to Minimize Losses in Low-Output-Voltage DC-DC Converters", Fairchild Semiconductor Power Seminar 2008 – 2009.

[5] "Properly Sizing MOSFETs for PWM Controllers", Sipex App. note ANP-20, http://www.exar.com/common/content/document.ashx?id=1245

[6] J. Strydom, "eGaN® FET- Silicon Power Shoot-Out Volume 8: Envelope Tracking", Power Electronics Technology, Apr. 2012, http://powerelectronics.com/power_semiconductors/gan_transistors/egan-fet-silicon-power-shoot-out-volume-8-0430/

[7] EPC2001 datasheet, EPC Corporation, https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2001.aspx

[8] EPC2016 datasheet, EPC Corporation, https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2016.aspx

[9] D. Jauregui, B. Wang, R. Chen, "Power Loss Calculation with Common Source Inductance Consideration for Synchronous Buck Converters", Texas Instruments, SLPA009A, June 2011, http://www.ti.com/lit/an/slpa009a/slpa009a.pdf

[10] W. Eberle, Z. Zhang, et. al, "A Practical Switching Loss Model for Buck Voltage Regulators", IEEE Transactions on Power Electronics, Vol. 24, No. 3, March 2009.

[11] T. Hashimoto, M. Shiraishi, et. al, "System in Package (SiP) With Reduced Parasitic Inductance for Future Voltage Regulator", IEEE Transactions on Power Electronics, Vol. 24, No. 6, June 2009.

[12] Y. Ying, "Device Selection Criteria - Based on Loss Modeling and Figure of Merit", M.Sc. Thesis, Virginia Tech, http://scholar.lib.vt.edu/theses/available/etd-05272008-143141/

APPENDIX

$R_{DS(on),A}$ On state resistance at 100 °C normalized for a die area taken as 1 Ω. All other device parameters are normalized with respect to this.

R_G Resistance of gate drive path – either pull-up or pull-down as needed. This includes a 2 Ω pull-up and a 0.5 Ω pull down driver resistance (that is die size independent) and 0.6 Ω internal eGaN FET gate resistance. This number tends to be die size independent as smaller die have both shorter and narrower effective gate traces. For MOSFETs, the datasheet value is used and also assumed die size independent.

V_{BUS} The DC bus voltage that the switching node sees during operation. e.g. Input voltage for a Buck and output voltage for a Boost.

I_L This is the average inductor current and/or switch current during the switch on-state. Ripple is neglected such that the same value can be used throughout.

D Device on-time duty cycle is the fraction of the total cycle for with the device being optimized is conducting.

f_{SW} This refers to the frequency at which the eGaN FET or MOSFET is switching.

V_{PL} The plateau voltage of a device at rated current. Although this value may vary significantly with load, it is assumed constant during optimization for simplicity.

V_{DR} Gate drive voltage

$Q_{GD,A}$ Miller charge per normalized die area. This is assumed constant for a given bus voltage and calculated from the datasheet values and related charge graph.

$Q_{GS2,A}$ Gate charge between device threshold and plateau voltage per normalized die area. This is constant for a given load current and calculated from the datasheet value at rated current.

$Q_{G,A}$ Total normalized gate charge at given device drive voltage calculated from datasheet.

$Q_{SW,A}$ Total normalized switching charge from reaching threshold to end of plateau.

$Q_{OSS,A}$ Total normalized device output charge a given bus voltage and calculated from the datasheet values and related charge graph.

$Q_{RR,A}$ Total normalized device diode reverse recovery charge taken from the MOSFET datasheets.

V_F Forward drop of the device diode carrying a current I_L.

Δt Total diode conduction interval per switching cycle.

k_{ON} The inverse of the gate current during device turn-on ; assumed constant for optimization.

k_{OFF} The inverse of the gate current during device turn-off; assumed constant for optimization.

Assumptions and approximations

- Common source inductance (CSI) related increase in switching loss is discussed separately, but neglected for optimization purposes.
- Temperature dependence of on-resistance is considered. All values are optimized based on 'typical' datasheet values at 100 °C. To determine the equivalent 25 °C values, the final optimized on-resistance value has to be normalized back to 25 °C.
- Q_{OSS} losses assume one switching edge is ZVS and one is 'hard' switching, i.e. the Q_{OSS} energy is lost at device turn-on or turn-off only.
- Q_{GS2} varies with current at turn-on/off, but the value used is taken from the data sheet at rated current – thus will overestimate this component for lighter loads. It has a smaller impact at higher voltages as shown below. Also the gate drive current for this interval is calculated using the same plateau voltage, thereby overestimating turn-on time and under estimating turn-off.

	40 V	40 V	100 V	200 V
V_{BUS}	12 V	24 V	48 V	100 V
$Q_{GS2,A}$ @ rated I_{DS}	3.5 pC / Ω	3.5 pC / Ω	5 pC / Ω	9 pC / Ω
$Q_{GD,A}$ @ V_{BUS}	6 pC / Ω	7 pC / Ω	14 pC / Ω	35 pC / Ω
$Q_{GD}/(Q_{SW})$	6/9.5 = 0.63	7/10.5 = 0.67	14/19 = 0.73	35/42 = 0.83
Error of Q_{SW} with varying load current	0 to 37%	0 to 33%	0 to 27%	0 to 17%

- Diode losses will vary with die size, but this variation is neglected for the optimization process for simplicity. The diode losses will vary inversely to other charge dependent losses with die size (will actually get smaller with increased die size), but this variation is assumed small in comparison to that of the charge dependent losses.
- The current at turn-on and turn-off are assumed equal and the influence of inductor current ripple is ignored. To quantify the error of doing so, consider turn on at I_L-I_P and turn off at I_L+I_P, then the turn-on/off losses are:

$$\left[\frac{V_{BUS}\cdot(I_L+I_P)}{2}k_{ON}+\frac{V_{BUS}\cdot(I_L-I_P)}{2}k_{OFF}\right]\cdot Q_{SW,A}\cdot A\cdot f_{SW}$$
$$=\left[\frac{V_{BUS}\cdot(I_L)}{2}k_{ON}+\frac{V_{BUS}\cdot(I_L)}{2}k_{OFF}+\frac{V_{BUS}\cdot(I_P)}{2}k_{ON}-\frac{V_{BUS}\cdot(I_P)}{2}k_{OFF}\right]\cdot Q_{SW,A}\cdot A\cdot f_{SW}$$
$$=\left[\frac{V_{BUS}\cdot(I_L)}{2}k+\frac{V_{BUS}\cdot(I_P)}{2}(k_{ON}-k_{OFF})\right]\cdot Q_{SW,A}\cdot A\cdot f_{SW}$$

So the error is an underestimation for eGaN FETs:

$$\frac{I_p\left(k_{ON}-k_{OFF}\right)}{I_L\cdot k}\approx\frac{1}{3}\frac{I_p}{I_L}\approx\frac{1}{6}\frac{I_{pp}}{I_L}$$

for a peak to peak ripple = 30%, then error = 5% (even smaller for MOSFET, where k_{ON} and k_{OFF} values are almost equal.

- Error for soft-switching devices where Q_G is used on driver loss and incorrectly includes Q_{GD}. This error, Q_{GD}/Q_G is about 30% over estimation of soft switching gate drive losses.

Normalize to typical $R_{DS(on)}$ at 100°C (~1.45 x $R_{DS(on)}$ at 25°C)				
	25 V MOSFETs	40 V MOSFETs	80 V MOSFETs	150 V MOSFETs
V_{BUS}	12 V	24 V	48 V	100 V
$Q_{GS2,A}$ @ rated I_{DS}	4 pC/Ω	7 pC/Ω	35 pC/Ω	116 pC/Ω
$Q_{GD,A}$ @ V_{BUS}	6 pC/Ω	21 pC/Ω	55 pC/Ω	96 pC/Ω
$Q_{G,A}$ @ 5 V rated V_{DR}	42 pC/Ω	65 pC/Ω	290 pC/Ω	535 pC/Ω
$Q_{OSS,A}$ @ V_{BUS}	84 pC/Ω	116 pC/Ω	375 pC/Ω	1500 pC/Ω
$Q_{RR,A}$ @ rated I_S	90 pC/Ω	70 pC/Ω	520 pC/Ω	8700 pC/Ω
V_{PL} @ rated I_{DS}	1.8 V	2.4 V	4.6 V	5.7 V
V_F @ rated I_{DS}	0.8 V	0.8 V	0.9 V	1.0 V
$k_{ON}=\frac{R_G}{V_{DR}-V_{PL}}$	2.5/3.2 = 0.78 1 Ω pull up	2.0/2.8 = 0.77 1 Ω pull up	3.0/5.4 = 0.56 1 Ω pull up	3.0/4.3 = 0.7 1 Ω pull up
$k_{OFF}=\frac{R_G}{V_{PL}}$	2.0/1.8 = 1.1 0.5 Ω pull up	1.5/2.4 = 0.62 0.5 Ω pull up	2.5/4.6= 0.54 0.5 Ω pull up	2.5/5.7= 0.44 0.5 Ω pull up
$k = k_{ON} + k_{OFF}$	1.88 / A	1.39 / A	1.10 / A	1.14/ A
$Q_{SW,A}$	10 pC/Ω	28 pC/Ω	90 pC/Ω	212 pC/Ω
ΔI_{EQ}	6.3 A	3.8 A	5 A	6.7 A
ΔI_{EQRR}	9.5 A	3.5 A	10.5 A	72 A

Table 3: State of the art MOSFETs normalized to 1 Ω typical $R_{DS(on)}$ for difference voltage ratings