Improving High Frequency DC-DC Converter Performance with Monolithic Half Bridge GaN ICs

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***Abstract*— The rapid maturation of GaN power transistors continues to enable new capabilities in high frequency power conversion. In this paper we will evaluate one of the latest technological advancements in eGaN® FETs, monolithic integration. The benefits of monolithic integration for GaN power transistors with regards to parasitic reduction, die size optimization, and thermal performance will be discussed. Experimental results for a 12 V_{IN} to 1 V_{OUT} buck converter operating at a switching frequency of 1 MHz and up to 40 A of output current will be demonstrated with 30 V eGaN monolithic half bridge (HB) ICs. For an 80 V eGaN monolithic HB IC, 48 V_{IN} to 1 V_{OUT} and 1.8 V_{OUT} point-of-load (POL) converters will be demonstrated at switching frequencies up to 500 kHz and output currents up to 30 A.**

I. Introduction

There are five basic requirements for a better transistor; (1) lower on-resistance, (2) faster switching speeds, (3) better thermal conductivity, (4) smaller size, and (5) lower cost. Different technologies, such as GaAs or SiC, have been able to improve on one or more of these basic requirements. Gallium nitride transistors, grown on a silicon crystal, can improve upon all of the characteristics just listed when compared with the best silicon devices available [1], [2]. The GaN technology journey is just beginning, and we are still far from theoretical performance limits. It is quite reasonable to expect a rapid rate of improvement reminiscent of Moore's Law, which predicted the growth of microprocessor technology – doubling of product performance every two to four years for at least the next decade.

II. Monolithic Integration of eGaN FETs

Beyond device level and design improvements, the greatest opportunity for lateral GaN technology to impact power conversion comes from its intrinsic ability to integrate multiple devices on the same substrate. In the future, GaN will allow designers to implement higher voltage monolithic power systems on a single chip in a more straightforward and cost-effective manner, as opposed to current silicon multi-chip solutions, which have higher complexity, lower performance, and higher cost.

The most common building block used in power conversion is the half bridge. This therefore becomes the starting point for the journey towards a power system-on-a-chip. On the left in figure 1 is a picture an eGaN FET based half bridge using discrete GaN transistors. On the right in figure 1 is a picture of the first commercially available enhancement mode monolithic half bridge (HB) GaN IC. In these GaN based half bridge ICs the high side FET is approximately one-fourth the size of the low side device to optimize efficient DC-DC conversion with a high V_{IN}/V_{OUT} step down ratio common in buck converters, shown on the bottom of figure 1.

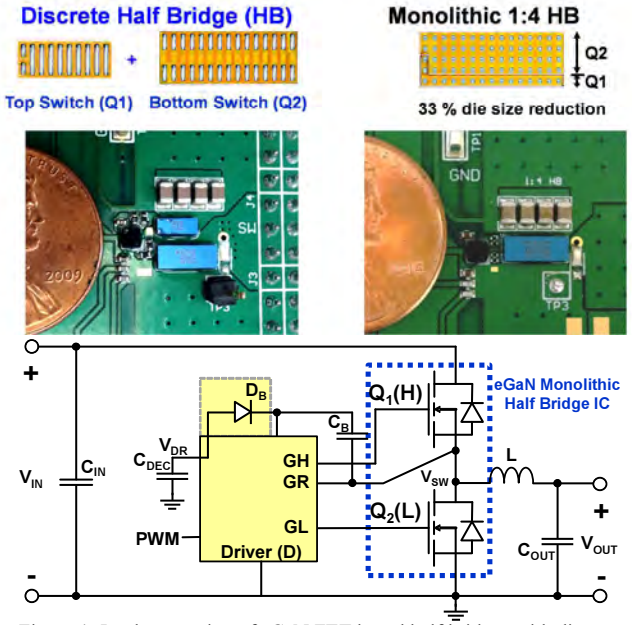

Figure 1: Implementation of eGaN FET based half bridges with discrete transistors (upper left) and an integrated eGaN monolithic half bridge IC (upper right) and schematic of buck converter (bottom)

The eGaN monolithic half bridge IC is the same size as a single discrete eGaN FET. By replacing two discrete devices with a single eGaN monolithic half bridge, a 33% smaller total solution size can be obtained. The removal of the interstitial space between die, coupled with an optimized printed circuit board (PCB) layout [3], results in a significant reduction in the overall power loop inductance to approximately 150pH [4]. In table I, the experimentally measured high frequency loop inductances of discrete eGaN FET based designs are compared with eGaN monolithic half bridge based designs.

TABLE I: APPROXIMATE HIGH FREQUENCY LOOP INDUCTANCES FOR EGAN FET BASED HALF BRIDGE DESIGNS

GaN Based Half Bridge Design	High Frequency Loop Inductance
Discrete eGaN FETs [4]	**0.25 nH**
eGaN monolithic half bridge IC [4]	**0.15 nH**

For applications requiring a more balanced sizing ratio of the transistors, such as class D audio, motor drives, and isolated DC-DC converters, there are also eGaN monolithic half bridge ICs where the high side FET is approximately the same size of the low side device, as shown on the right of figure 2.

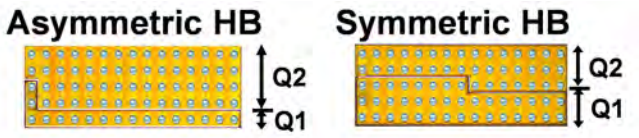

Figure 2: Asymmetric (left) and symmetric (right) eGaN monolithic half bridge ICs

There are three major advantages of monolithically integrating two half bridge devices, Q_1 and Q_2, onto a single chip. The first advantage of monolithic integration is the minimization of parasitic inductances. These induce unwanted voltage stresses and have been demonstrated to reduce switching speeds [3]-[8]. As power devices' FOMs improve, the reduction of parasitics must follow or the system performance will be limited by the tradeoffs designers must make, sacrificing performance for reliable operation. While discrete eGaN FETs in chipscale packages already demonstrate significant advantages over state-of-the-art Si MOSFET module packaging, as the technology rapidly improves so must its packaging. Monolithic integration is a natural packaging evolution for this high voltage lateral technology.

The second advantage of monolithic integration is the ability to efficiently optimize die size. As switching frequencies rise, so to do the switching related losses ($P_{SWITCHING}$) incurred in the top side device (Q_1) and the optimal die size ($A_{OPTIMAL}$) will continue to decrease [2] to minimize total device power loss ($P_{DEVICE}=P_{SWITCHING}+P_{CONDUCTION}$), as illustrated on the top of figure 3. Decreasing the die size (A_{DEVICE}), while simple in theory, poses a number of practical barriers. The first barrier comes in the form of a reduced number of solder bump columns (shown on bottom of figure 3) available for electrical connections. This increases parasitics, which in turn increases switching loss and offsets the advantages of a smaller die size. To minimize parasitics while decreasing die size, the length of the die, shown on the bottom of figure 3, should be maximized, and the width minimized to allow an increased number of electrical connections, where the pitch between electrical connections is set by the voltage rating of the device. The ratio of the length and width of the die, or aspect ratio, is mechanically limited, and electrical connections must be removed in order to decrease die size for a discrete device. This can be seen on the bottom of figure 3 for various commercially available discrete eGaN FETs.

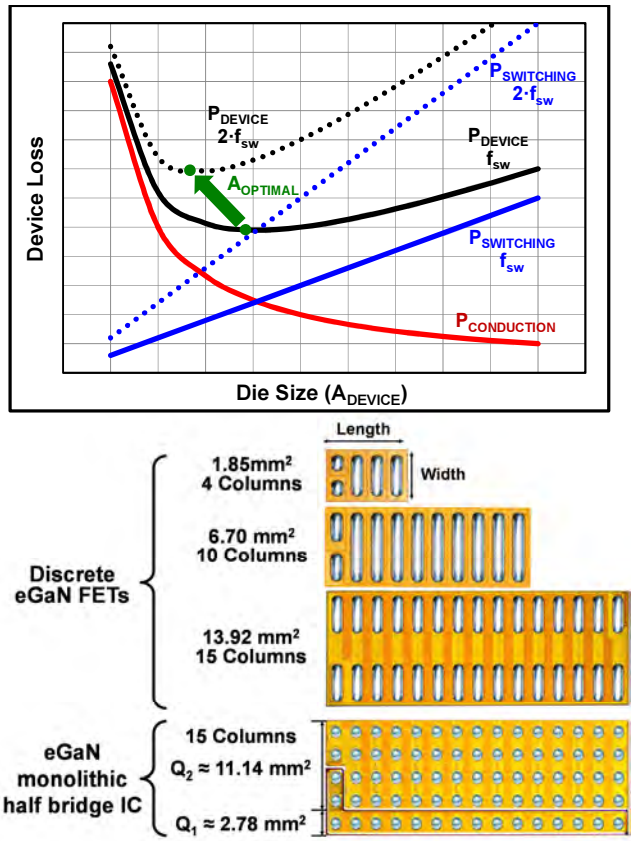

Figure 3: Impact of switching frequency on optimal die size (top) and impact of die size reduction on the number of columns available for electrical connections (bottom)

With eGaN monolithic half bridge ICs, shown on the bottom of figure 3, two devices are contained on a single chip. This allows for the reduction in size of one of the devices while achieving a high aspect ratio, minimizing the package parasitics. For a high step down point-of-load (POL) application, a smaller control FET (Q_1) to reduce the switching related losses and a larger synchronous rectifier (Q_2) to reduce conduction losses, each the respective dominant loss mechanism for devices Q_1 and Q_2, is preferred. The first implementation of a eGaN monolithic half bridge IC designed for high step down POL converters sizes the top device (Q_1) to approximately one fourth of the size of the low side device (Q_2).

The third advantage of monolithic integration is the improvement of thermal performance. Monolithic integration allows highly efficient heat transfer from the smaller sized top device (Q_1) to the larger device (Q_2), giving more balanced heat distribution in the system as well as a more efficient path to distribute heat from the devices to the PCB. Thermal evaluations of discrete and eGaN monolithic half bridge ICs are covered in detail in [9].

III. 1 MHz eGaN Monolithic Half Bridge IC based 12 V_{IN} to 1 V_{OUT} POL Buck Converter

Current Si based POLs are limited to the range of a few hundred kilohertz to approximately one megahertz [10]-[12]. To advance the high frequency performance of silicon based POL converters many efforts have been made to improve device characteristics and packaging. For improved device performance, the switching related parameters critical to the top switch, Q_1, gate to drain charge (Q_{GD}) and gate to source switching charge (Q_{GS2}) have been decreased. The body diode reverse recovery (Q_{RR}) and body diode forward voltage (V_{DF}) for the low side device, Q_2, have been improved with the addition of an internal Schottky diode. Advanced drivers have also been developed to minimize dead time losses and gate charge (Q_G) has been reduced. Advanced packaging techniques have improved performance by providing reduced parasitic inductances and resistances. For higher current, lower resistance synchronous rectifiers have been developed and advanced packaging has enabled greater transistor density through techniques such as 3D die stacking [10], [13].

While there have been advances in silicon power device based POL designs, the pace has slowed as device performance approaches its theoretical limit [1], and further packaging improvements are limited by the trench device structure [14]. POL designers are trying to squeeze more performance from aging Si technology, with each generation producing fewer returns. GaN technology, as we will demonstrate in this section, meets the demand for high frequency, high power density, high current POLs.

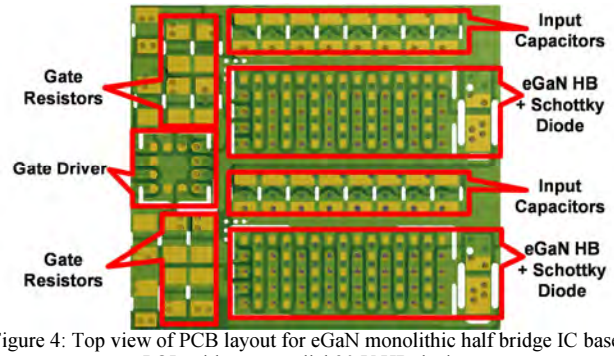

Figure 4: Top view of PCB layout for eGaN monolithic half bridge IC based POL with two parallel 30 V HB devices

From the performance of previous discrete eGaN FET based POLs [2], [9], a lower resistance low side device (Q_2) is required for better high current performance. Using a single commercially available 30 V eGaN monolithic half bridge IC (EPC2100), the die size for Q_2 would be approximately 25% smaller than the discrete 30 V (EPC2023) eGaN FET used previously, so two 30 V eGaN monolithic half bridge ICs are selected and will be designed in parallel. The total device area for the top device (Q_1) using two parallel HBs is approximately 20% smaller than the discrete design which used a 40 V EPC2015C. By selecting a more suitable 30 V rating for the top device, an approximately 25% lower switching FOM can be gained.

To obtain the best performance when using high speed eGaN FETs operating in parallel, it has been demonstrated that the parasitics must not only be minimized, but they also must remain balanced to ensure good dynamic current sharing [15]. Shown in figure 4 is the top layer of the four-layer EPC9059 demonstration board [16]. A single LM5113 gate driver is located between the two eGaN monolithic half bridge ICs. Each HB has separate pull-up and pull-down resistors to give the option of controlling gate speed and keep the gate drive loop parasitics approximately the same by providing good gate drive symmetry. This also avoids parasitic oscillation between the gates [17]. In this design the gate resistors were populated with a value of zero Ω. Two identical optimal high frequency power loops [3] were created for each HB with their own high frequency input capacitors (8 pcs of 0402 25 V X5R 20% 2.2 µF ceramic capacitors) and chipscale packaged Schottky diode (Diodes incorporated SDM2U30CSP).

The total system efficiency and power loss comparisons of the eGaN FET and Si MOSFET based 12 V_{IN} to 1 V_{OUT} buck converters operated at a switching frequency of 1 MHz are shown in figure 5. This includes the losses of the entire system, including the inductor, capacitors, and PCB losses. The eGaN monolithic half bridge IC based POL buck converter with two parallel 30 V HB devices (EPC2100) has higher efficiency than the Si MOSFET based solutions at every operating point. At a light load condition of 10 A, the eGaN FET based design has an over 1.5% efficiency advantage. At a heavy load condition of 40 A, the efficiency advantage is around 2.5%, which translates to an almost 20 % reduction in total system power loss.

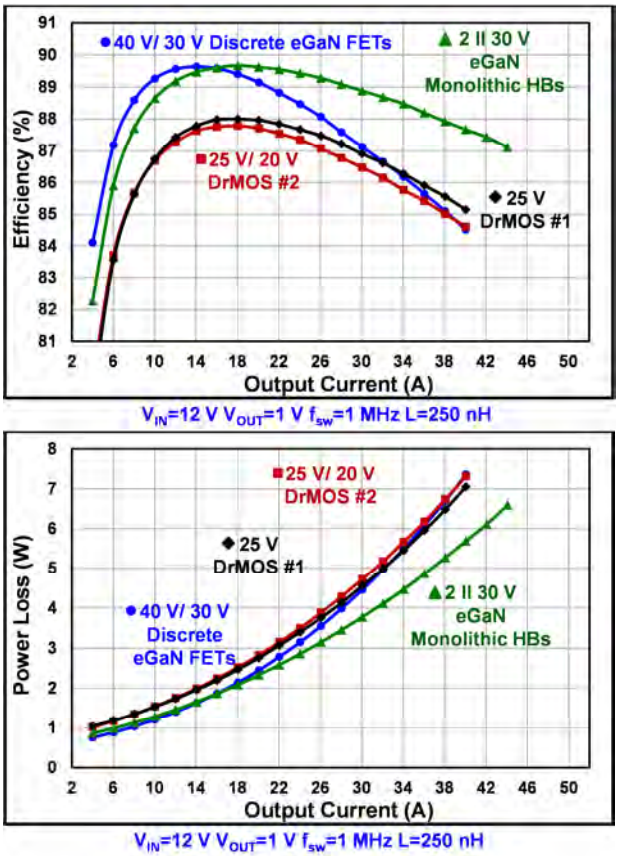

Figure 5: Experimental electrical comparison between GaN and Si based buck converters, V_{IN}=12 V to V_{OUT}=1 V, f_{sw}=1 MHz (L=Würth Elektronik 744 309 025)

At a nominal 12 V_{IN}, the switching waveform of the eGaN monolithic half bridge IC based POL buck converter with two parallel 30 V HB devices is shown in figure 6, and an approximate peak voltage of 14 V was measured for the converter. With the reduced parasitics provided by the monolithic HB combined with the low FOM eGaN FETs and die size optimization, low overshoot, fast switching speeds, and high efficiency can be achieved.

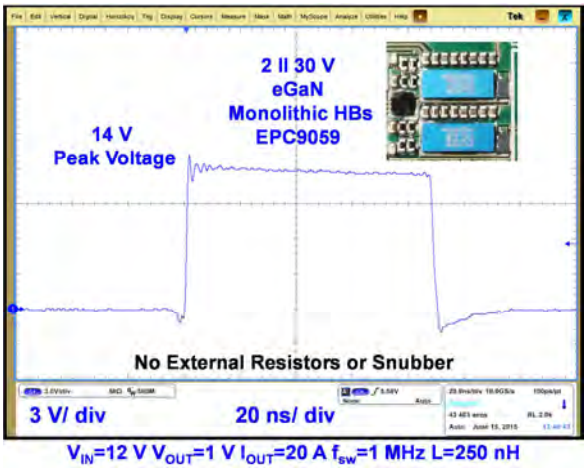

Figure 6: Synchronous rectifier switching waveforms (V_{SW}) of eGaN monolithic half bridge IC based POL buck converter with two parallel 30 V HB devices (EPC2100)

IV. eGaN Monolithic Half Bridge IC based 48 V_{IN}-1 V_{OUT} POL Converter

In this section the ability of eGaN FETs to enable new power delivery approaches that can improve overall system efficiency, power density, and cost will be evaluated. When the state of the art intermediate bus architecture (IBA), shown on top in figure 7, was first introduced, the benefits of replacing a single power conversion stage (DPA) with two power conversion stages to improve system performance was not readily apparent. But, as the number of load voltages increased and the load demands became more complex, the architecture provided better performance with its divide-and-conquer approach. A highly efficient first stage bus converter [18] converts the 48 V_{IN} at lower currents, a byproduct of the isolation transformer, and the second stage high frequency 12 V_{IN} non-isolated POLs provide the power to the various loads.

Since the adoption of the IBA, the power demands of data and telecom systems have continued to increase and, with emerging trends like cloud computing, the system power demands show no signs of slowing down. Bus converters are currently approaching an order of magnitude increase in output power since the adoption of the IBA, from around 100 W to current designs of around 1 kW in a quarter brick footprint. This means that the amount of current on the 12 V bus to the POL converters has also increased by a factor of 10 and, without reductions in bussing resistance, a two-order-of-magnitude increase in bussing conduction losses. With the increasing conversion losses in the 48 V_{IN} bus converter, and the mounting 12 V bussing losses on the motherboards, different architectures are being considered. One approach is going directly from 48 V_{IN} to load using non-isolated POL converters, as shown on the bottom of figure 7. By removing the 12 V intermediate bus this approach can be viewed as a return to the distributed power architecture, without isolation, a subject we will discuss at the end of the section.

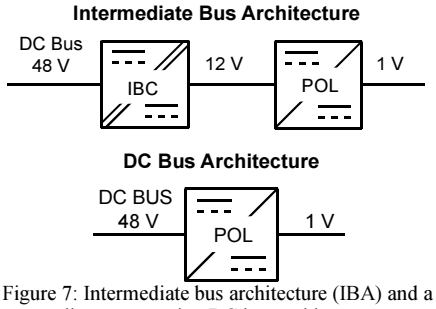

Figure 7: Intermediate bus architecture (IBA) and a direct conversion DC bus architecture

To evaluate converting 48 V_{IN} directly to 1 V_{OUT}, an 80 V eGaN monolithic half bridge IC (EPC2105), embedded in an EPC9041 demonstration board [16], was selected for the much higher step down ratio. The total system efficiency and power loss for the eGaN FET based 48 V_{IN} to 1 V_{OUT} buck converter operated at switching frequencies of 300 kHz and 500 kHz are shown in figure 8. This efficiency includes the losses of the entire system, including the inductor (Würth Elektronik 744 301 033), capacitors, and PCB losses. At 500 kHz, a peak efficiency of over 80% is achieved for the full buck converter system. At 300 kHz, a peak efficiency of 84% is achieved for the full buck converter system, and at 20 A the efficiency is around 83.5%.

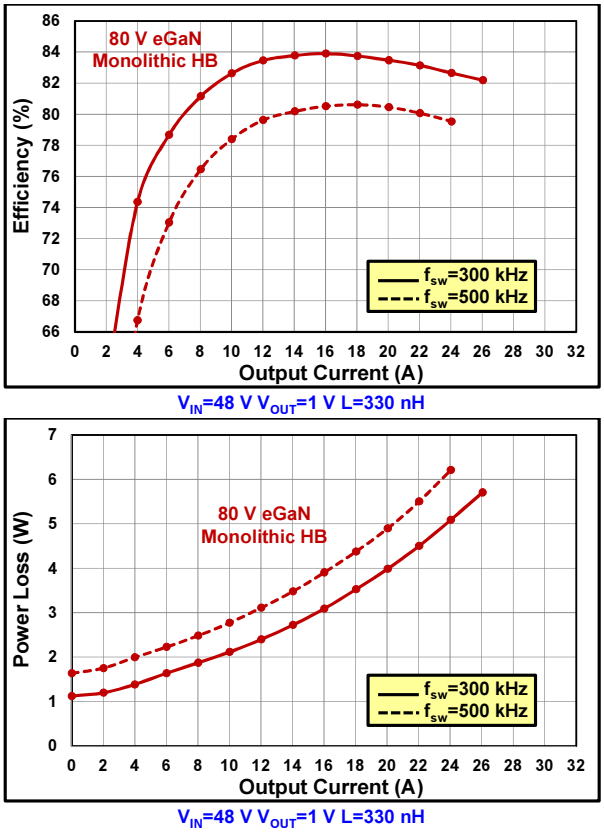

Figure 8: Experimental efficiency and power loss curves for eGaN monolithic HB IC based POL, V_{IN}=48 V to V_{OUT}=1 V, f_{sw}=300 kHz, 500 kHz

The switching waveform for the 48 V_{IN} to 1 V_{OUT} POL converter is shown in figure 9. The switching rise and fall times are measured to be approximately 2 ns for the eGaN monolithic half bridge IC based POL. To realize the high step down ratios and narrow pulse widths required to convert 48 V_{IN} to load, the 5 ns to 10 ns rise and fall times of Si MOSFETs are not practical, and GaN can be an enabling technology. In addition to eGaN FET devices capable of these switching speeds, controllers and gate drivers capable of generating and controlling the narrow pulse widths are required. The development of digital and conventional controllers suitable for these applications is advancing and the number of 48 V_{IN} non-isolated POL product offerings, currently limited in frequency and output current by Si MOSFET technology, are growing [19]-[23].

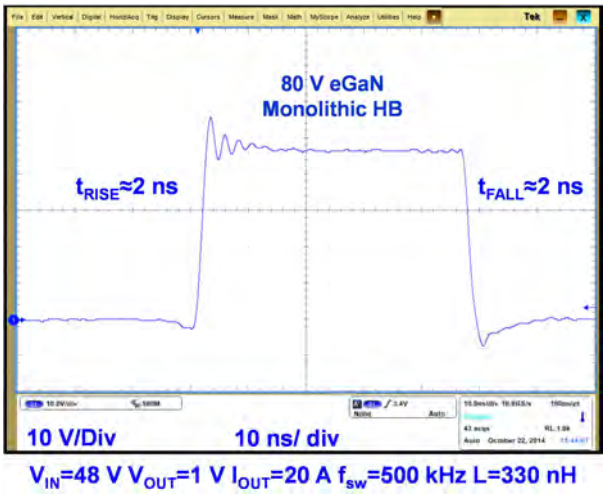

Figure 9: Synchronous rectifier switching waveform (V_{SW}) of eGaN monolithic half bridge IC based POL, V_{IN}=48 V to V_{OUT}=1 V, f_{sw}=500 kHz

A comparison of estimated efficiencies and power densities for the single stage 48 V_{IN} to 1 V_{OUT} POL converter, and the traditional two stage IBA approach using the designs discussed in [9], [18] and the POL section of this paper are shown in figure 10 and summarized in table II. The IBA's power converters have an estimated 1.5% efficiency improvement over the direct 48 V_{IN} to 1 V_{OUT} conversion. When considering the 12 V bus, whose efficiency is estimated to be 98% [24]-[26], the total system efficiencies are very similar. The estimated power density of the 48 V_{IN} to 1 V_{OUT} direct conversion approach is estimated to be 20% higher than the IBA, but at a switching frequency of 300 kHz additional output bulk capacitance for transient response would likely be required [27], [28] decreasing the power density.

While a definitive performance advantage of the single stage 48 V_{IN} to 1 V_{OUT} DC bus architecture for current high performance computing systems is not shown here, some advantages are apparent. The DC bus architecture shows a clear cost advantage as the cost of the IBC can be eliminated, and the cost increase of the 48 V_{IN} POL over the 12 V_{IN} POL will be minimal as they use a similar number of power devices, controllers, and drivers. From a forward looking efficiency and power loss perspective, the DC bus architecture shows a much greater potential for improvements due to the higher performance GaN transistors. As the 12 V bus power levels continue to increase in the IBA, the bussing losses and intermediate bus converter magnetic related losses become larger, and better power devices will not resolve this issue. For example: The magnetic related losses in the IBC demonstrated in [9], [18] represented roughly half of the full load power loss. In the direct 48 V_{IN}-to-load conversion approach, the device is the major loss contributor and device improvements will have a significant impact on both converter efficiency and frequency and power density capability.

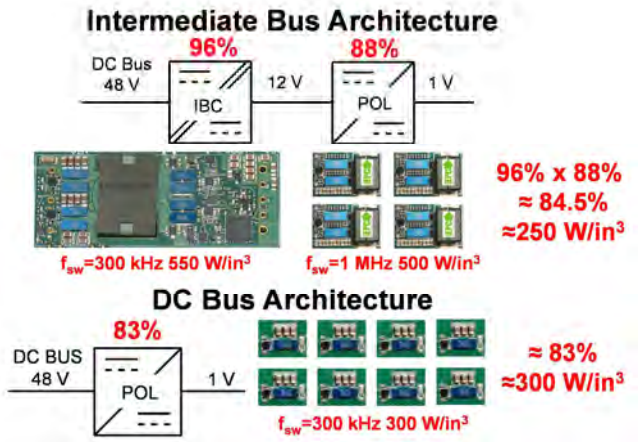

Figure 10: Performance comparisons of 48 V_{IN} intermediate bus architecture and 48 V_{IN} DC bus architecture

TABLE II: SUMMARY OF 48 V_{IN} INTERMEDIATE BUS ARCHITECTURE AND 48 V_{IN} DC BUS ARCHITECTURE PERFORMANCE COMPARISONS

Parameter	Units	48 V_{IN} IBA		48 V_{IN} Direct Conversion
		48 V_{IN} – 12 V_{OUT} IBC	12 V_{IN} – 1 V_{OUT} POL	48 V_{IN} – 1 V_{OUT} POL
Stage Switching Frequency	kHz	300	1000	300
Total Power Devices[a]		32[b]		32[b]
System Transformer Isolation		Yes		No
PCB Complexity		High	Low	Low
Stage Efficiency	%	96	88	83
Bus Efficiency	%	98[c]		99.9%
Total System Efficiency	%	82.8		82.9
Stage Power Density	W/in^3 (W/cm^3)	550 (34)	500 (31)	300[d] (18)
Total System Power Density	W/in^3 (W/cm^3)	250 (15)		300[d] (18)

(a) Scaled to 500 W of output power.
(b) For 12 V_{IN}, a single 30 V eGaN monolithic half bridge IC is assumed to have a steady state current capability of approximately 20 A at a switching frequency of 1 MHz. For 48 V_{IN}, a single 80 V eGaN monolithic half bridge IC is assumed to have a steady state current capability of approximately 15 A at a switching frequency 300 kHz. These operating points are estimated from measured in-circuit thermal performance with minimal air flow and no additional heat sinking [9].
(c) Average based on reported 97-99% bus efficiencies [24]-[26].
(d) This power density assumes no additional output capacitance required due to lower switching frequency operation (ESR/ESL limited operation).

V. EGAN MONOLITHIC HALF BRIDGE IC BASED 48 V_{IN}-1.8 V_{OUT} BUS CONVERTER

Recent developments in placing high frequency buck regulators directly on the microprocessor (up to 140 MHz

switching frequencies) [29], [30] has changed the way power is delivered to CPUs. The new intermediate bus architecture with high frequency buck converter integration is shown in figure 11. The 48 V_{IN}-to-12 V_{OUT} IBC remains unchanged, but now the 12 V_{IN} POL, which was previously used to directly power the CPU, now serves as a second IBC stage and the dynamically regulated POL conversion is done at the microprocessor level from 1.8 V_{IN}-to-load. With the new 1.8 V bus, the architecture has grown to three power delivery stages.

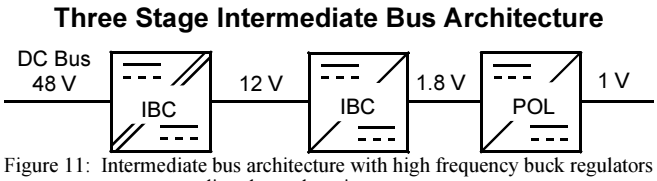

Figure 11: Intermediate bus architecture with high frequency buck regulators directly on the microprocessor

For architectures with a 1.8 V bus, the major transients are now handled by the 1.8 V_{IN} POL converter and the frequency demands of a 48 V_{IN} to 1.8 V_{OUT} single stage power converter are more about power density than transient response. To evaluate converting 48 V_{IN} to 1.8 V_{OUT}, the 80 V eGaN monolithic half bridge IC (EPC2105) was chosen. The total system efficiency and power loss for the eGaN FET based 48 V_{IN} to 1.8 V_{OUT} buck converter operated at switching frequencies of 300 kHz and 500 kHz are shown in figure 12. Once again we are including the losses of the entire system, including the inductor (Würth Elektronik 744 301 047), capacitors, and PCB losses.

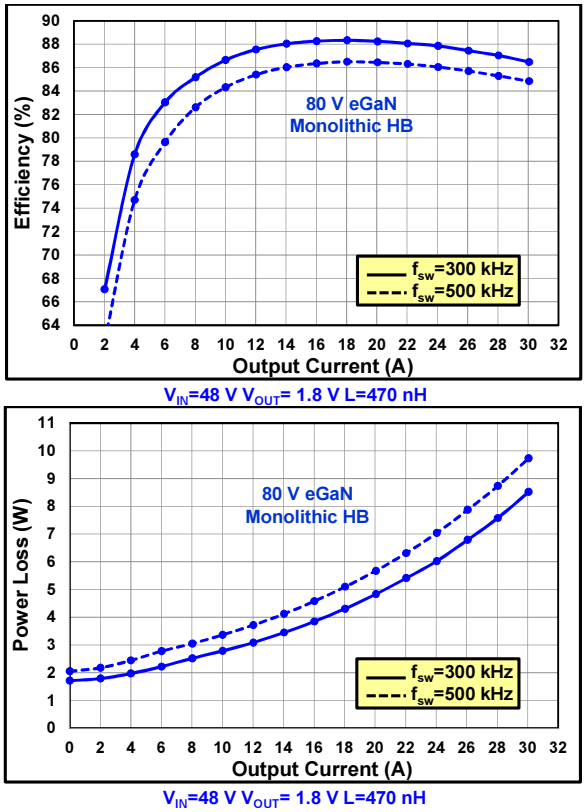

Figure 12: Experimental efficiency and power loss curves for eGaN monolithic half bridge IC based non-isolated bus converter, V_{IN}=48 V to V_{OUT}=1.8 V, f_{sw}=300 kHz and 500 kHz

A comparison of estimated efficiencies and power densities for the two stage 48 V_{IN} to 1.8 V_{OUT} non-isolated IBA, and the traditional three stage IBA approach using the designs discussed in [9], [18] and the POL section of this paper are shown in figure 13 and summarized in table III. The three stage IBA power converters have an estimated 1.3% efficiency improvement over the direct 48 V_{IN} to 1.8 V_{OUT} conversion approach, but it should be noted that no 12 V bussing losses are included. When considering the 12 V bus, whose efficiency is estimated to be 98% [24]-[26], the total system efficiency of the direct 48 V_{IN} to 1.8 V_{OUT} conversion approach is around 0.5% higher and the estimated power density has been improved by more than 65% compared with the conventional three stage IBA and, when operated as a non-isolated IBC at the switching frequency of 300 kHz, it will likely not require additional output capacitance for load transients. There is a clear cost and power density advantage by removing one of the redundant bus conversion stages, and by having a single bus converter from 48 V_{IN} to 1.8 V_{OUT}.

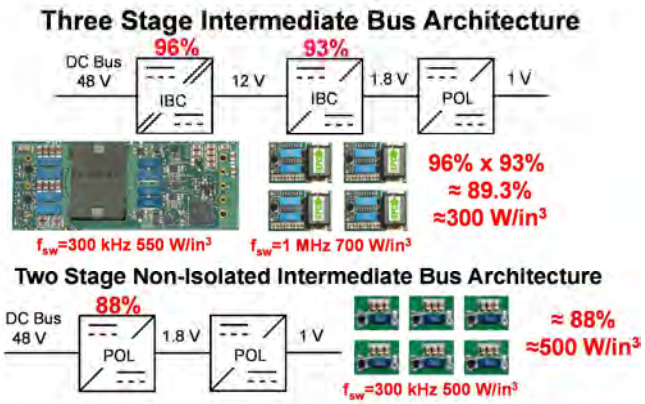

Figure 13: Performance comparisons of 48 V_{IN} three stage and two stage non-isolated intermediate bus architecture

TABLE III: SUMMARY OF 48 V_{IN} THREE STAGE AND TWO STAGE NON-ISOLATED INTERMEDIATE BUS ARCHITECTURE PERFORMANCE COMPARISONS

Parameter	Units	48 V_{IN} IBA		48 V_{IN} Direct Conversion
		48 V_{IN} – 12 V_{OUT} IBC	12 V_{IN} – 1.8 V_{OUT} IBC	48 V_{IN} – 1.8 V_{OUT} IBC
Stage Switching Frequency	kHz	300	1000	300
Total Power Devices[a]		22 [b]		18 [b]
System Transformer Isolation		Yes		No
PCB Complexity		High	Low	Low
Stage Efficiency	%	96	93	88
Bus Efficiency	%	98[c]		99.9%
Total System Efficiency	%	87.5		87.9
Stage Power Density	W/in³ (W/cm³)	550 (34)	700 (43)	500 (31)
Total System Power Density	W/in³ (W/cm³)	300 (18)		500 (31)

(a) Scaled to 500 W of output power
(b) For 12 V_{IN}, a single 30 V eGaN monolithic half bridge IC is assumed to have a steady state current capability of approximately 20 A at a switching frequency of 1 MHz. For 48 V_{IN}, a single 80 V eGaN monolithic half bridge IC is assumed to have a steady state current capability of approximately 15 A at a switching frequency 300 kHz. These operating points are estimated from measured in-circuit thermal performance with minimal air flow and no additional heat sinking [9].
(c) Average based on reported 97-99% bus efficiencies [24-26].

The non-isolated step down approaches in this section do not serve as a design guide for new power architectures, but as an exercise to evaluate the feasibility of GaN technology to eliminate the number of stages currently required for DC-DC power conversion. The approach of non-isolated power conversion from 48 V_{IN} is met with some skepticism by system designers due to concerns regarding safety, reliability, and EMI. However, these same designers are always under pressure to pack more power into less space. As the IBA matures, the system improvements realized by taking traditional approaches with aging Si technology will continue to slow. As for any recently introduced approaches, new technical challenges must be overcome as precursors to adoption. With power architectures in telecom and datacom systems as an example, there were hurdles the intermediate bus architecture had to overcome to supplant the distributed power architecture, which itself had to prove its worth when replacing its predecessor, the centralized power architecture. In this section, we have demonstrated the feasibility of a non-isolated GaN transistor based approach to 48 V_{IN} power conversion in both current and future systems. The authors plan to further study more non-isolated and isolated topological approaches to assess the potential of the 48 V_{IN} to load architecture.

VI. Conclusions

This paper evaluated the benefits of monolithically integrating GaN power transistors. These eGaN monolithic half bridge ICs are the initial building blocks to more efficient high frequency power conversion, and just the beginning of the journey towards a GaN based high voltage power system-on-a-chip. For low voltage applications, a 12 V_{IN} to 1 V_{OUT} eGaN monolithic half bridge IC based POL with two parallel 30 V HB devices operated at a switching frequency of 1 MHz demonstrated 20% lower power loss than state-of-the-art multi-chip Si MOSFET modules. Beyond demonstrating performance improvements possible with eGaN FETs in traditional applications, this paper focused on the ability of eGaN FETs to enable a new approach to the traditional intermediate bus architecture. Direct 48 V_{IN} to load power conversion allows for the removal of a power conversion stage and it was shown that with the significant performance improvements provided with GaN power devices, a single stage approach in telecom and datacom systems can yield higher power densities and lower system cost with similar system efficiencies.

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